MODEL 6637, 6638, 6647, 6648
PROGRAMMABLE SWEEP GENERATORS
OPERATION AND MAINTENANCE
MANUAL

APPLICABLE SERIAL NUMBERS

D-8000 Basic Frame:	101001 & up*
6637 RF Deck:	103001 & up**
6638 RF Deck:	101001 & up
6647 RF Deck:	103001 & up
6648 RF Deck:	101001 & up

*On inside of rear panel.

**On outside of rear panel.

WILTRON

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2-6637/6647-OMM
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WARRANTY

All products are warranted against defects in materials and workmanship for one year from the date of shipment except YIG-tuned oscillators, which have a two-year warranty period. Our obligation covers repairing or replacing products which prove to be defective during the warranty period and which shall be returned with transportation charges prepaid to WILTRON. Obligation is limited to the original purchaser. We are not liable for consequential damages.

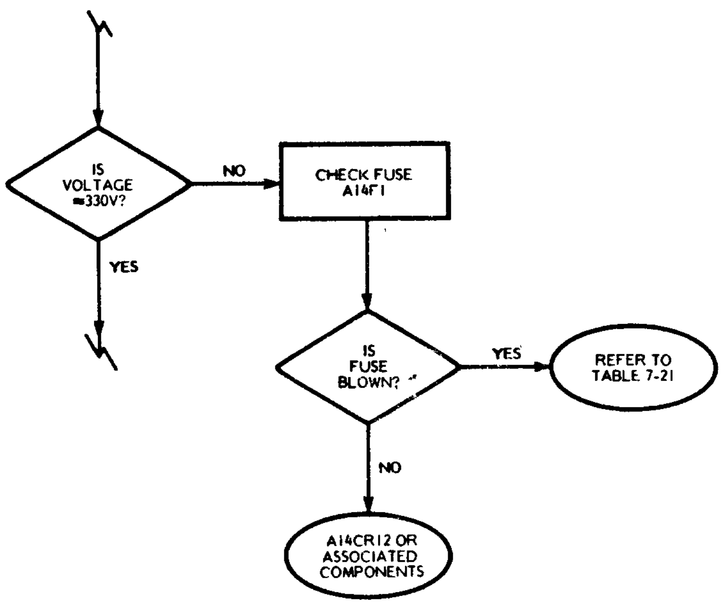
<u>**MANUAL CHANGES**</u>

6637, 6638, 6647, 6648 OPERATION AND MAINTENANCE MANUAL
(Issue 2, Printed January 1982)

CHANGE #1

Serial Numbers Affected
All

A. On page 7-164, Figure 7-87, at the top diamond in the third column, modify as shown below.



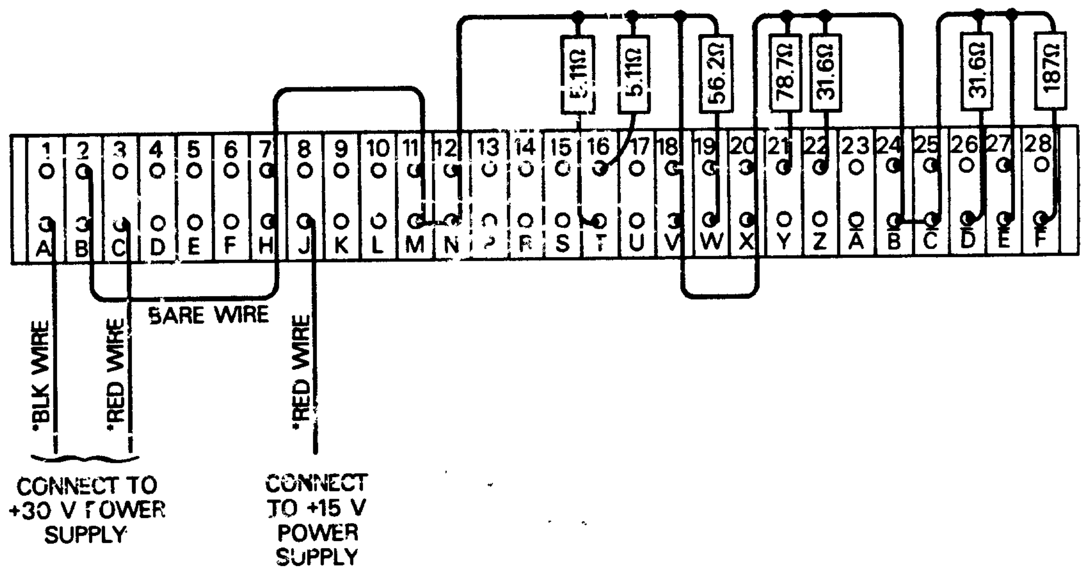
B. On page 7-2, add the following items to Table 7-1, "Recommended Test Equipment":

INSTRUMENT	CHARACTERISTICS	MANUFACTURER
DC Power Supply	3 volts @ 3 amps.	HP 6281
Dual DC Power Supply	1 supply = 0 to 7V. 1 supply = +15V. Common ground OK.	HP 6236B
DC Power Supply	30V – Isolated from ground and other voltage supplies.	HP 6216

CHANGE #1 (continued)

C. After page 7-165, add the following figures and table:

A13 PCB TEST CONNECTOR - END VIEW



*WIRE SHOULD BE 24-GUAGE, APPROXIMATELY 2 FT IN LENGTH.

Resistor Legend

PURPOSE	PINS*	VALUE (OHMS)
Load for +5V Supply	16, T 17, U	5.11 (2 ea.)
Load for -18V Supply	22, Z 23, $\overline{A}$	31.6
Load for +18V Supply	26, $\overline{D}$	31.6
Load for -12/+24V Supply	19, W	56.2
Load for +28V Supply	21, Y	78.7
Load for -43V Supply	28, $\overline{F}$	187

*Other resistor lead connects to ground bus

A13 Test Connector Parts List

NAME	WILTRON PART NO.
Connector-Receptacle, 56-pin	551-198
Resistor, 5.11Ω, 1/8W*	110-5.11-1
Resistor, 31.6Ω, 1/8W**	110-31.6-1
Resistor, 56.2Ω, 1/8W	110-56.2-1
Resistor, 78.7Ω, 1/8W	110-78.7-1
Resistor, 187Ω, 1/8W	110-187-1

*Resistor values are not critical.

**2 ea.

Figure 7-90a. A13 PCB Test Connector

C. (continued)

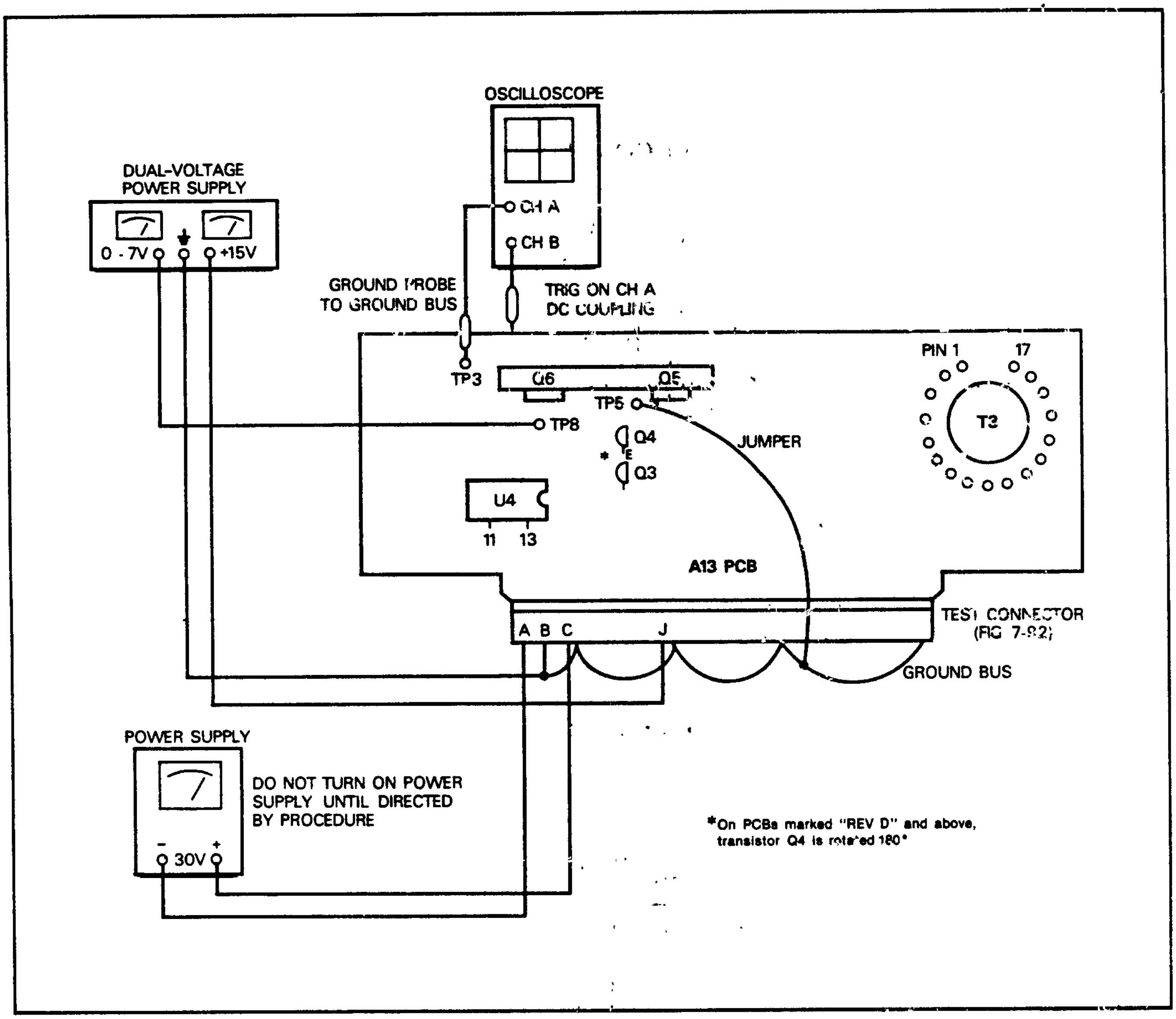


Figure 7-90b. Test Equipment Setup for A13 PCB Benchtop Tests

C. (continued)

Table 7-21. A13 PCB Low-Voltage Troubleshooting Procedure

General: This table provides instructions for troubleshooting the A14 PCB overcurrent-protection and A13 PCB voltage-supply circuits. The table, which is an extension of the "IS VOLTAGE ≈330V?" decision block in Figure 7-87, starts with the fact that (1) fuse A14F1 is blown, and (2) the A13 PCB caused it to blow.

Part 1 of this procedure describes troubleshooting the A14 overcurrent-protection circuit. This troubleshooting will detect whether Over-Current Sense IC U1 was destroyed by the over-current condition. Part 2 describes a low-voltage, benchtop method for troubleshooting the A13 PCB. Such a method is necessary because of the hazardous voltages present when the A13 PCB is operating from line voltage.

Part 1, Troubleshooting the A14 PCB Overcurrent-Protection Circuit

1. Turn off the sweep generator, disconnect the line cord, and wait at least 5 minutes for capacitor voltages to decay to a safe level.
2. Remove the voltage-protection shield from the underside of the A14 PCB.
3. Connect the positive (+) lead of a 3A, 3V dc power supply (HP 6281 or equivalent) to the lead on A14R6 that is nearest the rear panel.
4. Connect the positive (+) lead of a digital multimeter (DMM) to XA13, pin F or 6, and the negative (-) lead to chassis ground; set up the DMM to read ohms (10kΩ scale). A reading of ≈18kΩ should be observed.
5. Momentarily (≤5 seconds) touch the power supply's negative (-) lead to the other side of A14R16; observe the resistance reading on the DMM. A reading of <1 kΩ indicates that U1 is good.

NOTE

While the resistance of A14U1 is being read, ensure that (1) A14R16 draws 3 amps of current and (2) the voltage across it stays at 3 volts.

6. Replace faulty components and reinstall voltage-protection shield; then proceed to Part 2.

Part 2, Troubleshooting the A13 PCB Voltage-Supply Circuits

1. Remove the A13 PCB from the sweep generator and place on a suitable work surface.
2. Install the A13 PCB Test Connector (Figure 7-90a).
3. Inspect the PCB and replace any obviously damaged components.
4. Remove the jumper from between test points 7 and 8, and connect a jumper between TP5 and the ground bus.

Table 7-21. A13 PCB Low-Voltage Troubleshooting Procedure (continued)

CAUTION

It is recommended that the A13 PCB be tagged with a label warning that the TP7-TP8 test jumper is removed. If this jumper is not in place while line voltage is applied, the switching power supply operates unregulated, and serious damage could occur to power supply circuits.

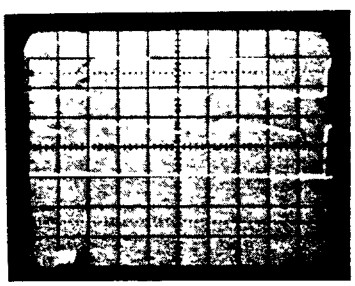
5. Connect the dual-voltage power supply as shown in Figure 7-90b.

6. Turn on the power supply, and set the variable (0-7V) supply to +5 volts and the fixed (+15V) supply to +15 volts.

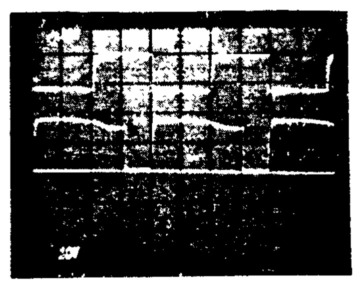
7. Connect the 30V supply as shown in Figure 7-90a, but DO NOT TURN IT ON.

8. Connect Channel A of the oscilloscope to TP3 and observe the 50 kHz oscillator pulse. This pulse supplies the reference-timing pulse for future waveform analysis.

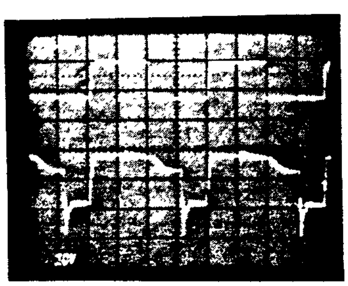
9. Using Channel B of the oscilloscope, check the waveforms at U4, pins 11 and 13, and at the emitters of Q3 and Q4. These waveforms should resemble those in figures "A" thru "D" below. Varying the +5V variable supply's voltage should cause the pulse width (PW) to vary: 0V should provide maximum PW, and ≈6.5V should shut the circuit down (both the test and sync signals will disappear).



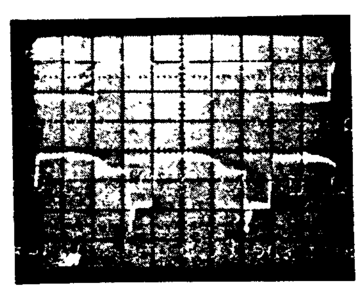
A



B



C

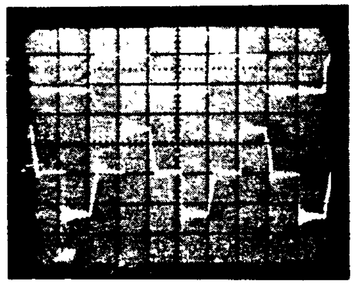


D

10. Reset the variable supply to +5 volts.

Table 7-21. A13 PCB Low-Voltage Troubleshooting Procedure (continued)

11. Turn on the 30-volt supply, and check the waveform at T3, pin 1. The waveform should resemble "E" below.



E

12. Check the A13 output voltages at the "hot" side of the load resistors. As the input 0-7V supply is varied from min. to max., the A13 voltages should vary as shown below.

+5V Supply, Pin 16	from 0 to ≈ +0.6 volts
-18V Supply, Pin 22	from 0 to ≈ -2.5 volts
+18V Supply, Pin $\overline{D}$	from 0 to ≈ +2.5 volts
-12/+24V Supply, Pin 19	from 0 to ≈ -3.0 volts
+28V Supply, Pin 21	from 0 to ≈ +4.0 volts
-43V Supply, Pin $\overline{F}$	from 0 to ≈ -6.5 volts

13. After completing the A13 tests and repairs, reinstall the jumper between test points 7 and 8 before reinstalling the PCB into the sweep generator.

CAUTION

To prevent possible damage to A13 should a short still exist, perform the following before applying full line voltage to the sweep generator:

- Inspect resistors A14R99, A14R100, and A14R101 for evidence of overheating. These resistors respectively fuse the -12/+24V, +28V, and +18V unregulated supplies.
- Use a variac to apply line power. Bring the line voltage up slowly while observing the A14 "SHUT DOWN" LED. If a short is still present, this LED should start flashing (A13 cycling on and off) between 80 and 100 Vac.

February 18, 1982

CHANGE #2

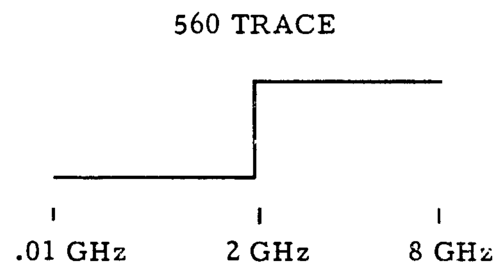
Serial Numbers Affected
All

A. On page 5-36, add the following note after step d.6.(b):

NOTE

If unable to obtain equal traces with A4R70 (above), adjust the A4U4 offset potentiometer (Figure 5-41A); then readjust A4R70 as described above.

B. After page 5-36, insert the following figure (Figure 5-41A).



Adjust A4R5 to bring the .01-2 GHz trace below the 2-8 GHz trace, as shown.

Figure 5-41A. Potentiometer A4R5 Adjustment

February 18, 1982

CHANGE #3

Model	Serial Nos. Affected	Manual Print Date
Mainframe D-8000	104001 and up	January 1982

A. On page 7-81, add the following to the end of the paragraph beginning, "When any of the above three conditions....":

"The **L CW MODE** line that also connects to this circuit prevents a dip in power when the sweeper is in a CW mode and the rear panel HORIZ OUTPUT DURING CW switch is ON."

B. On page 7-92, add the following to the end of the paragraph beginning, "The center frequency group is loaded....":

"The other A5 PCB input affecting the **F CEN** signal line is **FREQ OFFSET.** This line is only active when the sweep generator is part of a Model 661 Tracking Sweeper Controller

CHANGE #3 (Continued)

System. At that time, the voltage present on this line offsets the **F CEN** signal, as determined by the tracking sweeper controller.

C. On page 7-93, add the following paragraph to the bottom of the second column:

"The **L CW MODE** signal is created by ANDing together the three **ΔF Latch 2** signals that control the W/M/N Switch. Only in a CW mode are all three of these signals HIGH simultaneously. The **L CW MODE** signal is applied to the A4 PCB."

PCO 2259
February 26, 1982

CHANGE #4

Model	Serial Nos.	Manual Print Date
Mainframe (D-8000)	104001 & up	January 1982

A. Remove pages 7-51 through 7-56 and replace them with the attached sheets, pages 7-51 through 7-56.

PCO 2321
1 March 1982

CHANGE #5

Serial Numbers Affected	Manual Print Date
All	January 1982

A. On page 4-10, change step d.4. to read as follows:

"On spectrum analyzer, displayed signal moves less than ± 500 kHz

March 16, 1982

CHANGE #6

Serial Numbers Affected	Manual Print Date
All	January 1982

A. On pages 6-7, 6-8, and 6-9 (Tables 6-1, 6-2, and 6-3), make the following changes:

FROM

U5	256 x 4 PROM, 74S387	56-4
U6	256 x 4 PROM, 74S387	5604

TO

U5	256 x 4 PROM	Not Field Replaceable
U6	256 x 4 PROM	Not Field Replaceable

25 March 1982

7-9 A2 RAMP GENERATOR PCB

7-9.1 A2 Ramp Generator PCB Circuit Description

The A2 Ramp Generator PCB generates one of the voltage tuning signals used to produce the sweep generator's sweep-frequency output. The PCB also generates the **RETRACE BLANKING** (+), (-), **BANDSWITCH BLANKING** (+), (-), and **SEQ SYNC** signals that are output to the respective rear panel connectors. A functional block diagram of this PCB is shown in Figure 7-28; the schematic diagram (3 sheets) is shown in Figure 7-29. The A2 PCB consists of three functional blocks (Figure 7-28), which are described below.

a. Ramp Generator. This functional block produces the PCB sweep ramp output signal and the two retrace blanking pulses that are supplied to the RETRACE BLANKING (+) and (-) rear panel connectors. The block also provides control for the relay connected to the rear panel PENLIFT OUTPUT connector. The input to this functional block is the front panel SWEEP TIME control group from the A12 Microprocessor PCB. Eight bits of this nine-bit group are latched into the digital-to-analog converter (DAC) circuit (U15) when the microprocessor clocks **SP13** HIGH. The DAC output is a negative voltage that causes the Sweep Ramp Integrator (U20B) to integrate in the positive direction. When the sweep ramp reaches 10 volts, the 10V Compare circuit (U25B, U25C) causes the Sweep Direction and Dwell Gating circuit (U24A, U24B, U2A, U2B, U17C) to open Switch A and close Switch B. This switching action causes the integrator to then integrate in the negative direction (retrace). When this negative-going ramp reaches 0 volts, the 0V Compare circuit (U25D, U25A) then causes Switch B to open and Switch A to close. A switch arrangement that reconfigures the integrator to again integrate in the positive direction. A typical sweep ramp waveform is shown in Figure 7-27.

The **1 SECOND CONTROL** bit (the ninth bit in the SWEEP TIME group) is a >1-or a <1-second flag bit. For sweep speeds between 1 and 99 seconds, this bit is HIGH. This HIGH causes the Sweep Ramp Integrator to integrate at the slower sweep-time rate.

The Retrace Blanking Logic circuit (Q2, U10C) causes both a plus (+) and a minus (-) 5 volt pulse to be generated during sweep retrace. The same signal that opens Switch A initiates these retrace blanking pulses.

The **H SWP** bit goes TRUE (high) to indicate when a forward sweep is in progress. This bit is supplied to the A12 Microprocessor, where it causes the front panel SWEEPING indicator to light.

The Activate Relay Logic circuit (Q3) controls relay A14K1, which is the relay that connects to the rear panel PENLIFT OUTPUT connector. This circuit has two purposes. First it activates A14K1, thus causing the XY recorder's pen to drop, when (1) the sweep generator is in the EXT OR SINGLE SWEEP mode, (2) sweep speed is greater than 1 second, and (3) a forward sweep occurs (**H SWP** line goes TRUE). Second it deactivates A14K1, thus causing penlift to occur, when the single-sweep ramp is interrupted and reset. To accomplish the first purpose, the circuit holds the relay deactivated (NO contacts open and NC contacts closed) when any of the following occur:

1. The **1 SECOND CONTROL** bit is LOW (sweep speeds between 10 ms and 1 s).

2. The **H SWP** bit is false (forward sweep not in progress).

3. The **H RESET** bit is TRUE (single-sweep is reset, subparagraph c below).

4. THE TRIGGER **EXT OR SINGLE SWEEP** control-word bit is not HIGH (subparagraph c below).

To accomplish the second purpose, a flip-flop circuit (U27A, U26A, U26B) deactivates the relay when reset occurs while a forward sweep is in progress (**L 10V COMPARE** line is FALSE).

b. Sweep Dwell and Related Circuits. The sweep dwell circuit causes the sweep ramp to dwell when:

1. The end of an oscillator band (ECB) is reached (bandswitch point).
2. An intensity marker command is received.
3. The top of the sweep ramp (10V) is reached.
4. The bottom of the sweep ramp (0V) is reached.

When any one of the above dwell conditions is detected, the Initiate Dwell circuit (U16B, U17A, U22A, U22B, U23A) sets the **H DWELL** line TRUE. When TRUE, **H DWELL** causes the following:

a. the Sweep Direction and Dwell Gating circuit (U24A, U24B, U2A, U2B, U17C, U10E) to open Switch A and Switch B. Opening these switches causes voltage integration of the sweep ramp to halt;

b. The 4 kHz clock in the Dwell Timing circuit (U3) to run at 144 kHz; thereby initiating a timing sequence.

The timing sequence initiated by the speeded-up clock consists of two timing pulses: **TP2** and **TP4.** The first occurring pulse, **TP2,** loads the dwell word

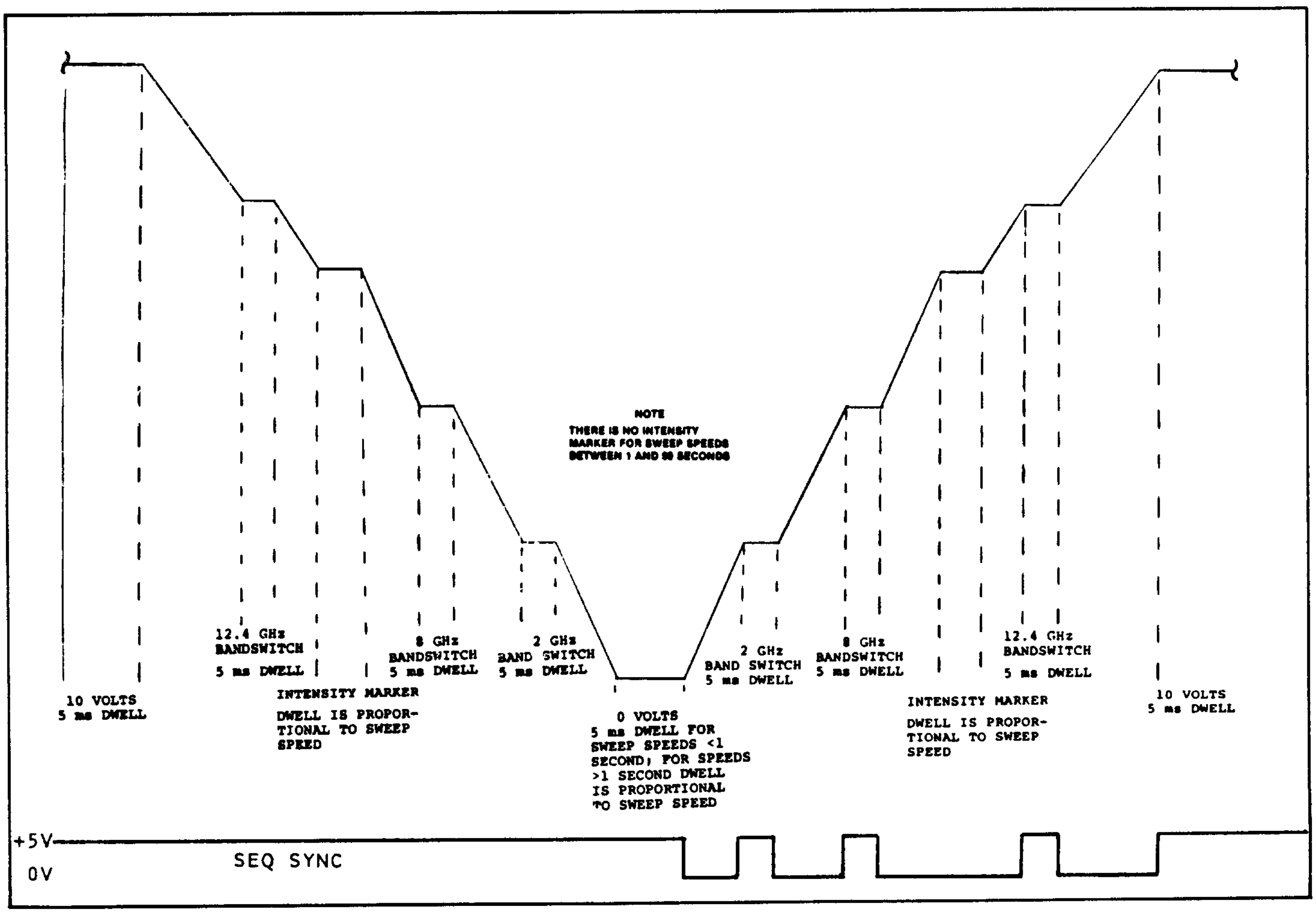


Figure 7-27. A2 PCB Sweep Ramp and Sequential Sync Pulse

(described below) into the Down Counter (U9, U13). And the second occurring pulse, **TP4**, both resets the clock to 4 kHz and enables the Down Counter. When enabled, the Down Counter sequentially counts down each time it is clocked. When a zero count is reached, the **U11 CLOCK** line is gated HIGH, which clocks the **L STRB** output from the Ext Sweep Logic circuit (U11A) TRUE (low). This **L STRB** output is applied to the Sweep Trigger Control Decoder circuit (U19) (subparagraph c below).

The dwell word that **TP2** loads into the Down Counter is either of two values, as determined by the Sel Logic circuit (U26C, U26D). If either the sweep ramp is at 0V and the sweep time is greater than 1 second or an intensity marker has been commanded, the dwell word's value represents the sweep time. Otherwise, the dwell word's value is 5 ms.

The related circuits in this block are the Level Dip circuit (U1A), the Seq Sync Logic (U23B, U5D, Q4) and the Bandswitch Blanking (Q5, Q6) circuits. The Level Dip circuit outputs a LOW when clocked by a **EOB** pulse. This LOW causes the A4 PCB to "dip" the RF output power during oscillator bandswitch.

The Seq Sync Logic circuit outputs a +5V pulse (Figure 7-27) during an oscillator bandswitch, 0-and 10-volt dwell periods, and sweep ramp retrace. This pulse goes to the A1 PCB (**H SEQ**) and to the rear panel SEQ SYNC connector.

The Retrace Blanking circuit outputs plus and minus (+, -) 5V pulses during sweep ramp retrace. These pulses go to the respective rear panel connectors.

c. Sweep Trigger Control. This functional block controls the recurrence of the A2 PCB sweep ramp. The input to this block is an 8-bit control group from the A12 Microprocessor PCB. This word is latched into the Control Word Latch and Logic circuit (U14, U2C, U5F) when the microprocessor clocks **SP14** HIGH. Of these eight bits, five comprise the TRIGGER group (AUTO, LINE, or EXT OR SINGLE SWEEP), one is the **1 SECOND CONTROL** bit (subparagraph b above), one is the **SEQ SYNC DISABLE** bit, and one is the **EXT FM DISABLE** bit. The **EXT FM DISABLE** bit is not used on this PCB; it is decoded here and sent to the A10 PCB. The **SEQ SYNC DISABLE** bit is used to activate the Seq Sync Disable Logic circuit (Q7). Three bits of the 5-bit control group go to the Decoder (U19), where they are used to control the trigger source. These 3 control-group bits are decoded by U19 when the **L STRB** line goes TRUE (low) (subparagraph b above). Once enabled by the **L STRB** line, U19 is controlled by the **H RAMP IS TEN** line. When TRUE, this line signals that the sweep ramp has reached its top end (10 volts). A chart showing the logic state of the **RAMP NOT DWELL** line for the various input signal logic states is given in Table 7-12.

The remaining signal in this block is **H RESET.** This signal line pulses TRUE when the EXT OR SINGLE SWEEP pushbutton is pressed while a sweep is in progress. When TRUE, **H RESET** initiates a dwell and, when the dwell period is finished, causes Switch A to close. When Switch A closes, the sweep ramp starts climbing toward 10 volts at a fast rate. When the ramp reaches 10 volts, the **L RAMP IS TEN** line enables a new sweep to be initiated when the EXT OR SINGLE SWEEP pushbutton is again pressed.

Table 7-12. L RAMP NOT DWELL Logic States

STROBE U19-7	RAMP IS TEN U19-9	AUTO U19-15	LINE U19-10	EXT OR SINGLE SWEEP U19-A	RAMP NOT DWELL U19-6
1	X*	X	X	X	1
0	0	X	X	X	0
0	1	1	0	0	0
0	1	X	1	0	0 Only when triggered by Line Trigger Pulse Generator. (U19-13 = 1)
0	1	X	0	1	0 Only when Single Sweep Logic circuit (U17D) has detected one of the following: a. An external trigger pulse from the rear panel. (U17D-12 = 0) b. An activate single-sweep logic level from the front panel, via the microprocessor. (U17D-13 = 0)

* = Don't Care

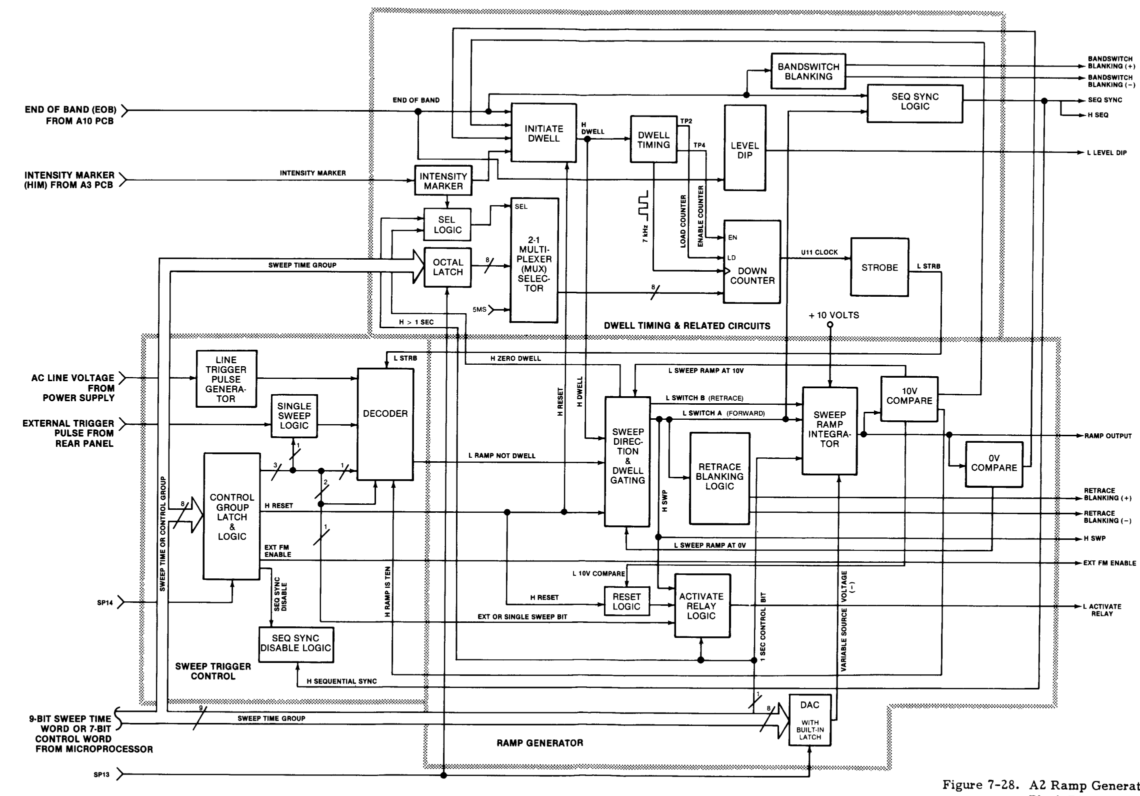


Figure 7-28. A2 Ramp Generator Functional Block Diagram

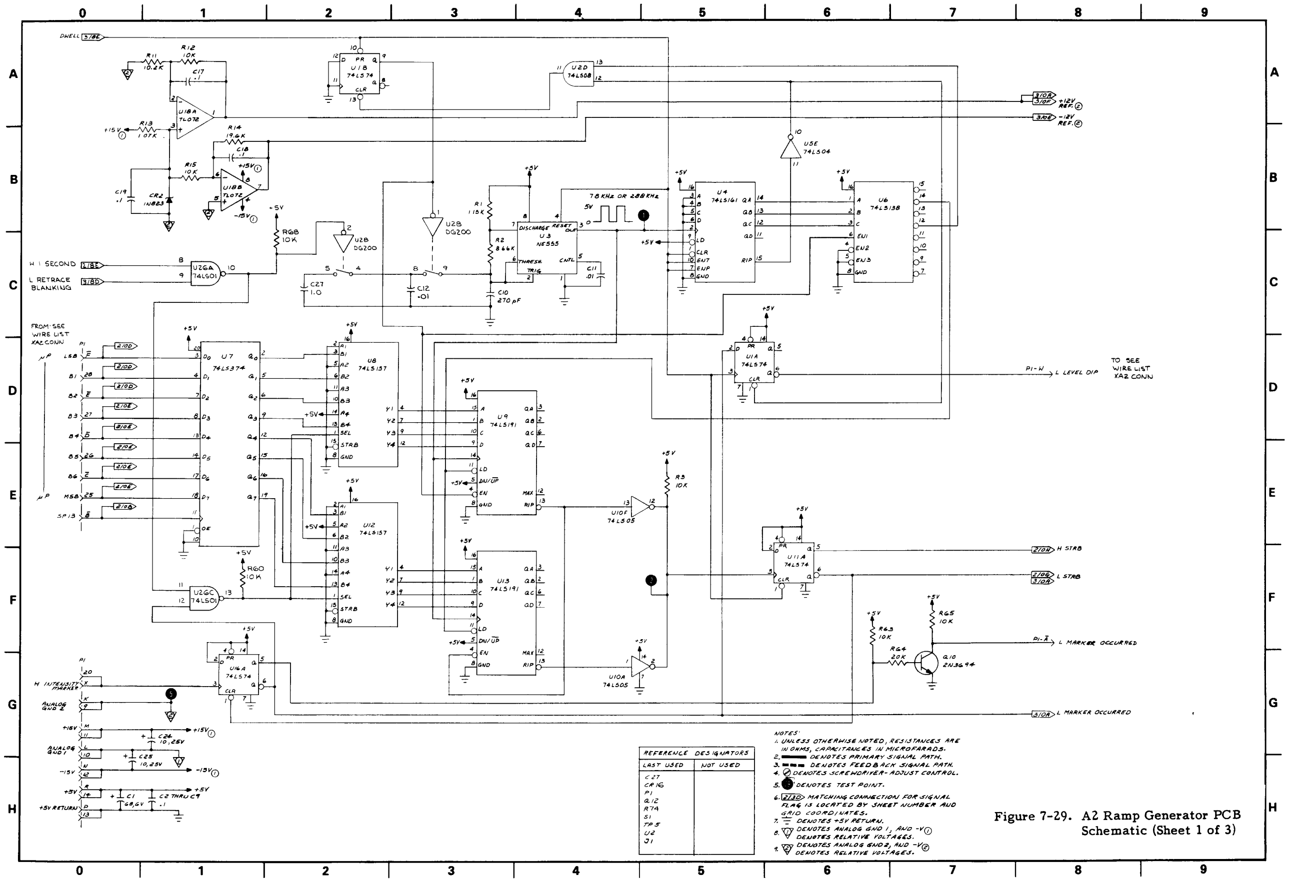


Figure 7-29. A2 Ramp Generator PCB Schematic (Sheet 1 of 3)

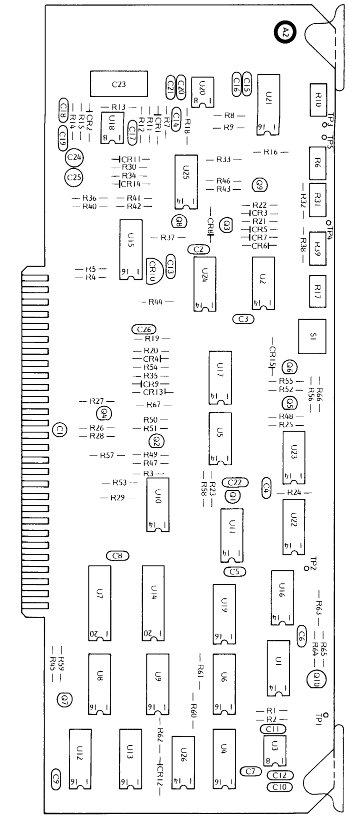


Figure 7-29. (Sheet 1)

A2 PCB Parts Locator

CHANGE #7

Model	Serial Nos. Affected	Manual Issue and Print Date
Mainframe (D-8000)	101001 thru 207099	1-6637/6647-OMM - Aug. 1981 2-6637/6647-OMM - Jan. 1982

A. On pages 3-21 and 3-22, Table 3-6, make the following changes:

1. Delete the words "and -POWER METER Controls" from the table title.

2. Delete steps 9 and 10.

B. Insert the following new figure and table after Table 3-6:

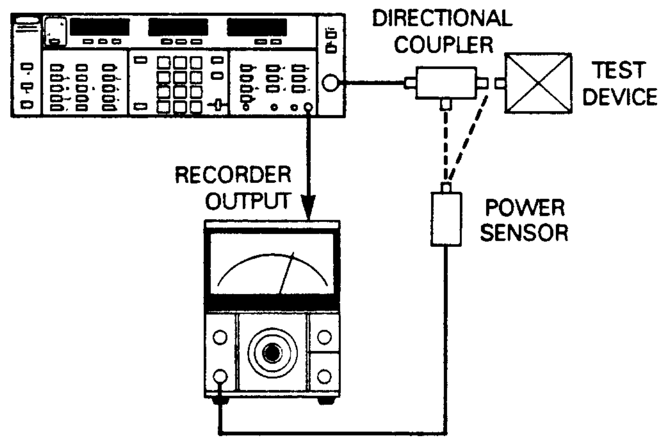


Figure 3-23A. Test Setup for Power Meter Leveling

Table 3-6A. Procedure for External Power Meter Leveling

1. Connect power sensor to the uncoupled port of the directional coupler, as shown in Figure 3-23A.
2. Turn on power on sweep generator (sweeper) and power meter.
3. On sweeper:
a. Press CW F1 and set frequency for the middle of the band of interest. That is, set to 1 GHz for the .01-2 GHz band, 5 GHz for the 2-8 GHz band, 10 GHz for the 8-12.4 GHz band, etc.
b. Press LEVELING-INTERNAL.
c. Press LEVEL and set output power for the desired power meter reading. This reading may be different from that indicated on the front panel, depending on the losses in the transmission system.
4. Disconnect power sensor from the uncoupled port and connect to the coupled port of the directional coupler.

CHANGE #7 (Continued)

5. Observe that the power meter indicates the step 3.c. reading, minus the coupling factor of the directional coupler (10 dB, 20 dB, etc.)

6. On sweeper:

   a. Press LEVELING-POWER METER.

   b. Adjust EXT ALC GAIN (do not push in) until the power meter indicates the same as reading in step 5, above.

NOTE

Do not readjust the EXT ALC GAIN control. The ALC loop is now calibrated for power meter leveling.

April 9, 1982

CHANGE #8

Models	Serial Numbers	Manual Affected	Print Date
All	All	2-6637/6647-OMM	Jan. 1982

A. On page 5-6, replace Table 5-2 (Power Supply Regulation and Ripple Specifications) with the new table shown below.

Table 5-2. Power Supply Regulation and Ripple Specifications

VOLTAGE SUPPLY	MONITOR POINT	REF. POINT	REGULATION TOLERANCE, 100% LOAD	REGULATION TOLERANCE, 10% LOAD	RIPPLE TOLERANCE, 100% LOAD (pk-pk)	RIPPLE TOLERANCE, 10% LOAD (pk-pk)
+5V	A14TP3 (P3-13)	A14TP4 (P13-26)	±3mV	±200mV	±50mV	±50mV
+15V LC	XA6-8	XA6-20	±300mV	±300mV	±10mV	±10mV
-15V LC	XA6-9	XA6-20	±300mV	±300mV	±10mV	±10mV
+15V HC	XA10-24	XA10-25	±300mV	±300mV	±10mV	±10mV
-15V HC	XA10-23	XA10-25	±300mV	±300mV	±10mV	±10mV
+24V	A14P12-2	XA6-10	±300mV	±300mV	±10mV	±10mV
-38V	A14P20-1	XA6-10	±300mV	±300mV	±10mV	±10mV

B. On page 5-6, paragraph 5-5b.7, change the last line to read

"(+0, -1.0mV)."

April 12, 1982

CHANGE #9

Models	Serial Numbers	Manual	Print Date
All	All	2-6637/6647-OMM	Jan. 1982

A new procedure eliminating the A2 Test Fixture has been developed for adjusting the voltage of the A2 sweep ramp. Eliminating the A2 Test Fixture necessitates the following manual changes:

A. Beginning on page 5-6, make the following changes to paragraph 5-5.

1. In the seventh line from the top left column, starting with the sentence "The voltage tolerance of ...," delete the remainder of the paragraph.

2. Replace steps 1-10 of subparagraph b. with steps 1-12 below:

"b. Ramp Voltage Adjustment

1. Press RESET on sweeper.

2. On oscilloscope, set the horizontal time base for External, and adjust its Vernier control so that the trace extends the full width of the screen (10 divisions).

3. On sweeper, press SWEEP TIME and set for 99 seconds.

4. Connect the DMM common lead to A2TP5; connect the "hot" lead to A2TP6 (A2U25, pin 7 for models without the test point).

5. While the ramp is sweeping in the forward direction, adjust A2R31 for +10V ± 1mV.

6. Move the DMM hot lead to A2TP7 (U25, pin 11).

7. After the ramp has swept thru its first 10 seconds (1 division), adjust A2R39 for 0V ± 1mV.

8. Disconnect the DMM leads from A2 and move them to the rear panel HORIZ OUTPUT connector (hot lead to the center conductor, and common lead to the shield).

9. Ground the center conductor on the rear panel EXT SWEEP connector.

10. Press SHIFT and EXTERNAL SWEEP (place the A2 PCB INT-EXT switch in EXT, for sweepers without the SHIFT functions).

11. Adjust A5R62 (Figure 5-7) for 0V ± 1mV.

12. Return the sweeper to AUTO sweep (INT-EXT switch back to INT) and remove the ground from the EXT SWEEP connector.

NOTE

The adjustment of A5R62 affects marker calibration. Consequently, perform or recheck marker calibration (paragraph 5-7) following the adjustment of A5R62."

CHANGE #9 (Continued)

3. Delete Table 5-3.

4. Replace the existing Figure 5-5 with the new Figure 5-5 below.

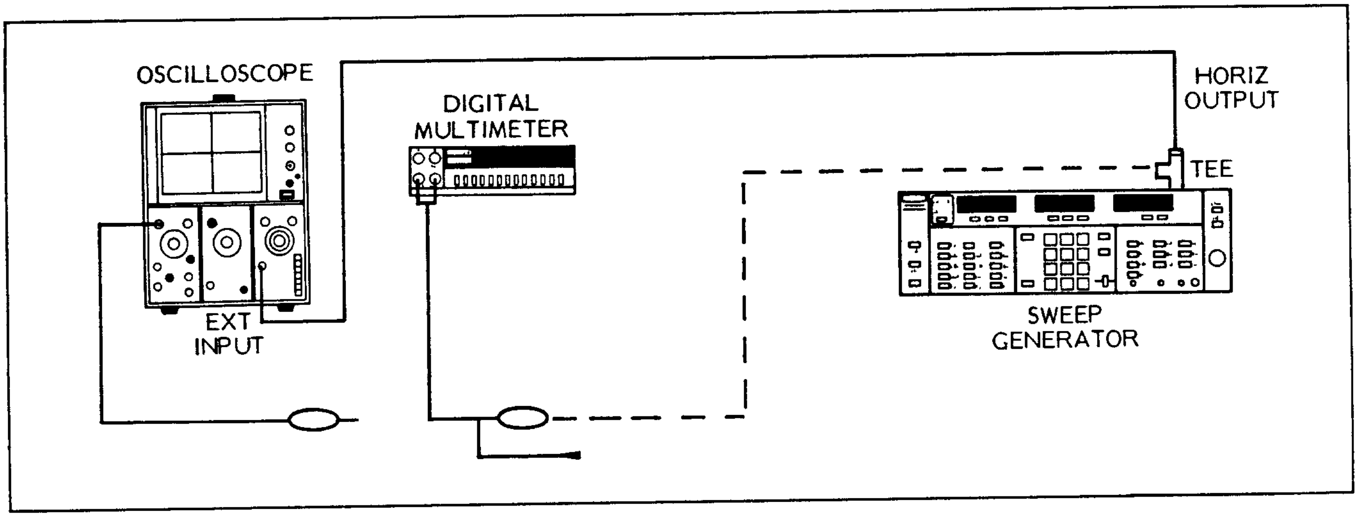


Figure 5-5. Test Equipment Setup for A2 Ramp Generator Adjustments

5. Delete Figure 5-6.

B. Beginning on page 5-12, make the following changes to paragraph 5-7:

1. Replace Figure 5-11 with the new figure below.

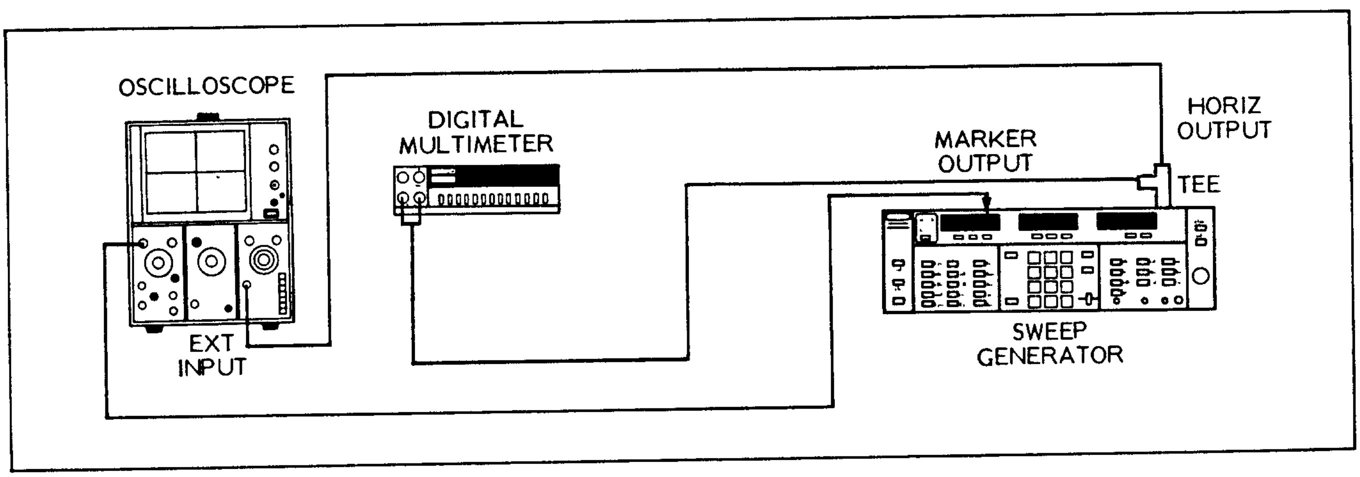


Figure 5-11. Test Equipment Setup for A3 Marker Generator Adjustments

CHANGE #9 (Continued)

2. Replace steps 2 thru 7 in subparagraph b. with the following:

   "2. Connect DMM "hot" lead to the center conductor of the rear panel HORIZ OUTPUT connector; connect the common lead to the shield.

   3. Ground the center conductor on the rear panel EXT SWEEP connector.

   4. Press SHIFT and EXTERNAL SWEEP (place the A2 PCB INT-EXT switch in EXT, for sweepers without the SHIFT functions).

   5. Adjust A5R62 (Figure 5-12) for 0V ± 1mV.

   6. Return the sweeper to AUTO sweep (INT-EXT switch back to INT) and remove the ground from the EXT SWEEP connector.

   7. Disconnect the DMM from the HORIZ OUTPUT connector."

3. In subparagraph c., delete steps 4.(c) and (d).

April 12, 1982

CHANGE #10

Serial Numbers Affected	Manual Print Date
All	January 1982

A. On page 6-21, Table 6-10, make the following addition:

CR12	Bridge Rectifier	60-13

24 May 1982

CHANGE #11

Serial Numbers Affected	Manual Print Date
All	January 1982

A. On page 4-10, Figure 4-17, add the following statement below the callout "NOISE SIDEBAND."

"(On analyzer, select VIDEO FILTER .3, .1, or .03 as necessary to view noise sidebands.)"

August 3, 1982

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TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

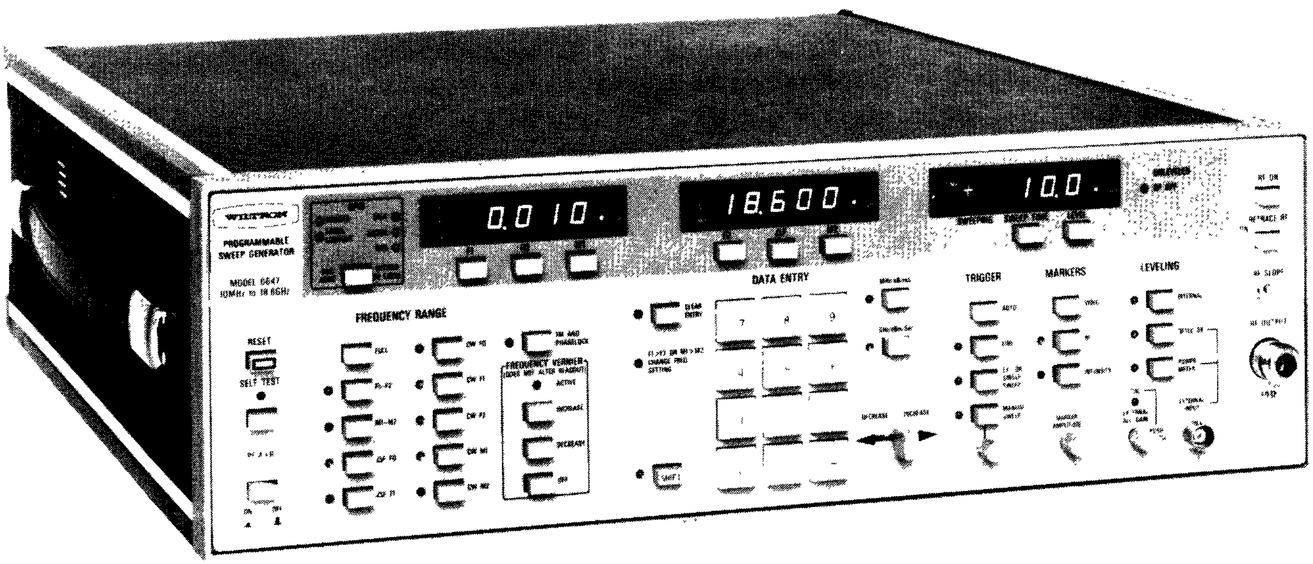


Figure 1-1. Model 6647 Programmable Sweep Generator

SECTION I

GENERAL INFORMATION

1-1 SCOPE OF THE MANUAL

This manual is the operation and maintenance (O&M) manual for the Model 6637, 6638, 6647, and 6648 Programmable Sweep Generators. The manual provides general information, plus installation and operation instructions. Refer to the Table of Contents for the manual organization.

1-2 INTRODUCTION

Section I provides a description, specifications, and option information for the programmable sweep generators.

1-3 DESCRIPTION AND SPECIFICATIONS

1-3.1 6600 Series Programmable Sweep Generators

The 6600 Series Programmable Sweep Generators are a family of GPIB-capable signal sources that generate sweep and CW frequencies from 10 MHz to 40 GHz. A representative list of available model numbers, with the frequencies they cover, is given below. This list will expand as additional frequency ranges are added to the 6600 Series family.

Model	Frequency Range
6609	10 to 2000 MHz
6617	10 MHz to 8 GHz
6637	2 to 18.6 GHz
6638	2 to 20 GHz
6647	10 MHz to 18.6 GHz
6648	10 MHz to 20 GHz
6636	18 to 26.5 GHz
6640	26.5 to 40 GHz

1-3.2 Model 6637, 6638, 6647, and 6648 Programmable Sweep Generators

The Model 6637, 6638, 6647, and 6648 Programmable Sweep Generators are microprocessor-based, pushbutton-controlled, broadband (see above), programmable sweep or fixed-frequency sources. When configured with the GPIB interface option (Option 3), any sweeper model is capable of being fully programmed via the IEEE 488 Interface Bus (GPIB). Specifications for the sweep generators are given in Table 1-1.

1-4 OPTIONS

The following options are available for the Model 6637, 6638, 6647, and 6648 Programmable Sweep Generators.

- **Option 1, Rack Mount.** Sweep generator comes equipped with both mounting ears and chassis track slides that have a 90° tilt capability.
- **Option 2, 10 dB Step Attenuator.** Sweep generator comes supplied with a front panel or GPIB-programmable 10 dB step attenuator. Step attenuator has a 70 dB range.
- **Option 3, GPIB Interface.** Sweep generator is equipped to operate on the IEEE 488 (IEC 625) Interface Bus. With Option 3 installed, all front panel pushbuttons except POWER are bus-programmable. Option 3 may be installed in the field.
- **Option 9, Main RF Connector on Rear Panel.** Sweep generator comes supplied with an SMA female connector installed on the rear panel rather than on the front panel.
- **Option 10, Auxiliary RF Output Connector (Rear Panel).** Sweep generator comes

equipped with a second RF connector (SMA female) installed on the rear panel. Its output power level is approximately 25 dB below the main connector power level, and its Maximum Leveled Power specification is derated by 1.5 dB.

Table 1-1. Specifications

SPECIFICATION	MODELS 6637/6638	MODELS 6647/6648
FREQUENCY CHARACTERISTICS		
RANGE:	6637: 2 to 18.6 GHz 6638: 2 to 20 GHz	6647: .01 to 18.6 GHz 6648: .01 to 20 GHz
ACCURACY (at 25°C)		
CW Mode:	±10 MHz	±10 MHz
Sweep Mode (≤50 MHz sweep width):	±15 MHz	±15 MHz
STABILITY, with		
Temperature (Typical):	±500 kHz/°C	±1 MHz/°C, below 2 GHz ±500 kHz/°C, above 2 GHz
10% Line Voltage Change:	±100 kHz	±100 kHz
10 dB Power Level Change:	±500 kHz	±500 kHz
3:1 Load SWR:	±300 kHz	±300 kHz
Time (10 minutes, typical):	±200 kHz	±200 kHz
RESIDUAL FM (30 Hz to 15 kHz bandwidth, peak)		
CW Mode and Swept Mode (≤50 MHz sweep width):	7 kHz pk, below 8 GHz; 10 kHz pk, above 8 GHz	7 kHz pk, below 8 GHz; 10 kHz pk, above 8 GHz
OUTPUT CHARACTERISTICS		
MAXIMUM LEVELED POWER (25° ±5°C):	6637: >10mW (+10 dBm) 6638: >10mW at ≤18.5 GHz >5mW at >18.5 GHz	6647: >10mW (+10 dBm) 6648: >10mW at ≤18.5 GHz >5mW at >18.5 GHz
With Option 2:	6637: >6.6mW (+8.2 dBm) 6638: >6.6mW at ≤18.5 GHz >3.3mW at >18.5 GHz	6647: >6.6mW (+8.2 dBm) 6648: >6.6mW at ≤18.5 GHz >3.3mW at >18.5GHz

Table 1-1. Specifications (continued)

SPECIFICATION	MODELS 6637/6638	MODELS 6647/6648
POWER LEVEL ACCURACY, INTERNALLY LEVELED:	±1 dB	±1 dB
With Option 2 (at 0 dBm):	±1.5 dB	±1.5 dB
With Option 10:	±1.5 dB	±1.5 dB
CALIBRATED RANGE:	12 dB	12 dB
With Option 2:	82 dB	82 dB
ATTENUATOR ACCURACY, per step (Option 2):	±0.4 dB/10 dB step	±0.4 dB/10 dB step
POWER VARIATION		
With Frequency, Internally Leveled:	±0.5 dB*	±0.6 dB*
With Temperature:	±0.05 dB/°C	±0.05 dB/°C
SPECTRAL PURITY		
Harmonics:	>40 dBc	>20 dBc, 10-30 MHz; >30 dBc, 30 MHz-2 GHz; >40 dBc, above 2 GHz
Spurious:	>60 dBc	>35 dBc, below 2 GHz; >60 dBc, above 2 GHz
OUTPUT SWR (50 ohms):	1.2, below 8 GHz; 1.4, above 8 GHz	1.4, below 2 GHz; 1.4, above 8 GHz; 1.2, between 2 and 8 GHz
With Option 2:	2.0	2.0
With Option 9:	1.6	1.6
RESIDUAL AM (50 kHz Bandwidth):	>50 dBc	>50 dBc
OUTPUT CONNECTOR		
Front:	Type N, Female	Type N, Female
Option 9 (rear):	Type N, Female	Type N, Female
AUXILIARY OUTPUT CONNECTOR		
Option 10, (rear):	SMA, Female	SMA, Female

*±1 dB with Option 2 or 9

Table 1-1. Specifications (continued)

SPECIFICATION	MODELS 6637/6638	MODELS 6647/6648
MODULATION CHARACTERISTICS		
EXTERNAL AM		
Sensitivity, Typical:	1 dB per volt	1 dB per volt
Frequency Response, Typical:	dc to 50 kHz	dc to 50 kHz
Input Impedance:	10kΩ	10kΩ
Amplitude Control Range:	>13 dB	>13 dB
Maximum Input:	20 volts	20 volts
EXTERNAL FM		
Sensitivity:	-6 MHz per volt	-6 MHz per volt
Maximum Deviations at Modulation Frequencies of:		
dc to 100 kHz:	±25 MHz	±25 MHz
100 to 250 kHz:	±5 MHz	±5 MHz
Input Impedance:	10kΩ	10kΩ
Maximum Input:	20 volts	20 volts

GENERAL CHARACTERISTICS - 6600 SERIES SWEEP GENERATORS

SWEEP TIME: Continuously adjustable from .01 to 99 seconds, displayed on front panel LED readout.

SWEEP MODES:

Full Sweep: Sweeps full band in one continuous frequency sweep. The high- and low-end frequency points are displayed on the front panel.

F1 to F2 Sweep: Sweeps between user-selected frequencies (F1 and F2), which are displayed on the front panel.

M1 to M2 Sweep: Sweeps between user-selected frequencies (M1 and M2), which are displayed on the front panel.

ΔF F0 Sweep: Sweeps symmetrically about a center frequency (F0) that is user-selected. F0 frequency and sweep width frequency range are simultaneously displayed on the front panel.

ΔF F1 Sweep: Sweeps symmetrically about a center frequency (F1) that is user-selected. F1 frequency and sweep-width frequency range are simultaneously displayed on the front panel.

CONTINUOUS WAVE (CW) MODES:

CW F0, **CW F1**, **CW F2**, **CW M1**, **CW M2**: Fixed frequency CW output at the respective F0, F1, F2, M1, or M2 frequency point. The frequency of the CW signal is displayed on a front-panel LED readout.

Table 1-1. Specifications (continued)

FINE-FREQUENCY CONTROL:

Frequency Vernier controls are available and may be used with a microwave counter to finely adjust (1) the output frequency in any CW mode or (2) the center frequency in either ΔF sweep mode. Frequency may be adjusted by up to ±12.7 MHz without changing the frequency appearing on the applicable LED readout.

TRIGGER MODES:

Automatic: Sweep recurs automatically.

Line: Sweep recurs in sync with the line frequency or in sync with multiples of the line frequency.

External or Single Sweep: Sweep recurs when triggered. Triggering can be accomplished either from the front panel or by applying an external pulse to the rear panel.

Manual: Frequency may be swept manually between upper and lower frequency limits using the front-panel MANUAL control.

MARKERS:

Video: Positive video pulse(s). Markers appear at frequencies M1, M2, and F0, depending upon sweep mode. In the FULL, F1-F2, and ΔF F1 modes, three markers are available. In the ΔF F0 mode, two markers (M1 and M2) are available. And, in the M1-M2 mode, one marker (F0) is available. The frequency and amplitude of the marker(s) may be controlled from the front panel.

RF: Negative RF pip(s). Markers appear at frequencies M1, M2, and F0, as described for Video above. The frequency and amplitude of the marker(s) may be controlled from the front panel.

Intensity: Intensity dot(s) that are created when the sweep is made to dwell momentarily at the marker frequency(ies). No connection between the sweep generator and the CRT Z-axis is required. Markers appear at frequencies M1, M2, and F0, as described for Video above. The frequency of the marker(s) may be selected from the front panel.

LEVELING MODES:

Internal: The output power is sampled internally and used to provide leveled RF power at the RF OUTPUT connector.

Detector: The output power may be sampled externally using a coupler and detector, and used to provide leveled RF power at the device under test.

Power Meter: The output power may be sampled externally using a coupler and a power meter, and used to provide leveled RF power at the device under test.

EXTERNAL LEVELING CONTROL (ALC):

The gain of the external leveling input (detector or power meter) may be calibrated from the front panel; the use of an external indicating device such as an oscilloscope is not necessary.

SELF TEST: Diagnostic self-test routines are accomplished each time the unit is turned on and when the front-panel SELF TEST pushbutton is pressed. In the event of a self-test failure, an error code is displayed on front-panel LED readouts. If the unit passes, the word PASS is indicated on an LED readout.

RESET: Sweep generator operation in either the local (front panel) or remote (GPIB) operational mode can be reset to a predetermined state by pressing the front panel RESET pushbutton.

GPIB OPERATION: All front-panel pushbuttons except POWER can be programmed over the IEEE 488 Interface Bus (GPIB). Front panel indicators light when:

Table 1-1. Specifications (continued)

1. The sweeper is under GPIB (remote) control.
2. Local Lockout is programmed.
3. A Service Request (SRQ) is initiated.
4. The sweeper is addressed to either Talk or Listen.

A chart showing GPIB subset capability is given in Figure 3-26.

INPUT/OUTPUT CONNECTORS:

Horizontal Output: 0 to 10 volts during all sweep and CW modes (if HORIZ OUTPUT DURING CW switch is ON). <100Ω impedance.

Seq Sync Output: Positive TTL-level pulse during oscillator bandswitching and sweep retrace.

Retrace Blanking (+) Output: +5 volt TTL-compatible pulse during retrace blanking.

Retrace Blanking (-) Output: -5 volt pulse during retrace blanking.

Marker Output: 0 to +5 volt pulse when video marker is selected. Pulse amplitude depends upon front panel MARKERS AMPLITUDE control. 1kΩ impedance.

Bandswitch Blanking Output: ±5 volts, depending upon BANDSWITCH BLANKING switch, during oscillator bandswitching. <100Ω impedance.

1V/GHz Output: 1 volt per GHz of output frequency. <100Ω impedance.

Penlift Output: Normally-open relay contacts for lifting recorder pen during retrace. Internal jumper available for normally-closed contacts.

Sweep Trigger Input: When TRIGGER–EXT OR SINGLE SWEEP pushbutton is engaged, an externally-applied clock pulse with the below listed characteristics triggers a sweep upon closure-to-ground.

Amplitude: 4 to 25Vpk
Pulse Width: >1μs
Fall Time: <5μs
Polarity: Low true

Sweep Dwell Input: +5V (maximum) TTL pulse causes frequency sweep to dwell. Provides interface for HP 8410 Network Analyzer.

External AM Input: 10 kΩ input impedance and 1V/dB input sensitivity.

External FM and Phase Lock Input: 10 kΩ input impedance and -6 MHz/V input sensitivity.

External Square Wave Input: TTL-compatible input that allows a ±10 volt (maximum) square wave to modulate the RF output signal. Input square wave frequency from dc to 50 kHz.

External Sweep Input: Allows a 0 to 10 volt external sweep ramp to be used to sweep the output frequency. 10kΩ impedance.

NONVOLATILE STORAGE: Front-panel control settings are retained in an internal memory (storage) when the ac power is turned off. When the ac power is turned on again, the previously-stored control settings are returned. The internal memory is powered by a rechargeable battery. Battery charge will last approximately 20 days when the sweeper is turned off and will be automatically recharged when the sweeper is turned on again.

INPUT POWER: 100, 115/120 Vac at 2.0A rms or 200, 230/240 Vac at 1.0A rms, 44-68 Hertz.

OPERATING TEMPERATURE RANGE: 0 to 50 degrees centigrade.

PHYSICAL:

Height: 13.34 cm (5.25 inches)
Width: 43.18 cm (17 inches)
Depth: 47.6 cm (18.75 inches)
Weight: 15.08 kg (33.5 pounds)

SECTION II

INSTALLATION

2-1 INTRODUCTION

This section provides information on initial inspection, preparation for use, and General Purpose Interface Bus (GPIB) interconnections. Also included is information concerning reshipment and storage of the sweep generator.

2-2 INITIAL INSPECTION

Inspect the shipping container for damage. If the container or cushioning material is damaged, retain until the contents of the shipment have been checked against the packing list and the instrument has been checked for mechanical and electrical operation.

If the sweep generator is damaged mechanically, notify your local sales representative or WILTRON Customer Service. If either the shipping container is damaged or the cushioning material shows signs of stress, notify the carrier as well as WILTRON. Keep the shipping materials for carrier's inspection.

2-3 PREPARATION FOR USE

Preparation for use consists of checking that the sweep generator is set for the correct line voltage. The line-voltage module on rear panel enables the sweep generator to be used with any of four international line voltages: 100, 115/120, 220, and 230/240. Before leaving the factory, each sweep generator is preset and tagged for the line voltage present in the customer's area. If the actual line voltage is different from that stated on the tag, the following procedure gives instructions for changing the line-voltage selector card.

a. Refer to Figure 2-1. Disconnect the power cord from the voltage selector module (1) and slide cover (2) down to gain access to the fuse compartment.

b. To select a different line voltage:

   1. Pull on FUSE PULL (3) and remove line fuse (4) and PC board (5) .

      NOTE

      The PC board is tightly secured within the module housing. It may be necessary to use needle-nose pliers or a similar tool as a pry.

   2. Using the example for 115/120 Vac operation (Figure 2-1) as a guide, reinstall the PC board. For the correct installation of this board, the desired line-voltage callout should be located:

      a. adjacent to the input receptacle and

      b. facing toward the BNC connector-bank.

   3. Push the FUSE PULL back to its normal position and insert a fuse of the proper value (as indicated on the right side of the module) into the fuse holder.

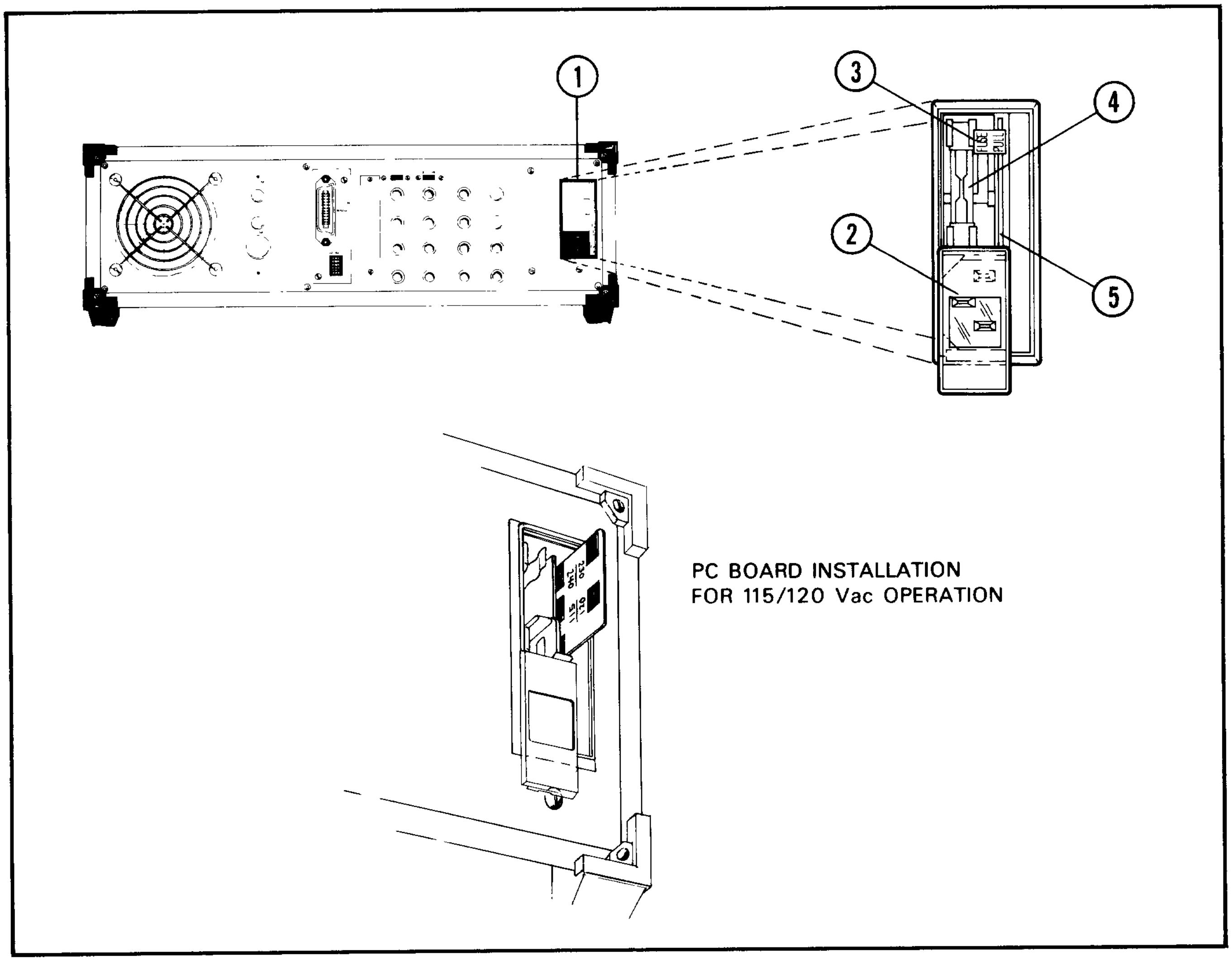


Figure 2-1. Line Voltage Selector Module

2-4 GPIB SETUP AND INTERCONNECTION

With Option 3 installed, the sweep generator is capable of providing automated microwave measurements via the GPIB. Specific GPIB information – including interface connections, cable requirements, and addressing instructions – is contained in the following paragraphs.

2-4.1 Interface Connector

Interface between the sweep generator and other devices on the GPIB is via a 24-wire interface cable. The interface cable is specifically constructed with each end containing a connector shell with two connector faces. These double-faced connectors allow for parallel connection of two or more cables to a single device. Figure 2-2 shows the pin assignments for the Type 57 GPIB connector, installed on the rear panel.

2-4.2 Cable Length Restrictions

The GPIB system can accommodate up to fifteen instruments at any one time. To achieve design performance on the bus, the proper timing and voltage level relationships must be maintained. If either the cable length between separate instruments or the accumulated cable length between all instruments is too long, the data and control lines

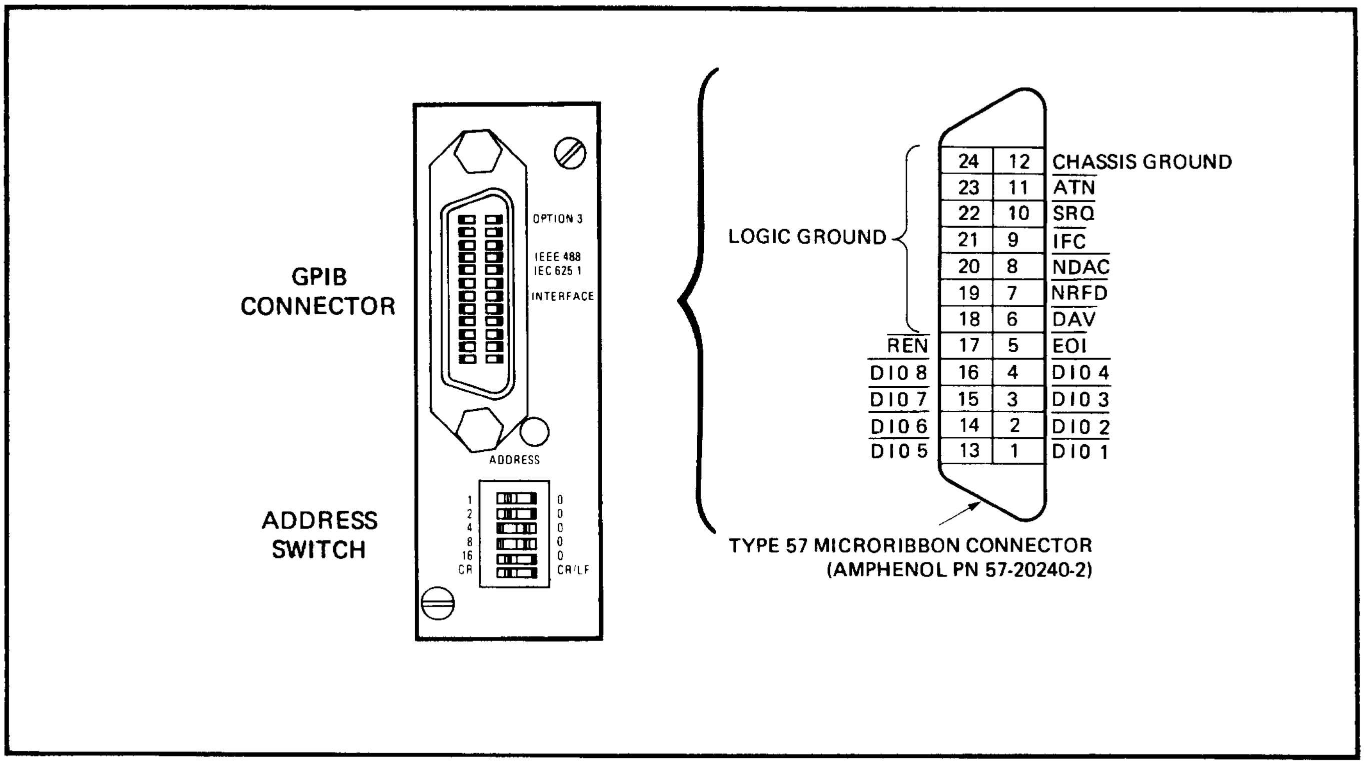


Figure 2-2. Option 3 Panel (Address Switch and GPIB Connector)

cannot be driven properly and the system may fail to perform. Cable length restrictions are as follows:

- No more than 15 instruments may be installed on the bus.
- Total accumulative cable length in meters may not exceed 2 times the number of bus instruments, or 20 meters – whichever is less.

2-4.3 GPIB Interconnection

The only interconnection required for GPIB operation is between the sweep generator and the controller. To accomplish this interconnection, a special cable is required. This cable – WILTRON Part No. 2000-1, -2, or -4 (1, 2, or 4 meters in length) – is available from the factory.

2-4.4 GPIB Address

The sweep generator is shipped from the factory preset to address 5. If a different address is desired, the ADDRESS switches on the Option 3 panel (Figure 2-2) provide for the selection of any address number between 0 and 30. Figure 2-3 provides a tabulation of the available address numbers, and Figure 2-4 provides an example of how an address number is selected.

2-4.5 Data Delimiting (CR–CR/LF Switch)

On the GPIB, data delimiting is accomplished using either the carriage return (CR) or both the carriage return and the line feed (CR/LF) ASCII characters, depending upon the requirements of the instrument used as system controller. For example, the PET 2001 requires CR. The HP 9825A requires CR/LF, while the WILTRON 85 and the Tektronix 4051 can use either CR or CR/LF.

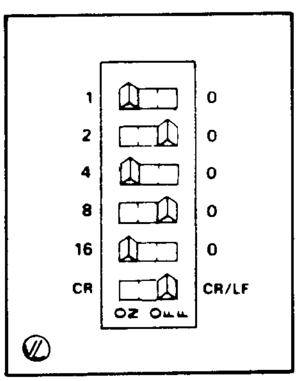
To provide ease in selecting the proper data-delimiting character for the controller in use, a switch is provided on the rear Option 3 panel. To use this switch, simply press the rocker arm to the position of the required delimiting character (Figure 2-4).

Decimal Address	ASCII Character	16 (MSB)	8	4	2	1 (LSB)
0	Space	0	0	0	0	0
1	!	0	0	0	0	1
2	"	0	0	0	1	0
3	#	0	0	0	1	1
4	$	0	0	1	0	0
5	%	0	0	1	0	1
6	&	0	0	1	1	0
7	'	0	0	1	1	1
8	(	0	1	0	0	0
9	)	0	1	0	0	1
10	*	0	1	0	1	0
11	+	0	1	0	1	1
12	,	0	1	1	0	0
13	-	0	1	1	0	1
14	.	0	1	1	1	0
15	/	0	1	1	1	1

Decimal Address	ASCII Character	16 (MSB)	8	4	2	1 (LSB)
16	0	1	0	0	0	0
17	1	1	0	0	0	1
18	2	1	0	0	1	0
19	3	1	0	0	1	1
20	4	1	0	1	0	0
21	5	1	0	1	0	1
22	6	1	0	1	1	0
23	7	1	0	1	1	1
24	8	1	1	0	0	0
25	9	1	1	0	0	1
26	:	1	1	0	1	0
27	;	1	1	0	1	1
28	<	1	1	1	0	0
29	=	1	1	1	0	1
30	>	1	1	1	1	0

Switch ON = 1
Switch OFF = 0

Figure 2-3. Available Address Codes and Corresponding Address Switch Positions



GPIB ADDRESS = 10 (2+8)

DATA DELIMITER = CR

Figure 2-4. Address Selection

2-5 PREPARATION FOR STORAGE AND/OR SHIPMENT

Instructions for preparing the sweep generator for storage, shipment, or both are provided in paragraphs 2-5.1 and 2-5.2.

2-5.1 Preparation for Storage

Preparation for storage involves cleaning the unit, packing the inside of the unit with moisture-absorbing dessicant crystals, and storing the unit in a temperature environment between -40 and +70 degrees centigrade.

2-5.2 Preparation for Shipment

To provide maximum protection against damage in transit, the sweep generator should be repackaged in the original shipping container. If this container is no longer available and the sweep generator is being returned to WILTRON for repair, contact

WILTRON Customer Service and a new shipping container will be sent to you free of charge. In the event neither of these two options is possible, the following paragraphs provide instructions for packaging and shipment.

a. Use a Suitable Container. Obtain a corrugated cardboard carton with a 275-pound test strength and inside dimensions of no less than six inches more than the instrument dimensions; this allows for cushioning.

b. Protect the Instrument. Surround the instrument with polyethylene sheeting to protect the finish.

c. Cushion the Instrument. Cushion the instrument on all sides by tightly packing dunnage or urethane foam between the carton and the instrument, allowing three inches on all sides.

d. Seal the Container. Seal the carton by using either shipping tape or an industrial stapler.

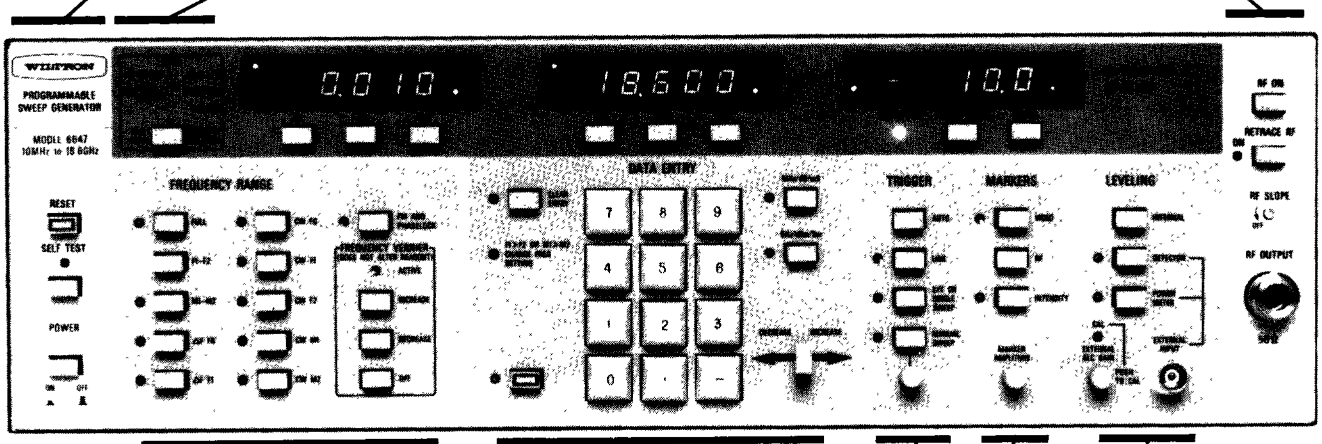
e. Address the Container. If the instrument is being returned to WILTRON for service, mark the WILTRON address and your return address on the carton in one or more prominent locations. The WILTRON address is:

WILTRON Company
ATTN: Customer Service
825 E. Middlefield Road
Mountain View, CA 94043

BUS ADRS/RETURN TO LOCAL Pushbutton and GPIB Indicators - Provide for the display of GPIB status and address information, plus, if the sweep generator is in the GPIB mode of operation, return to local (front panel) control. The pushbutton and indicators are described in paragraph 3-2.8.

POWER, SELF TEST, and RESET Pushbuttons - Provide for turning power on/off, performing self test, and resetting front-panel controls to a known state. Individual pushbuttons are described in paragraph 3-2.7.

RF OUTPUT Pushbutton, Indicators, and Connector - Provide for the output and control of the RF output function. Individual pushbuttons and indicators, along with the connector, are described in paragraph 3-2.5.



FREQUENCY RANGE Pushbuttons - Control the frequency sweep and CW output of the sweep generator. Individual pushbuttons are described in paragraph 3-2.2.

LEVELING Pushbuttons and Connector - Provide for RF output leveling. Individual pushbuttons, along with the connector, are described in paragraph 3-2.5.

MARKERS Pushbuttons - Provide for markers. Individual pushbuttons are described in paragraph 3-2.4.

DATA ENTRY and SHIFT Pushbuttons - The data entry controls provide for inputting frequency, sweep time, and output-power level information. The SHIFT pushbutton provides alternate functions for certain controls. Individual pushbuttons are described in paragraph 3-2.1.

TRIGGER Pushbuttons - Provide for sweep triggering. Individual pushbuttons are described in paragraph 3-2.3.

Figure 3-1. Sweep Generator Front Panel Controls

SECTION III

OPERATION

3-1 INTRODUCTION

This section contains information on the front and rear panel controls and connectors, plus a description of the sweep generator self-test feature. Also included are operational checkout procedures and a description of the Option 3 GPIB command codes.

3-2 FRONT PANEL CONTROLS

The front panel controls are grouped by function, as shown in Figure 3-1. Detailed descriptions of individual controls within each group are given in paragraphs 3-2.1 thru 3-2.8.

3-2.1 DATA ENTRY Pushbuttons

There are five discrete-frequency parameters (F0, F1, F2, M1, and M2) and one sweep width parameter (ΔF) – plus the sweep time and RF-output power level parameters – used to control the operation of the sweep generator. The DATA ENTRY pushbuttons (Figure 3-2) provide for entering new values for these parameters.

To provide an overview, several examples of how these pushbuttons are used to accomplish data entry are given in Figure 3-3. Individual DATA ENTRY pushbuttons are described in subparagraphs a through f.

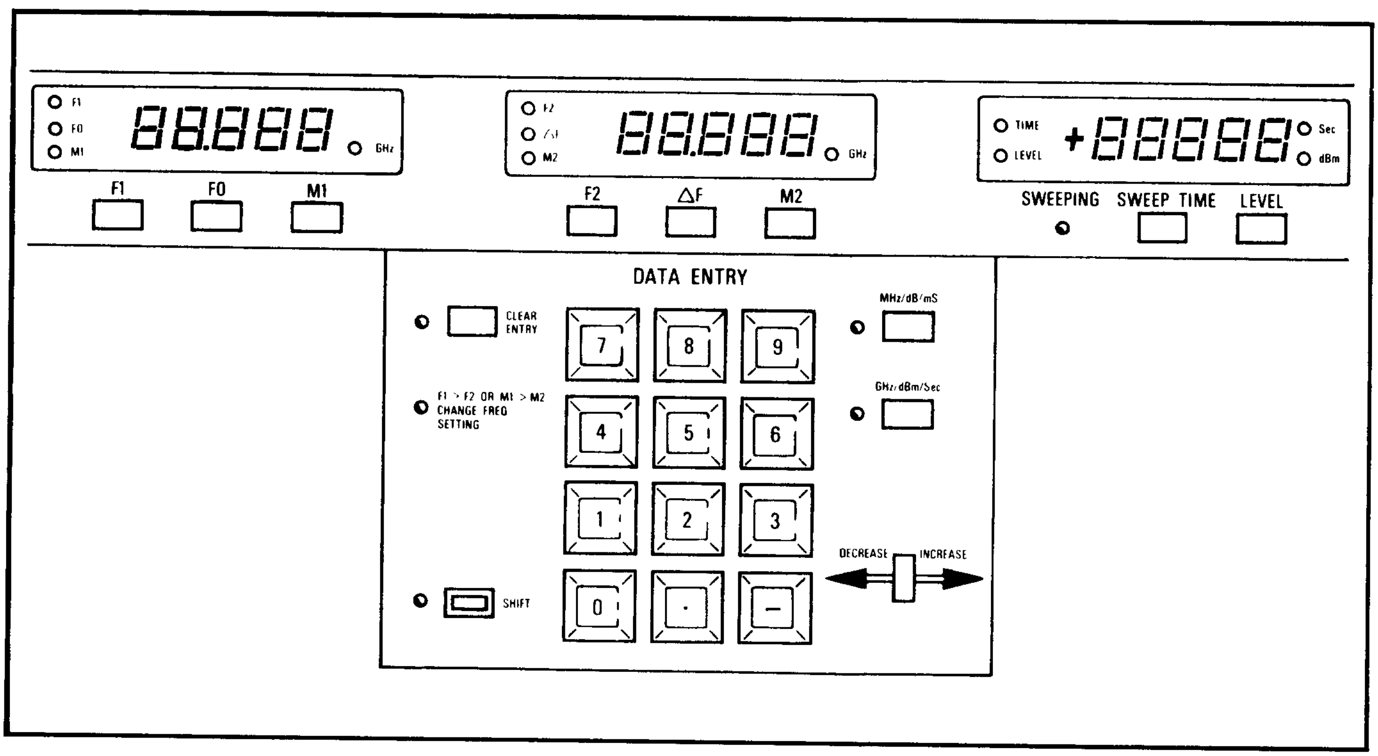


Figure 3-2. DATA ENTRY Pushbuttons

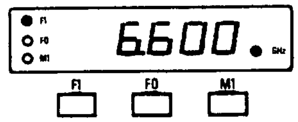
1. To enter a new F1 parameter of 6600 MHz, proceed as follows:

Press [F1] + [6] [6] [0] [0] + [MHz/dB/mS]

or

Press [F1] + [6] [.] [6] + [GHz/dBm/Sec]

The display above the F1 pushbutton will read:



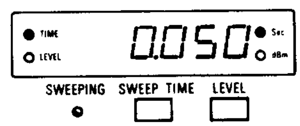
2. To enter a new SWEEP TIME parameter of 50 ms, proceed as follows:

Press [SWEEP TIME] + [5] [0] + [MHz/dB/mS]

or

Press [SWEEP TIME] + [.] [0] [5] [0] + [GHz/dBm/Sec]

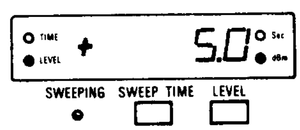
The display above the SWEEP TIME pushbutton will read:



3. To enter a new RF level parameter of 5 dBm, proceed as follows:

Press [LEVEL] + [5] + [GHz/dBm/Sec]

The display above the LEVEL pushbutton will read:

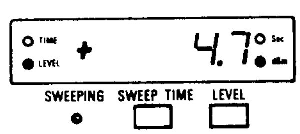


4. To change the RF power level, two methods are available: (1) a new power level may be selected using the example shown in 3, above, or (2) a value in dB may be added to or subtracted from the present power level; the algebraic sum or difference of this arithmetical process will appear on the display in dBm. Examples are shown in a and b, below.

   a. To subtract 0.3 dB from the power level selected in 3, above, proceed as follows:

   Press [LEVEL] + [−] [.] [3] + [MHz/dB/mS]

   The display above the LEVEL pushbutton will read:



   b. To add 2 dB to the power level selected in 4a, above, proceed as follows:

   Press [LEVEL] + [2] + [MHz/dB/mS]

   The display above the LEVEL pushbutton will read:

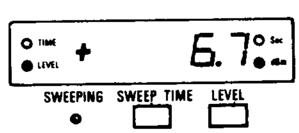


Figure 3-3. How to Enter Parameter Data

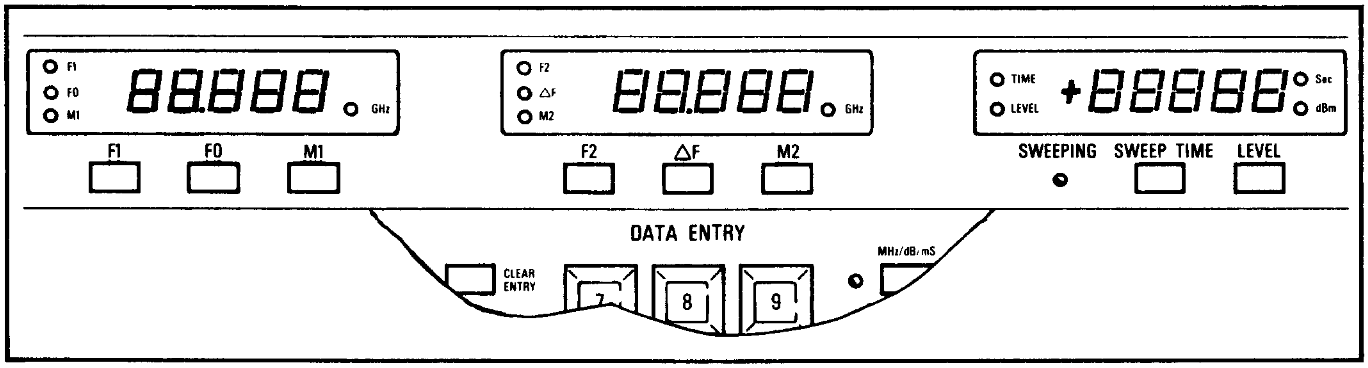


Figure 3-4. F1, F0, M1, F2, ΔF, M2, SWEEP TIME and LEVEL Pushbuttons and SWEEPING Indicator

a. F1, F0, M1, F2, ΔF, M2, SWEEP TIME, and LEVEL Pushbuttons and SWEEPING Indicator (Figure 3-4).

1. The pushbuttons enable the selected parameter's value to be changed via the DATA ENTRY keypad or the INCREASE/DECREASE lever, or to be monitored via the appropriate LED readout. The parameter that is selected for either changing or monitoring is hereafter known as the **selected parameter.**

2. The SWEEPING Indicator lights during the forward portion of the frequency sweep. The indicator is out during retrace.

b. DATA ENTRY Keypad (Figure 3-5). The DATA ENTRY keypad is used to change the value of the selected frequency, sweep time, or level parameter. When the selected parameter is frequency (F1, F0, M1, F2, ΔF, or M2), the new value may be entered in either MHz or GHz. When the selected parameter is sweep time, the new value may be entered in either seconds or milliseconds. And, when the selected parameter is power level, the new value may be entered in either dB or dBm.

c. INCREASE-DECREASE Lever (Figure 3-6). When enabled by a parameter pushbutton (F1, SWEEP TIME, LEVEL, etc.), this lever may be used to increase or decrease the parameter's value. The length of lever travel, either right or left, determines the rate at which the parameter's value increases or decreases. To increase or decrease the parameter's value in one increment steps, "tap" the switch in the direction of desired change. When the lever is "tapped," a frequency parameter will change in 1 MHz increments. An RF level parameter will

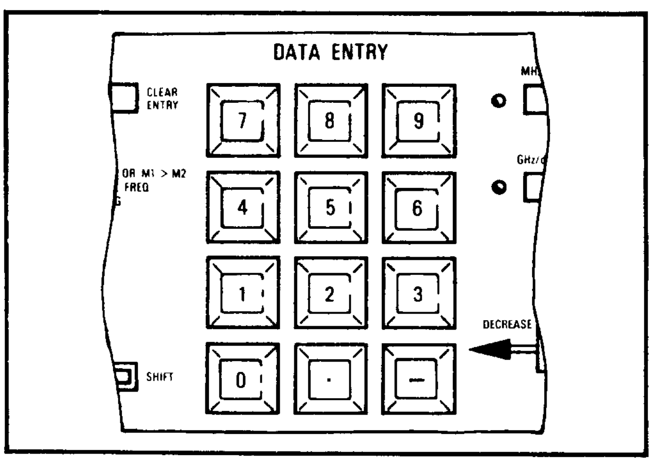


Figure 3-5. DATA ENTRY Keypad

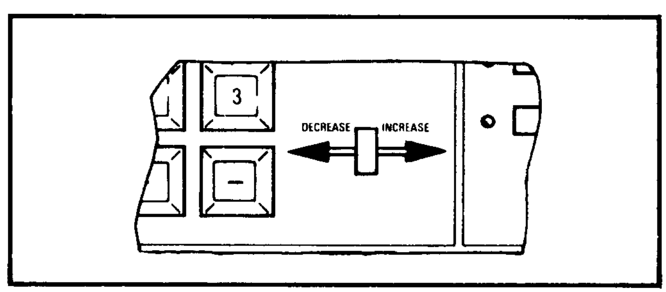


Figure 3-6. INCREASE/DECREASE Lever

change in 0.1 dB increments. And, a sweep time parameter will change in 1-ms increments between .01 and 1.0 seconds, 0.1-second increments between 1 and 10 seconds, and 1-second increments between 10 and 99 seconds.

d. MHz/dB/mS and GHz/dBm/Sec Pushbuttons (Figure 3-7). These two pushbuttons are data string terminators. That is, they mark the end of a parameter-input entry, and they assign the appropriate units (GHz, dBm, mS, etc.) to the entry. However, whereas

- a frequency parameter may be ended in either MHz or GHz, the value is always displayed in GHz.

- a sweep time parameter may be ended in either seconds (Sec) or milliseconds (mS), the value is always displayed in seconds.

- a power level parameter may be ended in either dB or dBm, the value is always displayed in dBm. The dB terminator pushbutton allows the displayed power level parameter to be either added to or subtracted from in dB's. When the dB terminator is used, the sweep generator performs the calculations that convert the output power to a value in dBm. Example 4 in Figure 3-3 shows the use of the dB terminator pushbutton.

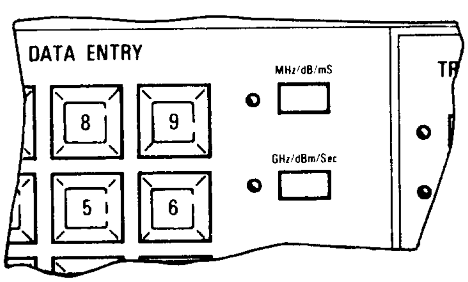


Figure 3-7. MHz/dB/mS and GHz/dBm/Sec (Terminator) Pushbuttons

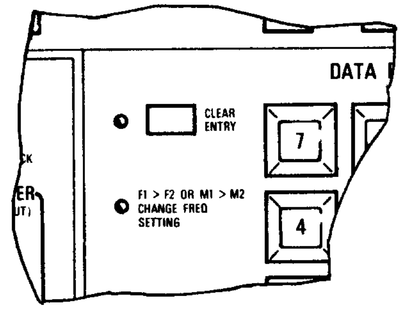


Figure 3-8. CLEAR ENTRY Pushbutton and F1>F2 OR M1>M2 Indicator

e. CLEAR ENTRY Pushbutton and Indicator and F1>F2 OR M1>M2 CHANGE FREQUENCY SETTING Indicator (Figure 3-8).

1. The CLEAR ENTRY pushbutton clears the keypad of an illegal or incomplete data entry (described below), and allows a new value to be entered.

2. The CLEAR ENTRY indicator flashes when an illegal or incomplete data entry has been attempted. (In addition, an illegal entry causes the LED readout displaying the illegal entry to flash; an incomplete entry causes both data terminator pushbutton indicators (Figure 3-7) to flash.)

3. The F1>F2 OR M1>M2 CHANGE FREQ SETTING indicator, along with the two LED readouts displaying frequency, flashes when a "backward" sweep is attempted. A backward sweep is when the respective value of F2 or M2 is less than that of F1 or M1. To clear a backward sweep, either re-enter the frequency values so that F1 or M1 is less than F2 or M2 or select a different frequency range.

An illegal entry is one in which a frequency, sweep time, or output-power level value beyond the range of the sweep generator is entered via the keypad. When this occurs, the CLEAR ENTRY pushbutton must be used to clear the keypad before the error can be corrected.

An incomplete entry is one in which a parameter value is entered on the keypad and the entry is not terminated with a terminator pushbutton (Figure 3-7). When this occurs, the error can be corrected by pressing the appropriate terminator pushbutton or by pressing the CLEAR ENTRY pushbutton and re-entering the data.

f. SHIFT Pushbutton (Figure 3-9). The SHIFT pushbutton is used to provide alternate functions for certain designated controls.

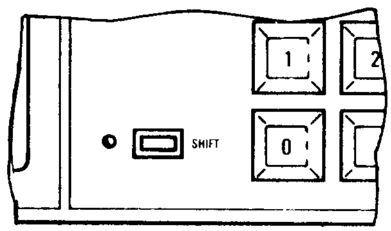


Figure 3-9. SHIFT Pushbutton

3-2.2 FREQUENCY RANGE Pushbuttons

The FREQUENCY RANGE pushbuttons are used to

- select the sweep generator's operational mode, either sweep or CW;
- apply fine-frequency vernier corrections to output frequency in the selected CW mode or to center frequency in the selected ΔF sweep mode;
- apply frequency modulation to or phase-lock control over output frequency in the selected CW output mode.

Individual FREQUENCY RANGE pushbuttons are described below.

a. FULL, F1-F2, M1-M2, ΔF F0, and ΔF F1 Pushbuttons (Figure 3-10). These pushbuttons select the sweep mode as follows:

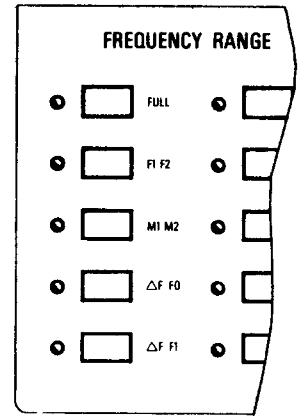


Figure 3-10. FULL, F1-F2, M1-M2, ΔF F0, ΔF F1 Pushbuttons

FULL: Selects a mode in which the frequency sweep is from the sweep generator's lower to its upper frequency limit. When FULL is engaged, its indicator lights, the lower frequency limit appears on the F1-F0-M1 LED readout, and the upper frequency limit appears on the F2-ΔF-M2 LED readout.

F1-F2: Selects a mode in which the frequency sweep is from F1 to F2. When F1-F2 is engaged, its indicator lights, the F1 frequency appears on the F1-F0-M1 LED readout, and the F2 frequency appears on the F2-ΔF-M2 LED readout.

M1-M2: Selects a mode in which the frequency sweep is from M1 to M2. When M1-M2 is engaged, its indicator lights, the M1 frequency appears on the F1-F0-M1 LED readout, and the M2 frequency appears on the F2-ΔF-M2 LED readout.

ΔF F0: Selects a mode in which the frequency sweep is symmetrical about the F0 frequency. The width of this sweep, though usually narrow-band, can go from 0 to 100% of the full frequency range. When ΔF F0 is engaged, its indicator lights, the F0 frequency appears on the F1-F0-M1 LED readout, and the ΔF Frequency appears on the F2-ΔF-M2 LED readout.

NOTE

The ΔF F0 and ΔF F1 sweeps can be asymmetrical. Asymmetry will occur when one/half the width of the ΔF sweep will cause the band-edge at either end of the frequency band to be exceeded. The sweep generator cannot sweep beyond its band-edges. (It will sweep only to the band-edge on one side of F0 (or F1) and up to one/half the ΔF sweep on the other side.)

ΔF F1: Selects a mode in which the frequency sweep is symmetrical about the F1 frequency. The width of this sweep and the frequency readouts are as described for ΔF F0, above.

The FULL, F1-F2, M1-M2, etc. controls are interlocked with the CW control group (subparagraph b, below) so that only one control can be engaged at any one time.

b. CW F0, CW F1, CW F2, CW M1, and CW M2 Pushbuttons (Figure 3-11).

These pushbuttons select a CW frequency mode, as follows:

CW F0: Selects a mode in which the CW frequency is at F0. When CW F0 is engaged, its indicator lights, and the F0 frequency appears on the F1-F0-M1 LED readout. The LED readout above F2-ΔF-M2 is blanked out.

CW F1: Selects a mode in which the CW frequency is at F1. When CW F1 is engaged, its indicator lights, and the F1 frequency appears on the F1-F0-M1 LED readout. The LED readout above F2-ΔF-M2 is blanked out.

CW F2: Selects a mode in which the CW frequency is at F2. When CW F2 is engaged, its indicator lights, and the F2 frequency appears on the F2-ΔF-M2 LED readout. The LED readout above F1-F0-M1 is blanked out.

CW M1: Selects a mode in which the CW frequency is at M1. When CW M1 is engaged, its indicator lights, and the M1 frequency appears on the F1-F0-M1 LED readout. The LED readout above F2-ΔF-M2 is blanked out.

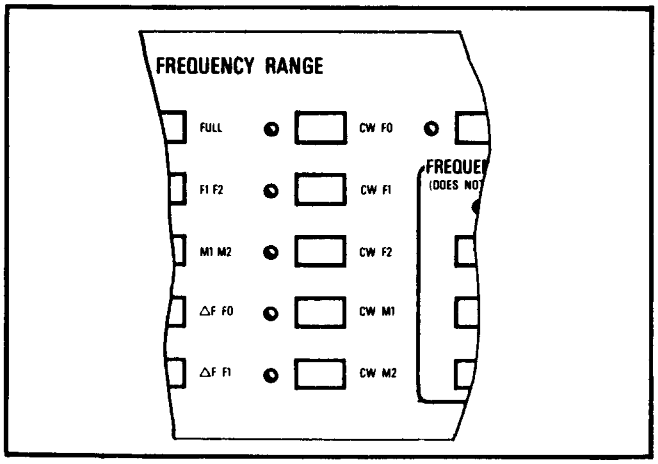


Figure 3-11. CW F0, CW F1, CW F2, CW M1/ and CW M2 Pushbuttons

CW M2: Selects a mode in which the CW frequency is at M2. When CW M2 is engaged, its indicator lights and the M2 frequency appears on the F2-ΔF-M2 LED readout. The LED readout above F1-F0-M1 is blanked out.

c. FREQUENCY VERNIER Pushbuttons (Figure 3-12). These pushbuttons may be used to make fine adjustments to (1) output frequency in the selected CW mode or (2) center frequency in the selected ΔF mode. The frequency resolution achievable using these pushbuttons is ±100 kHz. Individual pushbuttons are described below.

INCREASE: Increases by a maximum of 12.7 MHz the value of the selected CW

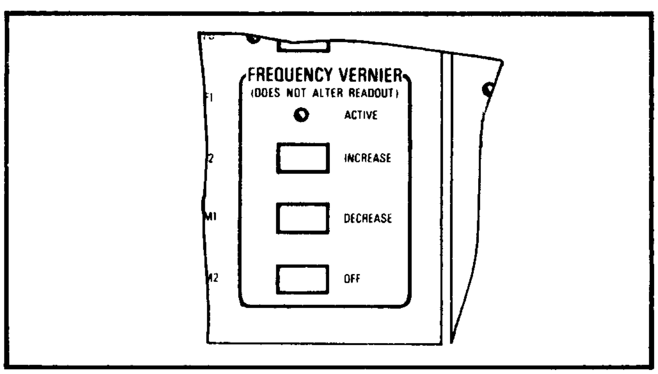


Figure 3-12. FREQUENCY VERNIER Controls

output or ΔF center frequency. The LED readout value of the selected CW or ΔF frequency is not affected by this control.

DECREASE: Decreases by a maximum of 12.7 MHz the value of the selected CW output or ΔF center frequency. The LED readout value of the selected CW or ΔF frequency is not affected by this control.

OFF: Cancels the vernier correction being applied to the selected CW output or ΔF center frequency and turns the ACTIVE indicator OFF in that mode.

NOTE

A different vernier correction value can be entered for each of the five frequency parameters (F0, F1, F2, M1, M2). Once made, the vernier correction is stored in memory with the parameter and remains in effect even when the sweep generator is turned off. Pressing the OFF pushbutton or changing the frequency value of a parameter cancels the vernier correction.

d. FM AND PHASELOCK Pushbutton (Figure 3-13). This pushbutton allows the sweep generator output frequency to be either frequency-modulated or phase-locked to an external frequency standard. The external FM or phase-lock signal is input via the rear panel EXT FM Ø LOCK INPUT connector.

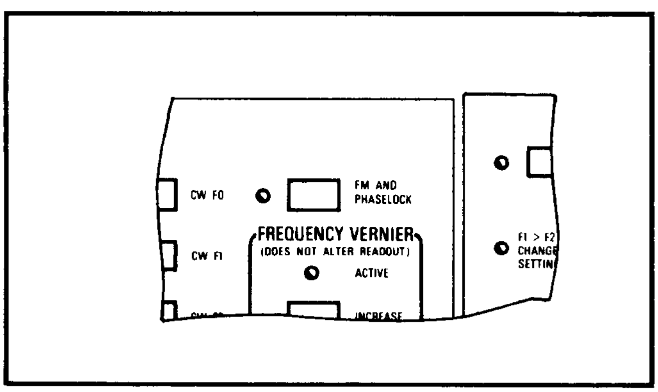


Figure 3-13. FM AND PHASELOCK Pushbutton

3-2.3 TRIGGER Pushbuttons

The TRIGGER pushbuttons (Figure 3-14) select a trigger mode for the frequency sweep. These pushbuttons are interlocked so that only one may be selected at a time. A description of each pushbutton follows:

AUTO: Selects a mode in which the sweep recurs periodically with a minimum delay (hold-off) time between sweeps.

LINE: Selects a mode in which the sweep recurs at a multiple or submultiple of the line frequency.

EXT OR SINGLE SWEEP: Selects a mode in which the sweep recurs only when internally or externally triggered. External triggering is via the rear panel EXT TRIGGER INPUT connector; internal triggering is via this pushbutton. When this pushbutton is first pressed, the mode is selected. When the pushbutton is next pressed, the sweep is triggered. And, if the pushbutton is pressed again while the sweep is in progress, the sweep is aborted and reset.

MANUAL SWEEP: Selects a mode in which the frequency band is manually tuned. Manual tuning is provided by the control associated with this pushbutton.

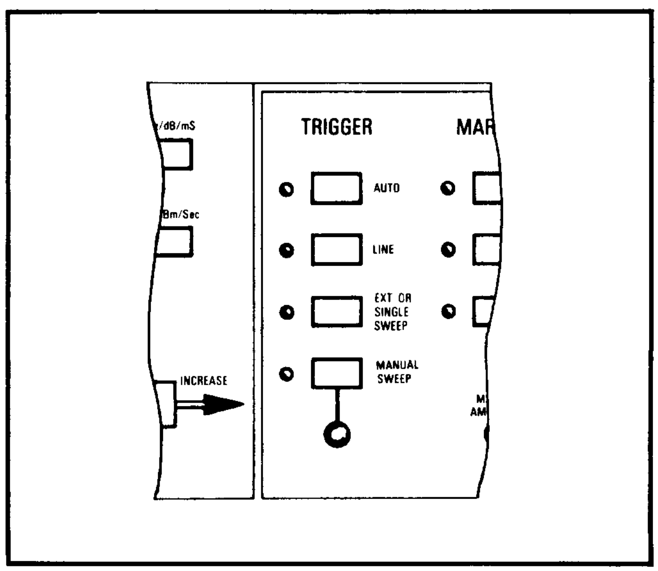


Figure 3-14. TRIGGER Pushbuttons

3-2.4 MARKERS Pushbuttons

There are three markers (M1, M2, F0) available with the sweep generator. The frequencies at which these markers occur are either user-defined and selected using the DATA ENTRY pushbuttons (paragraph 3-2.1), or they are preset and selected using the RESET pushbutton (paragraph 3-2.7). The type of marker that occurs at the marker frequency is selected using the MARKERS pushbuttons (Figure 3-15). The number of markers (1, 2, or 3) that actually occur when a MARKERS pushbutton is pressed is dependent upon which sweep mode is selected. For sweep modes FULL, F1-F2, and ΔF F1, three markers occur (M1, M2, and F0). For sweep mode ΔF F0, two markers occur (M1 and M2). And, for sweep mode M1-M2, one marker occurs (F0).

To determine which marker frequency (M1, M2, or F0) is being observed on a CRT display, press the M1, M2, and F0 pushbuttons while observing the display. The marker will disappear from the display when the corresponding pushbutton is pressed.

The MARKERS pushbuttons are described below. These pushbuttons are interlocked in such a way that all three may be off, but only one may be on at a time.

VIDEO: Causes a positive-video pulse to occur at the marker frequency(ies). The amplitude of this pulse can be adjusted from 0 to +5 volts using the MARKER AMPLITUDE control.

RF: Causes a negative RF pip to occur at the marker frequency(ies). The amplitude of this pip can be adjusted between 0 and approximately 10 dB using the MARKER AMPLITUDE control.

INTENSITY: Causes an intensity dot to occur at the marker frequency(ies). The intensity marker is created by causing the sweep to dwell at the marker frequency(ies). No connection is required between the sweep generator and a CRT Z-axis input. The intensity of this marker is not affected by the MARKER AMPLITUDE control.

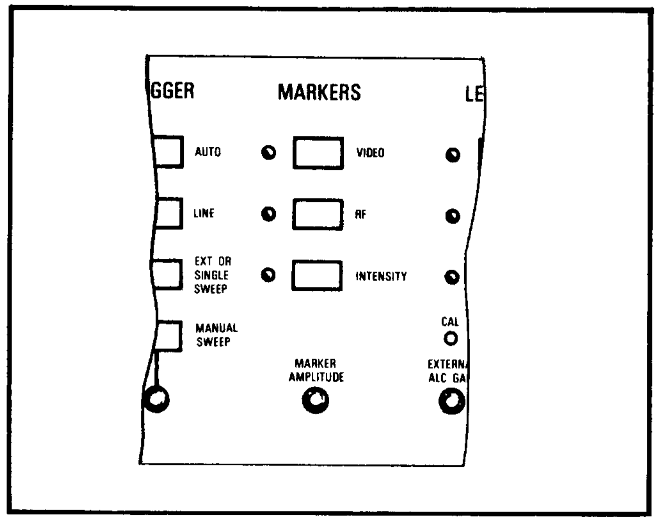


Figure 3-15. MARKERS Pushbuttons

NOTE

For the intensity marker to be used with the Model 560 Scalar Network Analyzer, the network analyzer must be in the REAL TIME display mode.

3-2.5 LEVELING Controls

The LEVELING controls (Figure 3-16) select the type of leveling to be employed. These controls are interlocked so that all three pushbuttons may be off, but only one pushbutton may be on at a time. A description of each pushbutton follows.

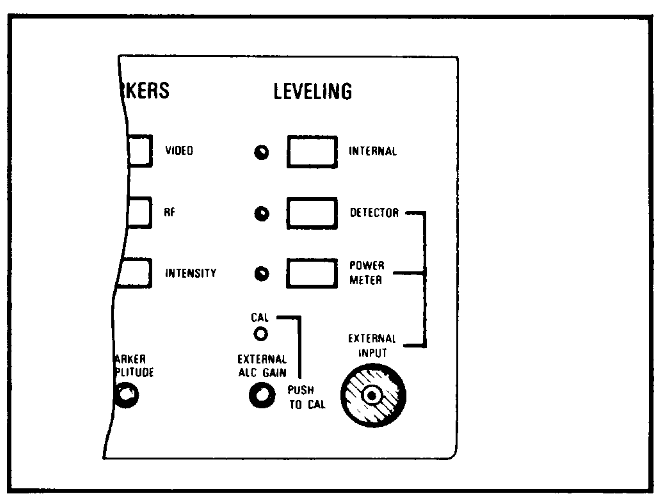


Figure 3-16. LEVELING Controls

INTERNAL: Selects an internally-mounted directional detector for use in leveling the output power. When this pushbutton is engaged, the output power is sampled at the front-panel connector and fed back for leveling control.

DETECTOR: Allows an external directional coupler and either a positive or a negative detector to be used in leveling the output power. When this pushbutton is engaged, the output power may be sampled at the end of the transmission line and fed back for leveling control.

POWER METER: Allows an external power meter, with either a positive or a negative recorder output voltage, to be used in leveling the output power. When this pushbutton is engaged, the output power may be sampled at the end of the transmission line and fed back for leveling control.

The sweep generator is compatible with power meters having a ±1V FS analog output, such as the HP431/432, HP435/436, and PM1009/1010 models.

EXTERNAL ALC GAIN: Adjusts the gain of the signal applied to the EXTERNAL INPUT connector. The control's calibrate function automatically indicates when the gain is adjusted correctly for optimum ALC operation. To use this function, push in and turn the control until the CAL indicator comes on and stays on continuously. The indicator goes out when the control is released to its normal position.

3-2.6 RF OUTPUT Controls, Indicators, and Connector

The RF OUTPUT controls, indicators, and connector (Figure 3-17) are described below.

RF ON (Pushbutton): Turns the RF output on and off.

RETRACE RF (Pushbutton): Turns the RF output on and off during sweep retrace. This control is interlocked with the RF ON control so that it cannot be turned on unless the RF ON control is on, but it can be turned off independently of the RF ON control.

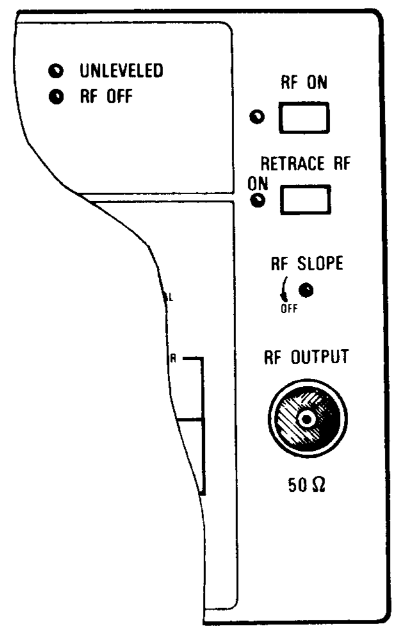


Figure 3-17. RF OUTPUT Controls

RF SLOPE (Control): Clockwise rotation adjusts the slope of the detected, leveled RF output signal. The control is used to compensate for the linear-with-frequency attenuation characteristics of RF transmission lines, when such lines are used with swept-frequency measurements. The OFF position provides optimum flatness at the RF OUTPUT connector.

UNLEVELED (Indicator): Lights when the RF output is unleveled.

RF OFF (Indicator): Flashes when the RF output is off.

RF OUTPUT (Connector): Provides RF output from 50Ω source. To prevent RF losses due to impedance mismatch, the mating connector and cable should have a 50Ω impedance rating.

3-2.7 POWER, SELF TEST, and RESET Controls

These controls (Figure 3-18) are described below.

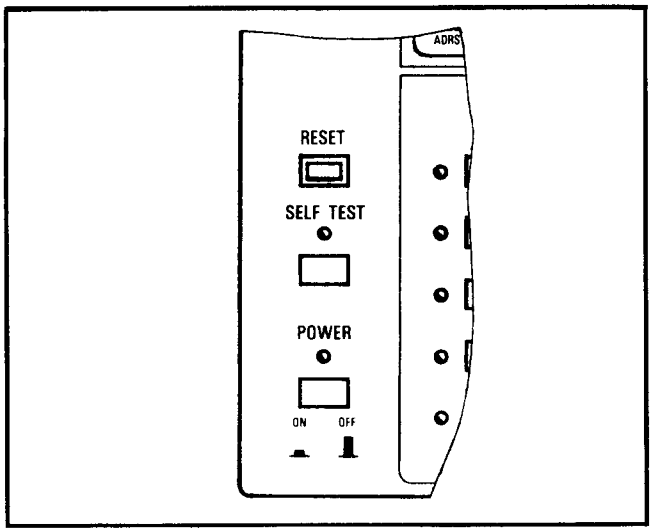


Figure 3-18. POWER, SELF TEST, and RESET Controls

POWER: Turns ac power on and off. When power is turned on, the A12 Microprocessor PCB software-version number (e.g. 1.7) appears on the F1-F0-M1 LED and a self test is initiated.

SELF TEST: Initiates self testing of sweep-generator circuits. Paragraph 3-4 describes the self-test feature.

RESET: Presets the front panel controls and numeric parameters as shown below.

Front Panel Controls

FREQUENCY RANGE: FULL (upper and lower frequency limits are displayed).
TRIGGER: AUTO
MARKERS: Off
LEVELING: INTERNAL
RF ON: On (output-power level is set to +10 dBm).

Numeric Parameters

F1: 2 GHz (Models 6637 & 6638),
10 MHz (Models 6647 & 6648)
F2: 18 GHz
F0: 10 GHz
M1: 3 GHz (Models 6637 & 6638),
2 GHz (Models 6647 & 6648)
M2: 17 GHz
ΔF: 1 GHz
SWEEP TIME: 50 ms
LEVEL: +10 dBm

3-2.8 BUS ADRS/RETURN TO LOCAL Control and GPIB Indicators

The BUS ADRS/RETURN TO LOCAL pushbutton and the REMOTE, LOCAL LOCKOUT, TALK, LISTEN, and SRQ GPIB indicators (Figure 3-19) are described below.

BUS ADRS/RETURN TO LOCAL (Pushbutton): In the local (front panel) mode, the pushbutton causes the bus address to be displayed on the SWEEP TIME-LEVEL LED readout. In the remote (GPIB) mode, provided that a local lockout bus message is not programmed, the pushbutton causes the sweep generator to return to the local mode.

REMOTE (Indicator): Lights when goes under GPIB control. Remains lit until sweep generator is returned to local control.

LOCAL LOCKOUT (Indicator): Lights when sweep generator receives a local lockout message; remains lit until local lockout message is recinded. When LOCAL LOCKOUT indicator is lit, sweep generator cannot be returned to local control via the front panel.

TALK (Indicator): Lights when sweep generator is addressed to talk; remains lit until unaddressed.

LISTEN (Indicator): Lights when sweep generator is addressed to listen; remains lit until undressed.

SRQ (Indicator): Lights when sweep generator sends a Service Request; remains lit until a serial poll is received or SRQ function is reset (paragraph 3-7.4).

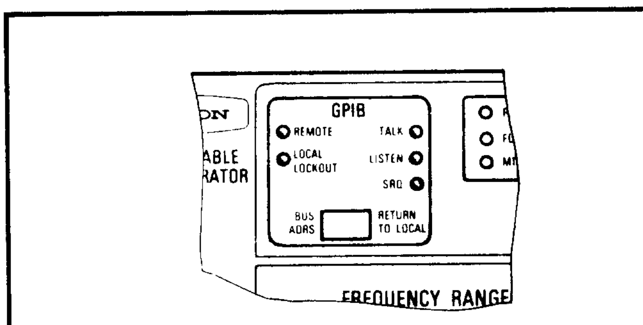
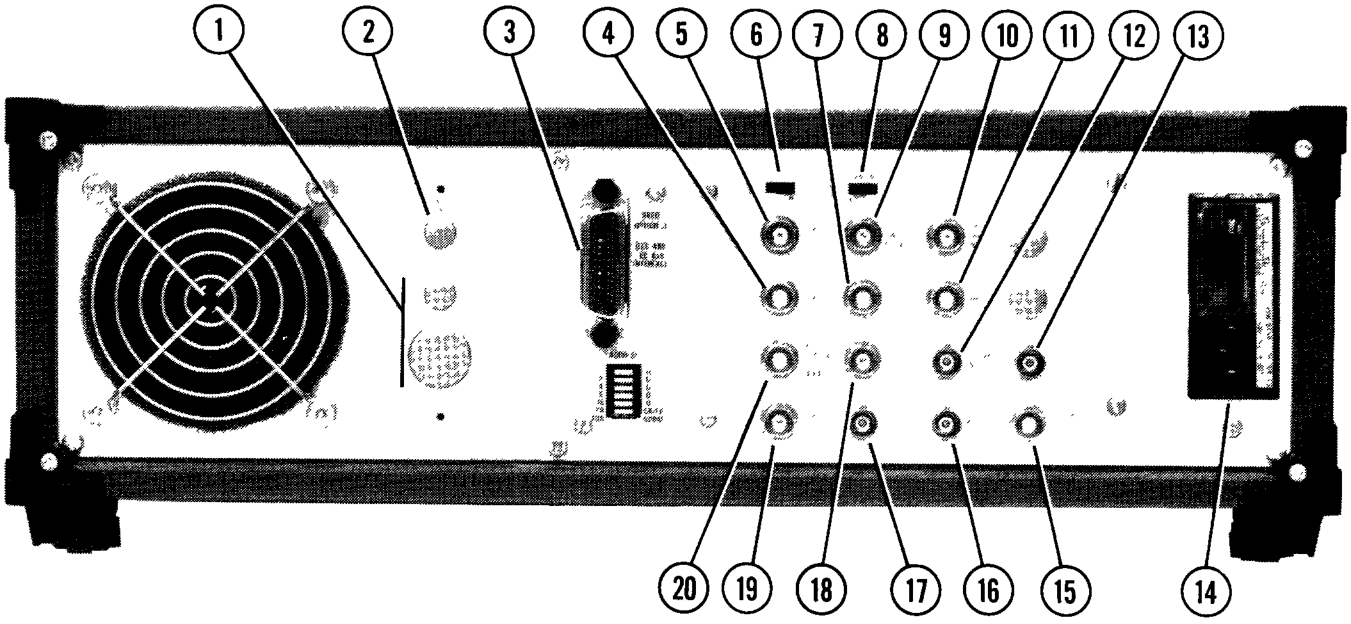


Figure 3-19. BUS ADRS/RETURN TO LOCAL Control and GPIB Indicators

3-3 REAR PANEL CONTROLS AND CONNECTORS

The rear panel controls and connectors are described in Figure 3-20.



(1) **Main RF OUTPUT Connector (Option 9):** Provides 50-ohm RF output.

(2) **Auxiliary RF OUTPUT Connector (Option 10):** Provides 50-ohm RF output. Output power is attenuated by ≈25 dB from the power available at the main RF connector.

(3) **IEEE-488 Interface Bus Connector (Option 3):** Provides input output connections to General Purpose Interface Bus (GPIB).

(4) **SEQ SYNC OUTPUT:** Provides a positive pulse during sweep retrace and when the RF plug-in switches between different YIG oscillators (bandswitches). Signal is used to supply bandswitching and retrace information to the WILTRON Model 560 and HP Model 8410 Network Analyzers. Connects to FROM SEQ SYNC WILTRON connector on Model 560 Scalar Network Analyzer.

(5) **HORIZ OUTPUT:** Provides 0 to 10 volts during all sweep modes, and during all CW modes when HORIZ OUTPUT DURING CW switch is ON. Connects to HORIZ INPUT connector on Model 560 Scalar Network Analyzer.

(6) **HORIZ OUTPUT DURING CW:** Causes the 0-10V horizontal ramp, available at the HORIZ OUTPUT connector, to be switched on or off by pressing either CW F0, CW F1, CW F2, CW M1, or CW M2.

NOTE

The HORIZ OUTPUT DURING CW switch should be OFF except when interfacing with the WILTRON Model 560 Scalar Network Analyzer.

(7) **1V/GHz OUTPUT:** Provides voltage signal equal to 1V per GHz. Signal may be used as an approximate frequency reference and also for tuning the HP 8410B Network Analyzer.

(8) **BANDSWITCH BLANKING (+, -):** Switches BANDSWITCH BLANKING signal either plus or minus.

(9) **BANDSWITCH BLANKING:** Provides + or -5V pulse, depending on BANDSWITCH BLANKING switch, during RF oscillator bandswitching. ±5V pulse may be used to blank sweep generator bandswitch points on oscilloscope display.

(10) **SWEEP TRIGGER INPUT:** Provides for external sweep triggering when TRIGGER-EXT OR SINGLE SWEEP pushbutton is engaged. Trigger occurs on closure-to-ground. To provide for proper triggering, the input pulse should be a clock pulse with the following characteristics:

Amplitude: 4 to 25 Vpk
Pulse Width: >1μs
Fall Time: <5μs
Polarity: Low true

(11) **SWEEP DWELL INPUT:** Allows a pulse from the HP 8410 Network Analyzer to cause the sweep generator sweep to dwell during 8410 sweep retrace.

(12) **EXT AM INPUT:** Provides for applying amplitude modulation to the RF output signal. The frequency of the modulating signal can go from dc to 50 kHz. Input impedance is 10 kilohms.

(13) **EXT SQ WAVE INPUT:** Provides for applying square-wave modulation to the RF output signal. The input square wave can have a frequency of up to 50 kHz and an amplitude of ±10 volts. Input impedance is TTL compatible.

(14) **Voltage Selector Module:** Allows 100, 115/120, 220, or 230/240 Vac line voltage values to be used with sweep generator. Refer to paragraph 2-3 for setup instructions.

(15) **EXT SWEEP:** Allows an external 0 to 10 volt ramp to be used to sweep the output frequency. To use this input, the INT-EXT switch on the Ramp Generator (A2) printed circuit board must be in the EXT position.

(16) **EXT FM Ø LOCK INPUT:** Provides for applying frequency modulation and phase-lock control (paragraph 3-2.2d) to the RF output signal.

(17) **PENLIFT OUTPUT:** Provides isolated, normally-open relay contacts for lifting recorder pen during sweep retrace. Can be modified internally for normally-closed relay contact operation.

(18) **RETRACE BLANKING OUTPUT (-):** Provides -5V pulse during sweep retrace.

(19) **MARKER OUTPUT:** Provides video marker output when MARKERS-VIDEO pushbutton is engaged. Connects to MARKER INPUT connector on Model 560 Scalar Network Analyzer.

(20) **RETRACE BLANKING OUTPUT (+):** Provides +5V pulse during sweep retrace. Connects to FROM BLANKING (+) WILTRON connector on WILTRON Model 560 Scalar Network Analyzer.

Figure 3-20. Rear Panel Controls and Connectors

3-4 SELF-TEST FEATURES

The sweep generator is equipped with a self-test feature that uses an internal microprocessor to test (1) selected circuits on each of the printed circuit boards and (2) all of the indicators and LED displays on the front panel. There are three ways in which a self-test is initiated. And, if an error is detected, there are up to 25 error codes that may be displayed on the front panel. The three ways in which a self-test is initiated are described in Table 3-1; the 25 error codes are described in Table 3-2.

Table 3-1. Three Ways in Which Self-Test is Initiated

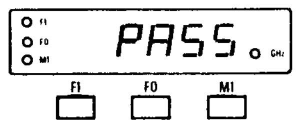
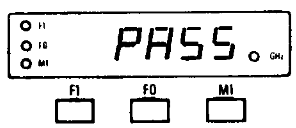
How Self Test Is Initiated	Indication If Self Test Passes	Indication If Self Test Fails
1. Pressing POWER pushbutton to ON.		An error code number between 00 and 24 is displayed above the F2-ΔF-M2 group of pushbuttons (Table 3-2).
2. Pressing SELF TEST.	a. All front panel indicators and LED displays are tested. (Indicators and displays light and remain lit 5 seconds.) and b. 	Same as above.
3. Sending sweep generator TST command over the bus (Option 3).	a. Numeric LED readouts are blanked. b. The ASCII character "P" is sent over the bus to the controller.	a. Numeric LED readouts are blanked. b. The ASCII character "F" is sent over the bus to the controller.

Table 3-2. Self-Test Error Codes

GENERAL: The microprocessor's self-test routines reside in software modules; each module is assigned an error-code number. When a self-test is initiated, these software modules are called up in sequential order, beginning with number 00 and ending with number 24. If an error is detected, the error-code number is displayed and the self-test continues. If multiple errors are detected, each error-code number is displayed. To abort self-test once it has begun, press the RESET pushbutton.

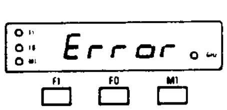
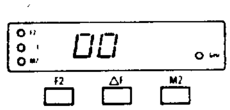
SWEEP GENERATOR ERROR DISPLAY	MEANING OF ERROR CODE	RECOMMENDED ACTION
 	A voltage supply other than the 5V supply is out of tolerance. If the 5V supply is faulty, the sweep generator will not operate.	See Figure 7-88 for troublehsooting flow-chart.

Table 3-2. Self-Test Error Codes (continued)

SWEEP GENERATOR ERROR DISPLAY	MEANING OF ERROR CODE	RECOMMENDED ACTION
Error 01	Line voltage too low.	See Figure 7-89 for troublehsooting flow-chart.
Error 02	Line voltage too high.	See Figure 7-90 for troubleshooting flow-chart.
Error 03	ROM U5 fails bit parity check.	Replace A12 U5.
Error 04	ROM U6 fails bit parity check.	Replace A12 U6.
Error 05	ROM U7 fails bit parity check.	Replace A12 U7.
Error 06	ROM U8 fails bit parity check.	Replace A12 U8.
Error 07	ROM U9 fails bit parity check.	Replace A12 U9.
Error 08	RAMs U11 and U12 fail write verification test.	Replace A12 U11 and A12 U12.
Error 09 Error 10 Error 11	These codes indicate that an analog circuit error was detected during testing of the Frequency Instruction (A5) and YIG Driver PCBs. Error code (EC) 09 is associated with the Heterodyne Band, EC10 with the 2-8 GHz YIG band, and EC 11 with the 8-12.4 GHz YIG band. NOTE Error code 09 not used with Model 6637 or 6638 Programmable Sweep Generator.	See Figure 7-64 (error code 09), 7-65 (error code 10) or 7-66 (error code 11) for troubleshooting flow-chart.

Table 3-2. Self-Test Error Codes (continued)

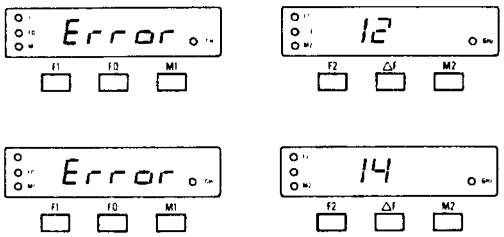
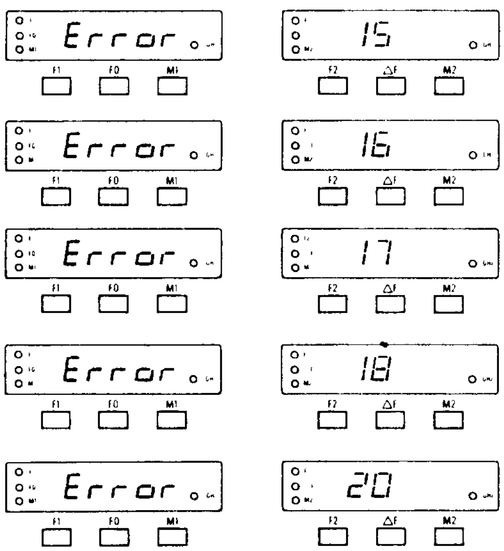
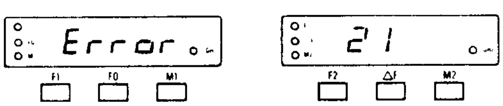
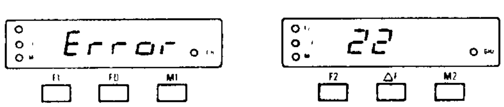
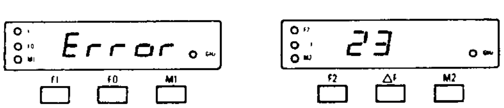
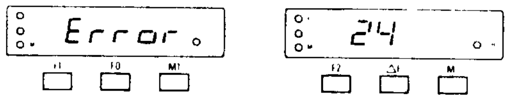
SWEEP GENERATOR ERROR DISPLAY	MEANING OF ERROR CODE	RECOMMENDED ACTION
	These codes indicate that an analog circuit error was detected during testing of the Frequency Instruction (A5) and YIG Driver PCBs. Error code 12 is associated with the 12.4-18.6 (or 20) GHz YIG band, and EC 14 with all of the bands.	See Figure 7-67 (error code 12) or 7-68 (error code 14) for troubleshooting flowchart.
	These codes indicate that an analog circuit error was detected during Automatic Level Control (A4) PCB test. Error code 15 is assoicated with the Heterodyne Band, EC 16 with the 2-8 GHz YIG band, EC17 with the 8-12.4 GHz YIG band, EC18 with the 12.4-18.6 GHz YIG band, and EC 20 with all of the bands. NOTE Error code 15 not used with Model 6637 or 6638 Programmable Sweep Generator.	See Figure 7-42 (error code 15), 7-43 (error code 16), 7-44 (error code 17), 7-45 (error code 18) or 7-46 (error code 20) for troubleshooting flowchart.
	Analog circuit error, detected during Ramp Generator (A2) PCB test.	See Figure 7-31 for troubleshooting flowchart.
	Analog circuit error, detected during Marker (A3) PCB test.	See Figure 7-36 for troubleshooting flowchart.
	Analog circuit error. detected during FM Attenuator (A10) PCB test.	See Figure 7-72 for troubleshooting flowchart.

Table 3-2. Self-Test Error Codes (continued)

SWEEP GENERATOR ERROR DISPLAY	MEANING OF ERROR CODE	RECOMMENDED ACTION
	Only appears if Option 3 installed. Indicates error detected during GPIB Interface (A1) PCB test.	See Figure 7-25 for troubleshooting flow-chart.

3-5 OPERATIONAL CHECKOUT PROCEDURES

The operational checkout procedures for the sweep generator are given in paragraphs 3-5.1, 3-5.2, and 3-5.3. These procedures are organized by function, so that only those functions being used need to be checked.

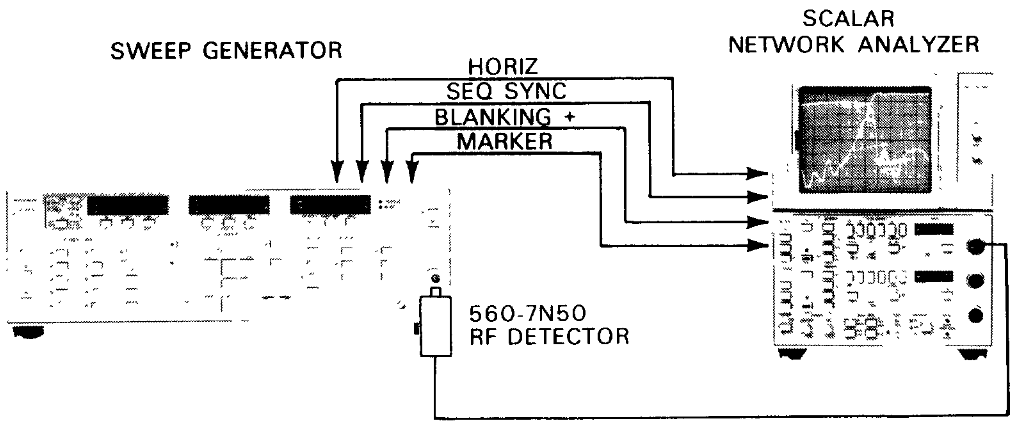
Table 3-3 gives the recommended test equipment for the three operational checkout procedures (Tables 3-4, 3-5, 3-6). Notice that the test equipment differs for each checkout procedure. If the recommended test equipment is not available, equipment with equivalent characteristics may be substituted.

3-5.1 Operational Checkout, Sweep Generator Confidence Test

This paragraph provides the confidence test procedure for the sweep generator. Figure 3-21 shows the test setup and Table 3-4 gives the test procedure.

Table 3-3. Recommended Test Equipment for Operational Checkout

EQUIPMENT	REQUIRED CHARACTERISTICS	RECOMMENDED MANUFACTURER	PURPOSE
Scalar Network Analyzer	Ability to display frequency response of sweep generator.	WILTRON Model 560 Scalar Network Analyzer	Display sweep generator output during operational checkout.
Microwave Frequency Counter	10 MHz to 18 GHz frequency response.	EIP Model 371	Used with Table 3-5 to check the operation of FREQUENCY VERNIER controls.
Microwave Frequency Counter	10 MHz to 18 GHz frequency response with source-locking capability.	EIP Model 371	Used with Table 3-5 to check the operation of phase-locking capability.
Directional Coupler	Ability to couple signals within a portion of the 10 MHz to 18 GHz frequency range.	NARDA Model 3202B-10	
RF Detector	Ability to detect signals within the 10 MHz to 18 GHz frequency range.	WILTRON Model 75N50	Used with Table 3-6 to check the operation of external leveling feature.
Power Meter	Ability to provide output signal that is (1) proportional to the measured power and (2) 1 volt for full-scale deflection.	Hewlett-Packard Model 435A	



Initial Control Settings

Sweep Generator

MARKER AMPLITUDE: Fully CW
HORIZ OUTPUT DURING CW
(rear panel): ON
SLOPE: OFF

Scalar Network Analyzer

CHANNEL A ON: On
INPUT: A
MEMORY: Off
dB PER DIVISION: 5
REFERENCE dB/dBm: dBm
SET (screwdriver pot): Midrange
OFFSET: -00.0
CHANNEL B: Not used
MARKER THRESHOLD: Midrange
REAL TIME: On
SMOOTHING: Off
POWER: ON

Figure 3-21. Equipment Setup for Confidence Test

Table 3-4. Sweep Generator Confidence Test

1. Connect the equipment as shown in Figure 3-21.
2. Turn on the sweep generator and press [RESET]. If no error code appears on the appropriate LED readouts (Table 3-2), the sweep generator should be functioning normally.
3. Observe the 560 CRT. A leveled trace should be located near center screen.
4. Press [INTERNAL]. The 560 trace should go unleveled.
5. Press [INTERNAL]. A leveled trace returns to the 560 CRT.
6. Press [LEVEL] [1] [0] [GHz/dBm/Sec]. Verify that the 560 trace "jumps" 2 divisions (10 dB), and that the trace remains level.

END OF CONFIDENCE TEST

3-5.2 Operational Checkout Procedure, FREQUENCY VERNIER Pushbuttons and Phase-Lock Operation

The FREQUENCY VERNIER pushbuttons provide for making small changes (up to ±12.7 MHz) to the output frequency in the CW F0 thru CW M2, ΔF F0, and ΔF F1 operational modes. These frequency changes do not affect the readout that appears on the respective frequency's front panel LED display.

The phase-lock operation automatically "locks" the sweep generator's output frequency to the crystal-controlled time base of the frequency counter. When the EIP 371 Source Locking Counter is used, the phase-lock function allows the sweep generator's frequency to be accurately resolved to 100 kHz.

The test setup for operationally checking the FREQUENCY VERNIER controls and phase-lock operation is shown in Figure 3-22; the checkout procedure is given in Table 3-5.

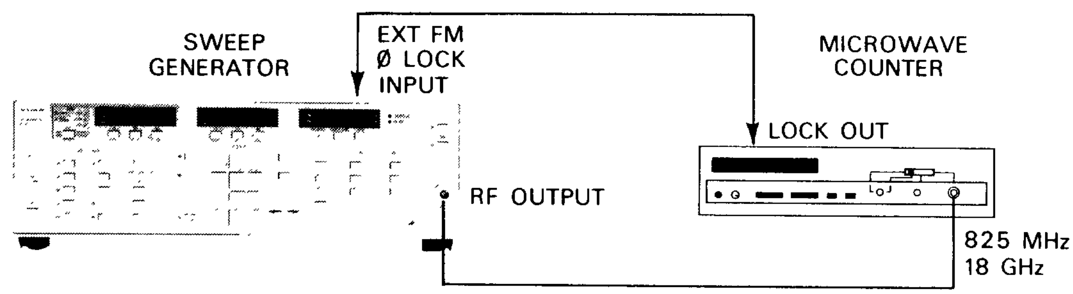


Figure 3-22. Test Setup for Operationally Checking the FREQUENCY VERNIER Controls

Table 3-5. Operational Checkout Procedure, FREQUENCY VERNIER Controls and Phase-Lock Operation

1. Turn on power to sweep generator (sweeper) and frequency counter (counter).
2. On sweeper, press [LEVEL] [0] [GHz/dBm/Sec] (or use [DECREASE/INCREASE]) to set the output level for 0 dBm.
3. Connect 50Ω cable between RF OUTPUT on sweeper and 825 MHz - 18 GHz input on counter.

Frequency-Vernier-Controls Operation

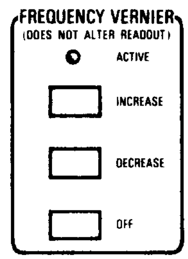
4. On sweeper:

   a. Press [CW F0].

Table 3-5. Operational Checkout Procedure, FREQUENCY VERNIER Controls and Phase-Lock Operation (continued)

b. Press [F0] [4] [GHz/dBm/Sec] (or use [DECREASE / INCREASE]) to enter a frequency of 4 GHz.

c. Observe counter. If frequency readout is not 4.000 GHz, the FREQUENCY VERNIER can be used to obtain this value. Adjust these controls as follows:



1) If the counter's frequency readout is below 4.0 GHz, press [INCREASE] until the frequency reads 04 000 0XX XXX.

2) If the counter's frequency readout is above 4.0 GHz, press [DECREASE] until the frequency reads 04 000 0XX XXX.

NOTE

When either the INCREASE or the DECREASE pushbutton is pressed, the ACTIVE indicator will light.

d. Press [CW F2]

e. Press [F2] [9] [GHz dBm Sec] (or use [DECREASE / INCREASE]) to enter a frequency of 9 GHz.

f. Observe counter. If frequency readout is not 9.000 GHz, adjust the FREQUENCY VERNIER controls as described in c, above, until this value is obtained.

g. Press [CW M2]

h. Press [M2] [1] [7] [GHz dBm Sec] (or use [DECREASE / INCREASE]) to enter a frequency of 17 GHz.

i. Observe counter. If frequency readout is between 16 987 3XX XXX and 17 012 7XX XXX (12.7 MHz), adjust the FREQUENCY VERNIER controls as described in c, above, until the counter indicates 17 000 0XX XXX.

Table 3-5. Operational Checkout Procedure, FREQUENCY VERNIER Controls and Phase-Lock Operation (continued)

j. Verify that the ○ ACTIVE lamp indicates which CW and ΔF Sweep frequencies have received a vernier correction, as follows:

1. Press [CW F0] ○ ACTIVE lit.
2. Press [CW F1] ○ ACTIVE not lit.
3. Press [CW F2] ○ ACTIVE lit.
4. Press [CW M1] ○ ACTIVE not lit.
5. Press [CW M2] ○ ACTIVE lit.
6. Press [ΔF F0] ○ ACTIVE lit.
7. Press [ΔF F1] ○ ACTIVE not lit.

k. Verify that the frequency-vernier correction is cancelled when the frequency to which a vernier correction was applied is changed, as follows:

1. Press [CW F0]
2. Press [F0] [5] [GHz·dBm·Sec]
3. Verify that ○ ACTIVE is not lit.

l. Verify that the frequency-vernier correction is disabled when [OFF] is pressed, as follows:

1. Press [CW F2]
2. Press [OFF] Verify that ○ ACTIVE goes out.

<u>Phase-Lock Operation</u>

5. Connect BNC-to-BNC test cable between LOCK OUT on counter and EXT FM Ø LOCK INPUT on sweeper.

6. On counter, enter a lock frequency of 10,000.0 MHz (use keypad and enter a reading of 10,000.0 on auxiliary (small) display).

Table 3-5. Operational Checkout Procedure, FREQUENCY VERNIER Controls and Phase-Lock Operation (continued)

7. On sweeper:

   a. Press [CW F1]

   b. Press [F1] [1] [0] [GHz/dBm/Sec]

   c. Press [FM AND PHASELOCK]

8. On counter, press LOCK.

9. Observe counter, it should indicate 10 000 000 000 ±1 count.

3-5.3 Operational Checkout Procedure, External Leveling Function

External leveling of the RF source is provided by the front panel EXTERNAL INPUT connector and the LEVELING-DETECTOR or -POWER METER pushbutton. A test setup for external leveling is shown in Figure 3-23; the operational checkout procedure is given in Table 3-6.

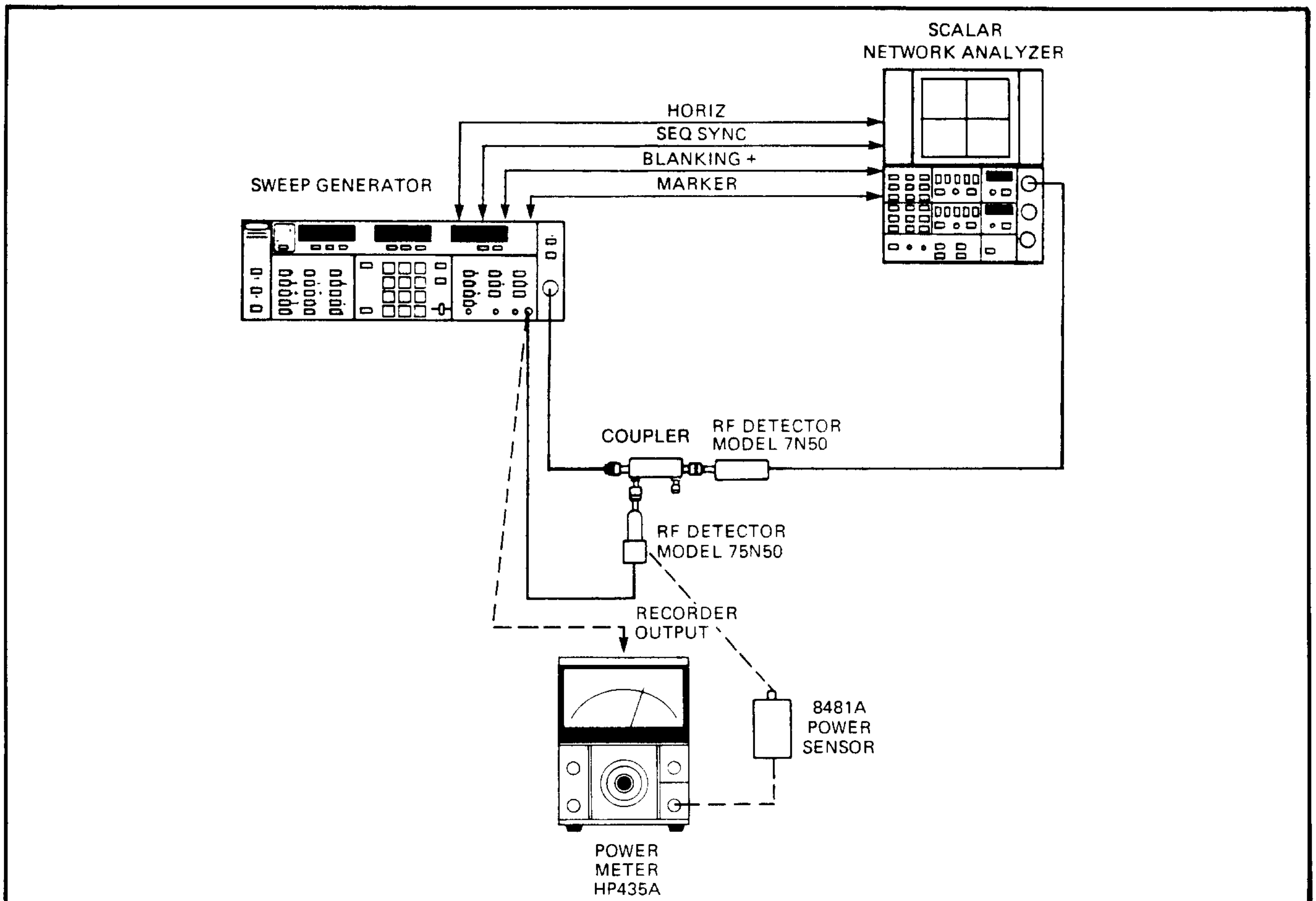


Figure 3-23. External Leveling Test Setup

Table 3-6. Operational Checkout Procedure, LEVELING-DETECTOR and -POWER METER Controls

1. Connect test equipment for detector leveling, as shown by the solid lines in Figure 3-23.

2. Turn on power on sweep generator (sweeper) and scalar network analyzer (network analyzer).

3. On sweeper:

   a. Press [F1 F2]

   b. Press [F1] [1] [GHz/dBm/Sec]

   c. Press [F2] [1] [2] [.] [4] [GHz/dBm/Sec]

   NOTE

   A frequency range of 1 to 12.4 GHz is being used because that is the range of the NARDA 3202B-10 coupler.

   d. Press [LEVEL] [0] [GHz/dBm/Sec]

   e. Press [SWEEP TIME] [5] [0] [MHz/dB/mS]

   f. Press [AUTO]

   g. Press [INTERNAL]

4. On network analyzer:

   a. Position front panel controls as follows:

      CHANNEL A ON: On
         INPUT A: A
         MEMORY: Off
         REFERENCE dB/dBm: dBm
         OFFSET: 00.0
         dB PER DIVISION: 1

      CHANNEL B: Not Used
      MARKER THRESHOLD: Off
      REAL TIME: On
      SMOOTHING: Off

Table 3-6. Operational Checkout Procedure, LEVELING-DETECTOR and -POWER METER Controls (Continued)

b. Press Channel A REF POS LOCATE and adjust SET control to position trace on center graticule line.

c. Release REF POS LOCATE and observe that a leveled trace slightly below the 0 dBm reference line appears on the CRT.

5. On sweeper:

a. Press DETECTOR

b. Push in on EXTERNAL ALC GAIN PUSH TO CAL control and turn until CAL comes on and remains on.

c. Release EXTERNAL ALC GAIN PUSH TO CAL

6. Observe that a leveled trace is present on the 560 CRT.

7. Observe that UNLEVELED is not lit.

8. Press DETECTOR to off. Observe that the 560 trace becomes unleveled and the sweeper UNLEVELED lamp lights.

9. Disconnect RF detector from between the sweeper and the directional coupler; in its place, connect the power meter as shown by the dashed lines in Figure 3-23.

10. On sweeper:

a. Press CW F1

b. Press POWER METER

c. Push in on EXTERNAL ALC GAIN PUSH TO CAL control and turn until CAL comes on and remains on.

d. Release EXTERNAL ALC GAIN PUSH TO CAL

NOTE

The response to a changing power level is slow using a power meter; consequently, external leveling should be accomplished using either CW or a slow sweep speed.

END OF PROCEDURE

3-6 DESCRIPTION OF THE IEEE 488 (IEC 625) INTERFACE BUS

The IEEE 488 bus (General Purpose Interface Bus – GPIB) is an instrumentation interface for integrating instruments, calculators, and computers into systems. The bus uses 16 signal lines to effect transfer of data and commands to as many as 15 instruments. The instruments on the bus are connected in parallel, as shown in Figure 3-24. Eight of the signal lines (DIO 1 thru DIO 8) are used for the transfer of data and other messages in a byte-serial, bit-parallel form. The remaining eight lines are used for communications timing (handshake), control, and status information. Data is transmitted on the eight GPIB data lines as a series of eight-bit characters, referred to as bytes. Normally, a seven-bit ASCII (American

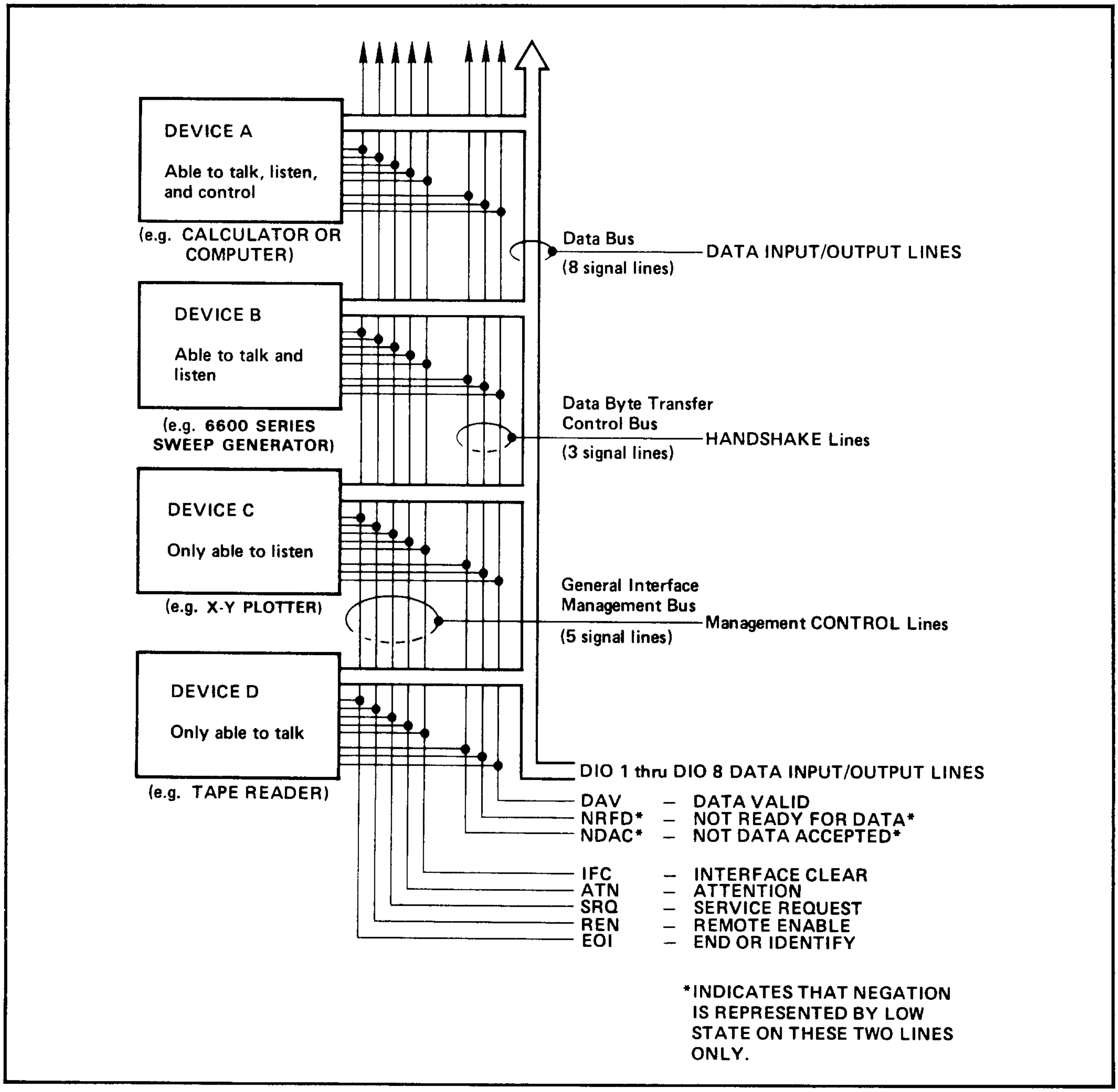


Figure 3-24. Interface Connections and Bus Structure

Standard Code for Information Interchange) code is used. The eighth (parity) bit is not used. Data is transferred by means of an interlocked handshake technique. This technique permits asynchronous communications over a wide range of data rates. The following paragraphs provide an overview of the data, management, and handshake buses, and describe how these buses interface with the sweep generator.

3-6.1 Data Bus Description

The data bus contains eight bi-directional, active-low signal lines – DIO 1 thru DIO 8. One byte of information (eight bits) is transferred over the bus at a time. DIO 1 represents the least-significant bit (LSB) in the byte; DIO 8 represents the most-significant bit (MSB) in the byte. Each byte represents a peripheral address (either primary or secondary), a control word, or a data byte. Data bytes are usually formatted in ASCII code, without parity. The data bus provides the conduit for transmitting control information and data between the controller and the instrument (sweep generator).

3-6.2 Management Bus Description

The management bus is a group of five signal lines that are used to control the operation of the bus system. Functional information regarding the individual management-bus control lines is provided below.

a. ATN (attention). When this line is TRUE, the sweep generator will respond to appropriate interface messages (e.g. device clear and serial poll) and to its own listen/talk address.

b. EOI (end or identify). This line is set TRUE during the last byte of a multi-byte message. This line is also used in conjunction with ATN to indicate a parallel-poll.

c. IFC (interface clear). When this line is TRUE, the sweep generator interface functions are placed in a known state, i.e., unaddressed to talk, unaddressed to listen, and service request idle.

d. REN (remote enable). When this line is TRUE, the sweep generator is enabled for entrance into the remote state (i.e., certain front panel functions disabled) upon receipt of its listen address. The remote state is exited when either (1) the REN line is FALSE (high), (2) the go-to-local (GTL) message is received, or (3) the sweep generator programming command RL (return to local) is received.

e. SRQ (service request). This line is pulled LOW (true) by the sweep generator to indicate that certain conditions (paragraph 3-7.4) exist.

3-6.3 Data Byte Transfer Control (Handshake) Bus Description

Information is transferred on the data lines under control of a technique called the three-wire handshake. The three handshake bus signal lines are described below; Figure 3-25 shows a typical interlocking handshake operation.

a. DAV (data valid). This line is set TRUE (arrow 1) when the talker has (1) sensed that NRFD is FALSE, (2) placed a byte of data on the bus, and (3) waited an appropriate length of time for the data to settle.

b. NRFD (not ready for data). This line is set TRUE (arrow 2) by a listener to indicate that valid data has not yet been accepted. The time between the events shown by arrows 1 and 2 is variable, and depends upon the speed with which a listener can accept the information.

c. NDAC (not data accepted). This line is set FALSE by a listener when the listener has accepted the current data byte for internal processing. When the data byte has been accepted, the listener releases its hold on NDAC and allows the line to go FALSE. However, because the GPIB is constructed in a wired-OR configuration, this line will not go FALSE until all listeners participating in the interchange have also released the line. As shown by the arrow labeled 3, when the NDAC line

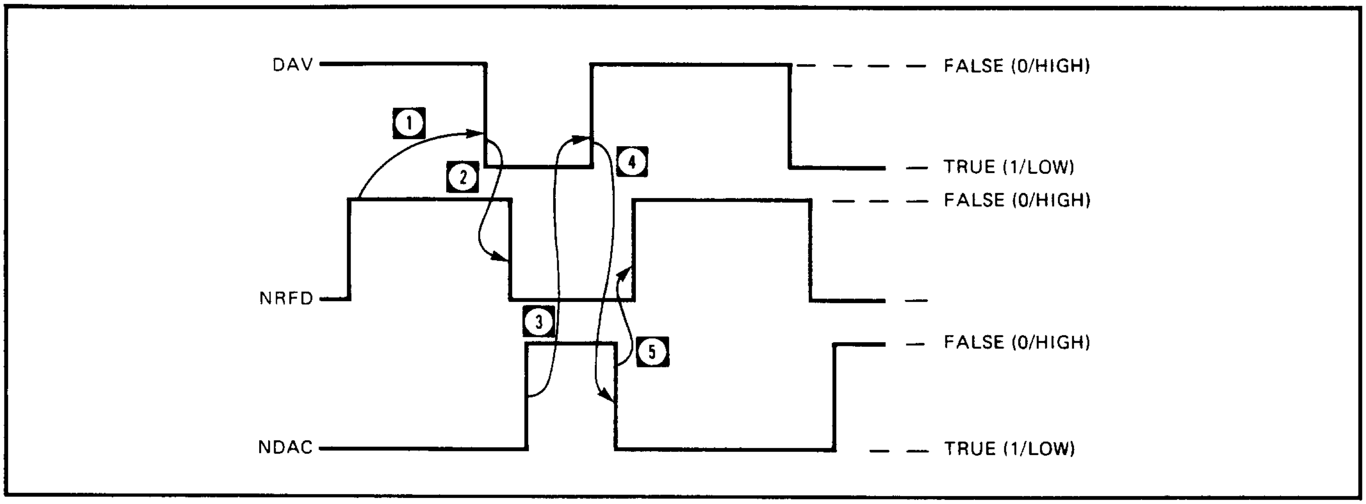


Figure 3-25. Typical Handshake Operation

goes FALSE the DAV line follows suit a short time later. The FALSE state of the DAV line indicates to the bus that valid data has been removed; consequently, with valid data no longer on the line, the NDAC line is pulled LOW again in preparation for the next data interchange. This action is shown by the arrow labeled 4.

The next action that occurs is shown by arrow 5. This arrow shows NRFD going FALSE after NDAC returns to its TRUE state. The FALSE state of NRFD indiciates to the bus that all listeners are ready for the next information interchange. The time period between these last two events (NDAC going TRUE and NRFD going FALSE) is variable and is dependent upon the length of time that it takes a listener to process the data byte. Therefore, the result of the wired-OR construction of the handshake bus is that a talker is forced to wait for the slowest instrument to accept the current data before it can place a new byte of information on the bus.

3-7 GPIB OPERATION (Option 3)

The sweep generator, when equipped with Option 3, has the capability for complete front-panel-control operation over the GPIB. When used on the GPIB, the sweep generator functions as both a listener and a talker; Figure 3-26 provides a listing showing the GPIB subset functions and gives the sweep generator's capability for each function.

To provide bus control, a system of device-dependent commands (hereafter known as bus commands) and IEEE 488 Bus Messages (hereafter known as bus messages) is used. The bus commands (approximately 100 in number) are divided into the following six classes:

1. Front Panel Control Related Commands.
2. Digital Sweep Commands.
3. Group Execute Trigger Mode Commands.
4. Service Request Mode Commands.
5. Output Commands.
6. Miscellaneous Commands.

These six classes of commands are described in paragraphs 3-7.1 thru 3-7.6, respectively. The bus messages recognized by the sweep generator are discussed in paragraph 3-7.7. In addition to bus commands and bus messages, the two types of errors that can occur with bus programming are discussed in paragraph 3-7.8. The sweep generator's default-from-reset-or-turn-on states are described in paragraph 3-7.9. An alphabetical index to bus command mnemonics is provided in paragraph 3-7.10. And, a description of information supplied to provide quick reference data for GPIB programmers is given in paragraph 3-7.11.

GPIB SUBSET	FUNCTION	DESCRIPTION
AH1	Acceptor Handshake	Complete Capability
SH1	Source Handshake	Complete Capability
T6	Talker	1. Basic Talker 2. Serial Poll 3. Unaddressed if MLA 4. No Talk Only (TON)
TEØ	Talker With Address Extension	No Capability
L4	Listener	1. Basic Listener 2. Unaddressed if MTA 3. No Listen Only (LON)
LEØ	Listener With Address Extension	No Capability
SR1	Service Request	Complete Capability
RL1	Remote/Local	Complete Capability
PP1	Parallel Poll	Complete Capability
DC1	Device Clear	Complete Capability
DT1	Device Trigger	Complete Capability
CØ	Controller	No Capability

Figure 3-26. 6600 Series Sweep Generator IEEE 488 Interface Bus Subset Capability

3-7.1 GPIB Commands, Front Panel Controls

The GPIB commands used to activate front-panel-control functions are listed in Table 3-7. Programming examples that demonstrate the use of these commands are shown in Figure 3-27.

Table 3-7. 6600 Series Sweep Generator Front-Panel-Control-Related Commands

FRONT PANEL CONTROL	BUS COMMAND	NOTES
A. DATA ENTRY		
1. Parameter Entry Controls		Select the sweep generator parameter and enter the parameter's value. The decimal digits (Xs) in these commands are the parameter's value in either GHz or MHz, seconds or milliseconds, dBm or dB (see below). This value is written in the same manner that it is entered from the keyboard, i.e., either an integer or decimal number (e.g. 2 or 2.21) followed by a suitable terminator (paragraph 3-3.1). The number is not limited to two or four digits; it can be any number of digits, so long as it does not exceed the limits of the instrument.
F0	FØXXXXGH (or MH)	
F1	F1XXXXGH (or MH)	
F2	F2XXXXGH (or MH)	
M1	M1XXXXGH (or MH)	
M2	M2XXXXGH (or MH)	
ΔF	DLFXXXXGH (or MH)	
SWEEP TIME	SWTXXSEC (or MS)	
RF LEVEL	LVLXXDM (or DB)	
2. Data Terminators		Select parameter terminator (paragraph 3-2.1).
GHz	GH	
MHz	MH	
Seconds	SEC	
Milliseconds	MS	
dB	DB	
dBm	DM	
3. SHIFT	SH	Selects shifted functions (paragraph 3-3.1).
4. CLEAR ENTRY	CLR	Clears invalid (or illegal) parameter entries (paragraph 3-2.1e).
B. FREQUENCY RANGE		
1. Sweep Range Controls		Select sweep range (paragraph 3-2.2a).
FULL	FUL	
F1-F2	FF	
M1-M2	MM	
ΔF F0	DFØ	
ΔF F1	DF1	

Table 3-7. 6600 Series Sweep Generator Front-Panel-Control-Related Commands (Continued)

FRONT PANEL CONTROL	BUS COMMAND	NOTES
2. CW Frequency Select Controls		Select sweep range (paragraph 3-2.2b).
CW F0	CFØ	
CW F1	CF1	
CW F2	CF2	
CW M1	CM1	
CW M2	CM2	
3. Frequency Vernier Controls		Provide a vernier correction for the selected frequency parameter. Correction is specified in hundreds of kilohertz. Range is from +127 to -128 (paragraph 3-2.2c).
INCREASE	FVSXXXE	
DECREASE	FVS-XXXE	
OFF	FVØ	Cancels the vernier correction (paragraph 3-2.2c).
C. TRIGGER Controls		Select trigger mode (paragraph 3-3.3).
AUTO	AUT	Selects AUTO sweep.
LINE	LIN	Selects LINE sweep.
EXT OR	EXT	Selects external sweep.
SINGLE SWEEP	TRS	Triggers single sweep.
MAN	MAN	Selects manual frequency tuning. NOTE When MAN command is used, sweep tuning is accomplished using front panel control.
D. MARKERS Controls		Turn on the selected marker (paragraph 3-2.4).
VIDEO	VM1	
RF	RM1	
INTENSITY	IM1	
All Markers Off	MKØ	Turns all markers off.

Table 3-7. 6600 Series Sweep Generator Front-Panel-Control-Related Commands (Continued)

FRONT PANEL CONTROL	BUS COMMAND	NOTES
E. **LEVELING Controls**		Select the leveling source (paragraph 3-2.5).
INTERNAL	IL1	
DETECTOR	DL1	
POWER METER	PL1	
No Leveling	LVØ	Turns leveling off.
F. **RF Output Controls**		
RF OFF	RFØ	Turns RF off.
RF ON	RF1	Turns RF on.
RETRACE RF Off	RTØ	Turns RF off during retrace.
RETRACE RF On	RT1	Turns RF on during retrace (paragraph 3-3.6).
G. **POWER**	None	Ac power cannot be turned off and on over the interface bus.
H. **SELF TEST**	TST	Initiates a self-test (paragraph 3-4).
I. **RESET**	RST	Resets all parameters and controls to a predetermined (initialized) state (paragraph 3-2.7). NOTE The RST command causes the sweep generator's GPIB interface to become unaddressed. Therefore, RST should either be used alone or be the last command in a programming statement (Figure 3-27).
J. **FM OR PHASE-LOCK**		Allows external frequency modulation or phase-lock control to be applied to the sweep generator (paragraph 3-2.2d).
Off	FMØ	
On	FM1	

EXAMPLE 1

(Assumes sweep generator set to address 5)

Sweep Range: F1-F2
F1 Frequency: 5.3 GHz
F2 Frequency: 12.6 GHz

TRIGGER: LINE
RF: On
LEVELING: INTERNAL

```
10 OUTPUT 705 ;"FF F15 3GH F212
 6GH LIN RF1 IL1"
```

EXAMPLE 2

(Assumes sweep generator set to address 5)

Sweep Range: ΔF F0
F0 Frequency: 2 GHz
ΔF Frequency: 10 MHz
TRIGGER: AUTO

FM OR PHASELOCK: On
Set Vernier: -7.5 MHz
LEVELING: INTERNAL
RF: On

```
10 OUTPUT 705 ;"DF0 F02GH DLF10M
H AUT FM1 FVS-75E IL1 RF1"
```

Figure 3-27. GPIB Front-Panel-Programming Examples

3-7.2 GPIB Commands, Step Sweep

To provide a high resolution sweep over a narrow band of frequencies, the sweep generator is equipped with a digitally-stepped sweep (step sweep). This sweep, which contains 4096 discrete points, can be incrementally stepped so that any number (or all) of the discrete points can be used. The width of the step sweep and the frequency start and stop points (or center frequency for a ΔF sweep) are selected using front-panel-control command statements. (Example: FF F1XXXXGH F2XXXXGH, DFØ FØXXXXGH, DLFXXXXMH, or MM M1XXXXMH M2XXXXMH.) Because the step sweep is a frequency sweep, the following apply:

a. The front panel LED displays remain unchanged as the sweep progresses from start to stop.

b. The frequencies corresponding to the step sweep's intermediate steps must be calculated. The formula for calculating step sweep frequencies is given in Appendix 2.

The step sweep comands are given in Table 3-8.

Table 3-8. 6600 Series Sweep Generator Digital Sweep Commands

NAME	COMMAND	FUNCTION
Step Sweep	STP	Selects the Step Sweep mode of operation.
Step Select	STSXXXXE	Selects the increment point at which the Step Sweep starts. This sweep start can be any point from 0 to 4095. Zero is the usual starting point, in which case STSØE (or STSE) is the command to use.

Table 3-8. 6600 Series Sweep Generator Step Sweep Commands (Continued)

NAME	COMMAND	FUNCTION
Increment Size	SIZXXXXE	Selects the number of steps by which the Step Sweep is to be incremented when an "N" command (see below) is received. Also, selects the number of steps in which an "UP" or "DN" command (Table 3-12) will increment the selected parameter (paragraph 3-2.1a). The Xs in this command represent digits. A maximum of 4 and a minimum of 0 digits may be used. The number that is formed by the digits must be an integer. If a fractional number is used, any digits that appear to the right of the decimal point are ignored. (Example: SIZ146E and SIZ146.5E are equivalent commands.)
Go to Next Step	N	Increments the Step Sweep by the number of steps programmed, using the Increment Size Command. The following is an example of the syntax required to implement a step sweep that starts at 0 volts, has an increment size of 819 steps, and takes data at 5 discrete frequency points: 1Ø OUTPUT 7Ø5;* "STP STSE SIZ819E" 2Ø FOR I = Ø TO 4 3Ø • 4Ø • Input Statements, etc. 5Ø • 6Ø OUTPUT 7Ø5; "N" 7Ø NEXT I *Assumes sweep generator address is 5.

3-7.3 GPIB Commands, Group Execute Trigger Modes

To speed up bus operations, the Group Execute Trigger (GET) bus message can be used to increment or decrement frequency, sweep time, or output-power level. The GET bus message can also be used to increment or decrement the step sweep. The bus commands that configure the sweep generator for this increase/decrease response to a GET bus message are listed in Table 3-9.

Table 3-9. 6600 Series Sweep Generator Group Execute Trigger (GET) Mode Commands

NAME	COMMAND	FUNCTION
Trigger Single Sweep	GTS	Configures the sweep generator to execute a single sweep each time a GET bus message is received. This is the default mode, i.e., the mode assumed when no GET Mode command is programmed.
Increment-Selected Parameter	GTU	Configures the sweep generator to execute an "UP" command (Table 3-12) each time a GET bus message is received.
Decrement-Selected Parameter	GTD	Configures the sweep generator to execute a "DN" command (Table 3-12) each time a GET bus message is received.
Go to Next Step	GTN	Configures the sweep generator to execute an "N" command (Table 3-8) each time a GET bus message is received.

3-7.4 GPIB Commands, Service Request Modes

To notify the controller that certain conditions exist (such as end-of-sweep, marker encountered, unleveled, and error entry), the sweep generator uses the GPIB Service Request function. To use this function, the sweep generator employs a system of Service Request mode commands; these commands are described in Table 3-10.

Table 3-10. 6600 Series Sweep Generator Service Request (SRQ) Commands

NAME	COMMAND	FUNCTION
Enable SRQ Capability	SQ1	Enables the SRQ mode commands (below) to request service from the controller.
Disable SRQ Capability	SQØ	Disables the SRQ function. This is the default mode, i.e., the mode assumed when neither SQ1 nor SQØ is programmed.
Dwell-at-Marker Mode:		
On	DW1	Activates the dwell-at-marker mode. In this mode, when an intensity marker is encountered, the frequency sweep will dwell at the marker until a Continue Sweep (CNT) command is received. When DW1 and SQ1 are

Table 3-10. 6600 Series Sweep Generator Service Request (SRQ) Commands (Continued)

NAME	COMMAND	FUNCTION
Dwell-at-Marker Mode (continued):		both programmed, the SRQ line is pulled LOW (true), and Status Byte (Figure 3-28) bits 0 and 6 are set HIGH (decimal 65). When DW1 and SQØ are both programmed, only the Status Byte is generated; the SRQ line is not activated.
Off	DWØ	Deactivates the dwell-at-marker mode. This is the default mode, i.e., the mode assumed when neither DW1 nor DWØ is programmed.
End-of-Sweep Mode:		
On	ES1	Activates the end-of-sweep mode. When ES1 and SQ1 are both programmed, the ending of the frequency sweep causes the SRQ line to be pulled LOW (true) and Status Byte bits 1 and 6 to be set HIGH (decimal 66). When ES1 and SQØ are both programmed, only the Status Byte is generated; the SRQ line is not activated.
Off	ESØ	Deactivates end-of-sweep mode. This is the default mode, i.e., the mode assumed when neither ES1 nor ESØ is programmed.
Unleveled Condition Mode:		
On	UL1	Activates the unleveled-condition mode. When UL1 and SQ1 are both programmed, an unleveled output-power condition causes the SRQ line to be pulled LOW (true) and Status Byte bits 2 and 6 to be set HIGH (decimal 68). When UL1 and SQØ are both programmed, only the Status Byte is generated; the SRQ line is not activated.
Off	ULØ	Deactivates the unleveled condition mode. This is the default mode; i.e., the mode assumed when neither ULØ nor UL1 is programmed.
Parameter-Entry Error Mode:		
On	PE1	Activates the parameter-entry error mode. When PE1 and SQ1 are both programmed, a parameter-entry error (paragraph 3-7.7) causes the SRQ line to be pulled LOW (true) and Status Byte bits 4 and 6 to be set HIGH (decimal 80). When PE1 and SQØ are both programmed, only the Status Byte is generated; the SRQ line is not activated.

Table 3-10. 6600 Series Sweep Generator Service Request (SRQ) Commands (Continued)

NAME	COMMAND	FUNCTION
Parameter-Entry Error Mode: (continued):		
Off	PEØ	Deactivates the parameter-entry error mode. This is the default mode; i.e., the mode assumed when neither PEØ nor PE1 is programmed.
Syntax Error Mode:		
On	SE1	Activates the syntax error mode. When SE1 and SQ1 are both programmed, a syntax error (paragraph 3-7.8) causes the SRQ line to be pulled LOW (true) and Status Byte bits 5 and 6 to be set HIGH (decimal 96). When SE1 and SQØ are both programmed, only the Status Byte is generated; the SRQ line is not activated.
Off	SEØ	Deactivates the syntax error mode. This is the default mode, i.e., the mode assumed when neither SEØ nor SE1 is programmed.

STATUS BYTE BITS

7	6	5	4	3	2	1	0

Bits 3 and 7 are not used by the sweep generator.

Bit 6 is the request service bit. This bit is set HIGH when certain conditions, as shown below, exist.

Bits 0, 1, 2, 4, and 5 are combined with the service request bit to provide a code number that tells the controller which condition exists. The condition codes are given below.

Bit 6 & Ø set HIGH: An intensity marker was encountered.

Bit 6 & 1 set HIGH: The frequency sweep has ended.

Bit 6 & 2 set HIGH: An unleveled RF output condition has been detected.

Bit 6 & 4 set HIGH: An invalid parameter was entered.

Bit 6 & 5 set HIGH: A syntax error has been detected.

NOTE

The Status Byte is explained under "Serial Poll Operation" in Table 3-13.

Figure 3-28. Sweep Generator Status Byte Coding

3-7.5 GPIB Commands, Output

To provide equipment identification and parameter information upon request, the sweep generator is equipped with output commands. The use of these commands causes the sweep generator to output the requested information when next addressed to talk. These output commands are given in Table 3-11.

Table 3-11. 6600 Series Sweep Generator Output Commands

NAME	COMMAND	FUNCTION
Identify Instrument	OI	Causes the sweep generator to identify itself by sending certain parameter information over the bus. This parameter information consists of model number, low-end frequency, high-end frequency, minimum output-power level, maximum output-power level, and software revision number. This command can be used to send parameter information to the controller automatically, thus relieving the operator from having to input the information manually. The format in which the OI data is returned is shown below. Number of Bytes: 4	5	5	6	4	4 Data: 6647	00.01	18.60	-071.0	10.1	01.1 6647 — Model Number 00.01 — Low-end frequency, in GHz 18.60 — High-end frequency, in GHz -071.0 — Minimum RF output power, in dBm 10.1 — Maximum RF output power, in dBm 01.1 — Software revision no.
Output ΔF Parameter	ODF	Returns the value of the ΔF frequency parameter to the controller, value is given in MHz.
Output FØ Parameter	OFØ	Returns the value of the FØ frequency parameter to the controller. Value is given in MHz.
Output F1 Parameter	OF1	Returns the F1 frequency value, as described above.
Output F2 Parameter	OF2	Returns the F2 frequency value, as described above.

Table 3-11. 6600 Series Sweep Generator Output Commands (Continued)

NAME	COMMAND	FUNCTION
Output F_{low}	OFL	Returns the low-end frequency value, as described above.
Output F_{high}	OFH	Returns the high-end frequency value, as described above.
Output M1 Parameter	OM1	Returns the M1 frequency value, as described above.
Output M2 Parameter	OM2	Returns the M2 frequency value, as described above.
Output Power Level	OLV	Returns the output-power level value to the controller. Value is given in ±0.1dB increments.
Output Status Byte	OSB	Returns the Status Byte (Figure 3-28) to the controller.
Output Sweep Time	OST	Returns the sweep time value to the controller. Value is given in milliseconds.

3-7.6 GPIB Commands, Miscellaneous

There are 9 GPIB commands unrelated to either front-panel, digital-sweep, GET-mode, SRQ-mode or output operation. These miscellaneous commands are described in Table 3-12.

Table 3-12. 6600 Series Sweep Generator Miscellaneous Commands

NAME	COMMAND	FUNCTION
Continue Sweep	CNT	Causes the sweep to continue after having dwelled at an intensity marker. CNT is used in conjunction with the SRQ Dwell-at-Marker Mode.
Front Panel Displays:		
Off	DSØ	Turns off the front panel numeric displays so that unauthorized personnel cannot read the frequency range currently in use.
On	DS1	Turns the front panel numeric displays on. This is the default, or unprogrammed, condition (paragraph 3-7.9).

Table 3-12. 6600 Series Sweep Generator Miscellaneous Commands (Continued)

NAME	COMMAND	FUNCTION
Decrement the Selected Parameter	DN	Decrements the selected frequency, sweep time, or RF level parameter by the number of steps programmed with the Increment Size command (SIZ). For DN to be effective, the selected parameter must still be active. That is, the selected parameter's command statement (F1XXXXGH, SWTXXMS, LVLXXDM, etc.) must be the last command to appear before DN is commanded. A non-parameter command, such as AUT, IL1, or VM1, cannot be sandwiched between the parameter mnemonic and the DN command. If necessary, insure that the selected parameter is still active by prefacing DN (or a string of DNs) with the selected parameter's mnemonic. For example, send F1 DN (or DN DN DN etc.) rather than just DN (or DN DN DN etc.).
Increment the Selected Parameter	UP	Increments the selected frequency, sweep time, or RF level parameter by the number of steps programmed with the Increment Size command (SIZ). As described for the DN command, above, the selected parameter must still be active for UP to be effective.
CW Filter:		
Off	FLØ	Causes the CW filter to be out of the RF output signal line.
On	FL1	Inserts a CW filter in the RF output signal line. This command overrides the CW filter control inherent in front-panel programming (i.e., CW filter inserted for sweep widths 50 MHz and below and not inserted for sweep widths above 50 MHz).
Return to Local	RL	Causes the sweep generator to return to local (front panel) control, provided that a local lockout message (Table 3-13) is not in effect.
Recall the Front Panel Control Settings	RCL	Causes the sweep generator to be reconfigured with the front-panel-control settings that were previously saved using the SAV command (below). Figure 3-29 provides a programming example.
Horizontal Output During CW (rear panel switch)		
OFF ON	CS0 CS1	Refer to Figure 3-20, item 6.

Table 3-12. 6600 Series Sweep Generator Miscellaneous Commands (Continued)

NAME	COMMAND	FUNCTION
Reset Sweep	RSS	Resets the frequency sweep to the sweep-start frequency, as programmed by a Parameter Entry command (e.g. FFF1XXXXGH). RSS can be used to abort the sweep currently in progress prior to sending a trigger command.
Save the Front Panel Control Settings	SAV	Causes the sweep generator to return an ASCII encoded representation of the entire instrument setup. This instrument setup information is contained in a data string approximately 310 bytes long. The SAV command can be used to store the front-panel-control settings for a measurement test setup. This test setup information can be stored on a program tape for future use. Figure 3-29 provides a programming example.

Example 1 - Print SAV information (GPIB address assumed to be 5).

```
10 DIM A$[350]
20 OUTPUT 705 ,"SAV"
30 ENTER 705 , A$
40 PRINT A$

[illegible]
E@E@EG[illegible]BA@I@L@LJOCE@
L@L@L[illegible]@L@L[illegible]
[illegible]IA@LOO@C@LE[illegible]
LOO@C@LIU@LIO@@BH@L@L@@@@@@@@@@@
@@@@@@@@@@@@@@@@@@@@ADI D@@@GM@@@@
@@J@@CHCH@@@@@J@@@@@J@@@@BH@@@@C
B@@@@@J@@DH JHANBHEI DCDF JGNDCEFAG
O@@CE[illegible]SCG[illegible]@@@LHE@II I H@CEH@H
@H@H@@@E JEJ@EECBA@AME
```

Line 10 - dimension A$ to accomodate 350 bytes of data.

Line 20 - address sweep generator to listen and send SAV command.

Line 30 - address sweep generator to talk and input SAV command data into A$.

Line 40 - print information contained in A$.

Encoded ASCII-data bytes representing the binary data contained in the front panel control RAM memories.

Example 2 - Record SAV information into a tape file.

```
10 DIM A$[350]
20 OUTPUT 705 ,"SAV"
30 ENTER 705 , A$
40 CREATE "filename",3
50 ASSIGN# 1 TO "filename"
60 PRINT# 1 , A$
70 ASSIGN# 1 TO *
```

Line 10 -
Line 20 - see Example 1 above.
Line 30 -

Line 40 - create a tape file and make it 3 records long.

Line 50 - assign the tape file to buffer #1.

Line 60 - print the data contained in file #1.

Line 70 - close file #1.

Example 3 - Recall SAV information from tape file.

```
10 DIM A$[350]
20 ASSIGN# 1 TO "filename"
30 READ# 1 , A$
40 ASSIGN# 1 TO *
50 OUTPUT 705 ,"RCL",A$
```

Line 10 - see Examples 1 and 2 above.

Line 20 - see Line 50, Example 2 above.

Line 30 - load data from file #1 into A$.

Line 40 - close file #1.

Line 50 - address sweep generator to listen; send both RCL command and data contained in A$.

Figure 3-29. Programming Examples Using SAV and RCL Commands

3-7.7 Bus Messages

The 6600 Series Sweep Generators recognize most of the IEEE 488 bus messages. A listing of the recognized bus messages, including specific information describing how the messages are used, is given in Table 3-13. Sample program statements showing how the WILTRON 85/HP9845A, HP 9825A, and Tektronix 4051/4052 bus controllers implement the recognized bus messages are shown in Table 3-14.

Table 3-13. Bus Messages Recognized by the 6600 Series Sweep Generators

BUS MESSAGE	HOW MESSAGE IS USED BY SWEEP GENERATOR
Device Clear	1. Aborts all current sweep generator GPIB activities. 2. Resets the STS, SIZ, SQ1, DW1, UL1, ES1, EF, and EI commands to their default condition (paragraph 3-7.9).
Go to Local	Returns the sweep generator to local control.
Group Execute Trigger	1. Triggers a new sweep if the EXT (Table 3-7) and the GTS (Table 3-9) commands are both programmed. 2. Increments the selected parameter (paragraph 3-2.1a) by the number of steps programmed using the SIZ command (Table 3-8) if the GTU command (Table 3-9) is programmed. 3. Decrements the selected parameter by the number of steps programmed using the SIZ command if the GTD command (Table 3-9) is programmed. 4. Increments the digital sweep by the number of steps programmed using the SIZ command if the GTN command (Table 3-9) is programmed.
Interface Clear	Stops the sweep generator GPIB interface from listening or talking. The front panel controls are not cleared.
Local Lockout	Prevents the RETURN TO LOCAL pushbutton or the RL command (Table 3-12) from returning the sweep generator to local control.
Remote Enable	Places the sweep generator under remote control if the REM line is TRUE and the sweep generator is addressed to listen. If placed in remote and not supplied with program data, sweep generator operation is determined by the position in which the front panel controls were set immediately prior to going remote.
Service Request (SRQ) Messages:	The sweep generator is equipped with SRQ capability. It will respond to both serial- and parallel-poll messages. Serial- and parallel-poll operations are described below.

Table 3-13. Bus Messages Recognized by the 6600 Series Sweep Generators (Continued)

BUS MESSAGE	HOW MESSAGE IS USED BY SWEEP GENERATOR
Serial-Poll Enable (SPE) Serial-Poll Disable (SPD)	<u>Serial Poll Operation</u> The SPE message causes the sweep generator to respond with a decimally-coded status byte (Figure 3-28). This status byte is coded to give the controller two pieces of information: 1. Whether it was the device requesting service. 2. If it was the service-requesting device, the type of service that it needs. The SPD message, which is sent by the controller in response to receiving a status byte, terminates serial-poll operation.
Parallel-Poll Configure (PPC) Parallel-Poll Enable (PPE) Parallel-Poll Unconfigure (PPU) Parallel-Poll Disable (PPD)	<u>Parallel-Poll Operation</u> When queried by a parallel-poll message command (PPOLL or pol; see Table 3-14), the sweep generator (if configured for parallel-poll operation; see below) responds by setting its assigned data bus line to the logical state (1, 0) that indicates its correct SRQ status. To configure a bus device that is (1) built for parallel-poll operation and (2) designed to be remotely configured on the bus, the controller sends a two-byte parallel-poll configure and enable (PPC and PPE) message. The PPC byte configures the device to respond to a parallel-poll message such as PPOLL or pol. The PPE byte assigns the logical sense (1, 0) that the parallel-poll response will take. When the sweep generator receives the PPC/PPE message, it configures itself to properly respond to the parallel-poll message. The PPU (or PPD) message is sent by the controller when a parallel-poll response is no longer desired. This message causes the sweep generator to become unconfigured for parallel-poll response.

Table 3-14. Sample Bus Message Statements

BUS MESSAGE	SAMPLE STATEMENT SHOWING HOW MESSAGE IS IMPLEMENTED		
	MODELS 85/9845A	HP 9825	TEKTRONIX 4051
Go to Local (GTL)	LOCAL 7[1] LOCAL 705[2]	lcl 7[1] lcl 705[2]	WBYTE Ω 95, 63, 37, 4:[2]
Group Execute Trigger (GET)	TRIGGER 7 TRIGGER 705	trg 7 trg 705	WBYTE Ω 95, 63, 37, 8:[2]
Interface Clear (IFC)	ABORTIO 7 ABORTIO 705	cli 7 cli 705	
Local Lockout (LLO)	LOCAL LOCKOUT 7	llo 7	WBYTE Ω 17:[1]
Remote Enable	REMOTE 7 REMOTE 705	rem 7 rem 705	PRINT Ω 5[2]
Serial Poll (Query Message)	SPOLL (7) SPOLL (705)	rds (7)→A: if bit (7, A); gto (Line No.)	POLL A, B; 5[2]
Parallel Poll (Query Message)	PPOLL (7)	pol(7)→A: if bit (0, A) = 1; gsb "Serv 0": if bit (1, A) = 1; gsb "Serv 1"	
Parallel Poll Configure (PPC) (The statements assign the sweep generator data line DIO5 for parallel-poll response with Sense (S) = 0.)	MODEL 85 ONLY: SEND 7; LISTEN 5 CMD 3 SCG 5 UNL HP 9845 ONLY: PPOLL CONFIGURE 705; 5	polc 705, 5[2]	

[1] Sends message to all bus instruments.
[2] Sends message to instrument at address 5 (sweep generator).

Table 3-14. Sample Bus Message Statements (Continued)

BUS MESSAGE	SAMPLE STATEMENT SHOWING HOW MESSAGE IS IMPLEMENTED		
	MODEL 85/9845	HP 9825	TEKTRONIX 4051
Parallel Poll Unconfigure (PPU)	MODEL 85 ONLY: SEND 7; LISTEN 5 CMD 21 HP 9845 ONLY: PPOLL UNCONFIGURE 705	polu 7 polu 705	
Device Clear (DC and SDC)	MODEL 85 ONLY: CLEAR 7 CLEAR 705 HP 9845 ONLY: RESET 7 RESET 705	clr 7 clr 705	INIT[1] WBYTE Ω 95, 63, 37, 4:[2]

[1] Sends message to all bus instruments.
[2] Sends message to instrument at address 5 (sweep generator).

3-7.8 Program Errors

There are two types of errors that occur in bus programming: invalid-parameter errors and syntax errors. These two error types are described below.

a. Invalid-Parameter Error. Invalid-parameter errors are those that will cause either the front panel CLEAR ENTRY, F1>F2 OR M1>M2 CHANGE FREQ SETTING, or GHz/dBm/Sec and MHz/dB/mS indicators to flash. These errors include:

1. Programming a frequency sweep where F1 is greater than F2 or M1 is greater than M2 (backward sweep, paragraph 3-2.1e).

2. Attempting to enter a frequency, sweep-time, or RF level parameter that exceeds the limits of the sweep generator.

3. Failing to properly end a parameter entry with a suitable terminator, such as MH, DB, MS, etc.

Invalid-parameter errors cause the front-panel indicators to flash.

b. Syntax Errors. Syntax errors are errors that occur in the formulation of a program statement, such as writing "EXTTFS" instead of "EXTTRS". To prevent misinterpretation of command statements, the sweep generator ignores all portions of the command statement following the syntax error. All commands are ignored until the sweep generator receives the Unlisten command (ASCII ?) over the bus or until the sweep generator is addressed to talk. An example showing how the sweep generator evaluates a syntax error is given in Figure 3-30.

Correctly-written program statement commanding external sweep, trigger sweep, and RF marker (sweep generator assumed to be set to address 5):

```
10 OUTPUT 7Ø5; "EXTTRSRM1"
```

Same program statement with syntax error.

```
10 OUTPUT 7Ø5; "EXTTFSRM1"
                    └─ error
```

This portion of the program statement, plus all future statements, is ignored until sweep generator receives the Unlisten (UNL) command (ASCII ?). The Unlisten Command is normally sent over the bus either (1) immediately prior to the next time the sweep generator is addressed (HP 9825 or Model 85, see below) or (2) immediately after the last data byte of the current data transaction has been received (TEK 4051 and PET 2001).

Program Format, HP 9825A and Model 85

1st Data Transaction	2nd Data Transaction
UNLISTEN, LIST ADDR, D, A, T, A	UNLISTEN, LIST ADDR, D, A, T, A

Program Format, TEK 4051 & PET 2001

1st Data Transaction	2nd Data Transaction
LIST ADDR, D, A, T, A, UNLISTEN	LIST ADDR, D, A, T, A, UNLISTEN

Figure 3-30. Program Statement with Syntax Error (Example)

3-7.9 Reset Programming and Default Conditions

Reset programming provides the means for quickly returning the sweep generator to its default, or preprogrammed, operational state. In the manual (local) mode. the default state can be entered into only by pressing the RESET pushbutton. In the GPIB (remote) mode, however, there are several ways in which to enter the default state. These reset-programming methods, along with related data, are given in Table 3-15. The default settings for the numeric frequency, sweep time, and output power level parameters are given in Table 3-16. And the recommended command sequence for reset programming is given in Figure 3-31. The use of this recommended command sequence assures that all parameters and commands assume their preprogrammed state each time reset is desired.

Line #	Purpose
10	Sends Device Clear Bus Message. This message clears the sweep generator GPIB interface.
20	Sends Reset Bus Command. This command resets the sweep generator front panel controls to a predetermined (initialized) state.
30	Sends new front panel settings: full sweep, internal leveling, and output-power level of 0 dBm.

```
10 CLEAR 705
20 OUTPUT 705 ,"RST"
30 OUTPUT 705 ,"FUL IL1 LVL0DM"
```

Figure 3-31. Reset Programming Statements

Table 3-15. Resetting the Sweep Generator GPIB Interface Circuits

METHODS OF RESETTING GPIB INTERFACE CIRCUITS	FUNCTIONS AFFECTED	DEFAULT CONDITION
1. Pressing RETURN TO LOCAL pushbutton.	Digital Sweep	STS = Ø SIZ = Ø
	Service Request Modes	SQØ DWØ ULØ ESØ
	Group Execute Trigger Mode	GTS
	Bus Messages	Local

Table 3-15. Resetting the Sweep Generator GPIB Interface Circuits (Continued)

METHODS OF RESETTING GPIB INTERFACE CIRCUITS	FUNCTIONS AFFECTED	DEFAULT CONDITION
2. Pressing RESET pushbutton.	Same as above.	Same as above, plus local and local lockout messages are also reset.
3. Sending RST command over the bus.	Same as above.	Same as 2, above.
4. Executing the interface message Device Clear.	Same as above.	Same as 1, above, except local bus message is not reset.
5. Turning the POWER switch on and off.	Same as above	Same as 2, above.

Table 3-16. Default Settings for Numeric Parameters

NUMERIC PARAMETER		DEFAULT SETTING
1. Frequency:	F0	10 GHz
	F1	2 GHz (Models 6637 & 6638), 10 MHz (Models 6647 & 6648)
	F2	18 GHz
	M1	3 GHz (Models 6637 & 6638), 1 GHz (Models 6647 & 6648)
	M2	17 GHz
2. ΔF Sweep Width		1 GHz
3. Sweep Time		50 ms
4. Output Power Level		+10 dBm

3-7.10 Index of Sweep Generator GPIB Command Codes

An alphabetical index of the sweep generator GPIB command codes is given in Table 3-17. This table lists the command mnemonic, the name of the command, and the table number where the command is described.

Table 3-17. Index of Sweep Generator GPIB Command Mnemonics

MNEMONIC	NAME	TABLE NO.
AUT	Auto Trigger	3-7
CFØ	CW Select FØ	3-7
CF1	CW Select F1	3-7
CF2	CW Select F2	3-7
CLR	Clear Keypad	3-7
CM1	CW Select M1	3-7
CM2	CW Select M2	3-7
CNT	Continue Sweep	3-12
CS0	Horizontal Output Off During CW Operation	3-12
CS1	Horizontal Output On During CW Operation	3-12
DB	dB Data Terminator	3-7
DFØ	Sweep Range ΔF F0	3-7
DF1	Sweep Range ΔF F1	3-7
DL1	Detector Leveling	3-7
DLF	Enter ΔF Frequency	3-7
DM	dBm Data Terminator	3-7
DN	Decrement Selected Parameter	3-12
DSØ	Front Panel Displays Off	3-12
DS1	Front Panel Displays On	3-12
DWØ	Dwell at Marker Mode Off	3-10
DW1	Dwell at Marker Mode On	3-10
ESØ	End of Sweep Mode Off	3-10
ES1	End of Sweep Mode On	3-10
EXT	External Trigger	3-7
FØ	Enter Parameter FØ	3-7
F1	Enter Parameter F1	3-7
F2	Enter Parameter F2	3-7
FF	Sweep Range F1-F2	3-7
FLØ	CW Filter Off	3-12
FL1	CW Filter On	3-12
FMØ	Frequency Modulation Off	3-7

MNEMONIC	NAME	TABLE NO.
FM1	Frequency Modulation On	3-7
FUL	Sweep Range Full	3-7
FVØ	Frequency Vernier Off	3-7
FVS	Set Frequency Vernier	3-7
GH	GHz Data Terminator	3-7
GTD	GET* Mode Execute "DN" Command	3-9
GTN	GET Mode Execute "N" Command	3-9
GTS	GET Mode Trigger Sweep	3-9
GTU	GET Mode Execute "UP" Command	3-9
IL1	Internal Leveling	3-7
IM1	Intensity Marker	3-7
LIN	Line Trigger	3-7
LVØ	Leveling Off	3-7
LVL	Enter Level Parameter	3-7
M1	Enter M1 Parameter	3-7
M2	Enter M2 Parameter	3-7
MAN	Manual Sweep	3-7
MH	MHz Data Terminator	3-7
MKØ	Markers Off	3-7
MM	Sweep Range M1-M2	3-7
MS	Millisecond Data Terminator	3-7
N	Go to Next Increment (Digital Sweep)	3-8
ODF	Output ΔF Frequency	3-11
OI	Identify Instrument	3-11
OFØ	Output FØ Frequency	3-11
OF1	Output F1 Frequency	3-11
OF2	Output F2 Frequency	3-11
OFL	Output Low-End Frequency	3-11

*Group Execute Trigger

Table 3-17. Index of Sweep Generator GPIB Command Mnemonics (Continued)

MNE-MONIC	NAME	TABLE NO.
OFH	Output High-End Frequency	3-11
OLV	Output RF Level	3-11
OM1	Output M1 Frequency	3-11
OM2	Output M2 Frequency	3-11
OSB	Output Status Byte	3-11
OST	Output Sweep Time	3-11
PEØ	Parameter Entry Error Mode Off	3-10
PE1	Parameter Entry Error Mode On	3-10
PL1	Power Meter Leveling	3-7
RCL	Recall Front Panel Setup	3-12
RFØ	RF Off	3-7
RF1	RF On	3-7
RL	Return to Local	3-12
RM1	RF Marker On	3-7
RSS	Reset Sweep	3-12
RST	Reset Front Panel	3-7
RTØ	RF During Retrace Off	3-7
RT1	RF During Retrace On	3-7
SAV	Save Front Panel Setup	3-12
SEØ	Syntax Error Mode Off	3-10
SE1	Syntax Error Mode On	3-10
SEC	Seconds Data Terminator	3-7
SH	Shift	3-7
SIZ	Increment Size	3-8
SQØ	SRQ Mode Off	3-10
SQ1	SRQ Mode On	3-10
STP	Step Sweep	3-8
STS	Step Select	3-8
SWT	Enter Sweep Time Parameter	3-7
TRS	Trigger Sweep	3-7
TST	Self Test	3-7
ULØ	Unleveled Condition Mode Off	3-10
UL1	Unleveled Condition Mode On	3-10
UP	Increment Selected Parameter	3-12
VM1	Video Marker On	3-7

3-7.11 Quick Reference Data

An alphbetical index of sweep generator GPIB command codes, along with a tabulation of default data, is provided in Appendix 1. This appendix may be copied and used as a handy source for the quick reference of certain GPIB programming data.

Table 4-1. Recommended Test Equipment for Performance Verification and Calibration

INSTRUMENT	REQUIRED CHARACTERISTICS	RECOMMENDED MANUFACTURER
Digital Multimeter	DC Volts: .05% to 30V, .002% to 10V. 5-1/2 digit resolution.	Keithley Model 191
Oscilloscope	60 MHz bandwidth. 1mV sensitivity.	Tektronix 5440/5A481/5B42
Function Generator	300mV to 5V output. 10 kHz square wave. 28 kHz square wave. 10 kHz sine wave.	Interstate Elect. Co. (IEC) Model F-77
Microwave Counter	10 MHz to 20 GHz range. 0.25 MHz accuracy.	EIP Model 548
RF Power Meter	10 MHz to 20 GHz freq. range. +13 dBm measurement capability.	HP 435A
Spectrum Analyzer	60 dB power range. 10 MHz to 20 GHz freq. range. IF output. 50 dB signal-to-noise ratio, .01 to 2 GHz.	HP 8565A
Modulation Meter	15 kHz bandwidth. 1 kHz sensitivity.	Marconi TF2304
True RMS Voltmeter	-60 dB sensitivity. 10 kHz bandwidth.	Fluke 8921A
Adjustable AC Line Transformer (Variac)	100/120V line voltage. 220/240V line voltage	General Radio W5MTB, General Radio W10HM73
Line Voltage Monitor	120V line voltage. 240V line voltage.	RCA 120B RCA WV 503A
RF Detector	Frequency range: .01 to 18.5 GHz.	WILTRON Model 75N50

SECTION IV

PERFORMANCE VERIFICATION

4-1 INTRODUCTION

This section contains the performance verification procedures, which are organized as follows:

Para.	Test
4-3	FREQUENCY ACCURACY
4-4	SWEEP TIME
4-5	OUTPUT POWER
4-6	RESIDUAL AM
4-7	RESIDUAL FM
4-8	EXTERNAL FM AND PHASE LOCK
4-9	RF OUTPUT SIGNAL

4-2 RECOMMENDED TEST EQUIPMENT

A listing of the test equipment required for performance verification and for calibration (Section V) is given in Table 4-1 (facing page).

4-3 FREQUENCY ACCURACY TESTS

To verify the sweep generator's frequency accuracy, perform the steps in subparagraphs a. thru c. below. If any of the frequencies are found to be out of tolerance, perform the A5 Frequency Instruction adjustments in paragraph 5-6 and the applicable Frequency Calibration adjustments in paragraph 5-11.

a. CW Frequency Accuracy

1. Connect test equipment as shown in Figure 4-1, and turn the equipment on.

2. Press RESET on sweep generator (sweeper).

3. Press CW F1.

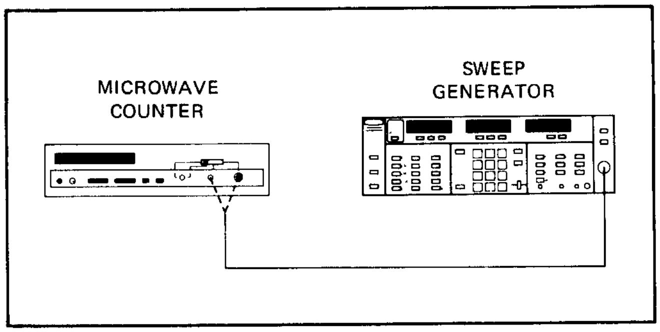


Figure 4-1. Test Equipment Setup for Frequency Accuracy Tests

4. Sequentially set F1 for the frequencies shown in Table 4-2, and verify their accuracy.

Table 4-2. CW Test Frequencies

MODEL	F1 FREQUENCY	COUNTER READING
6647/6648	0.010	0.000 - 0.020
6647/6648	1.000	0.990 - 1.010
6647/6648	1.950	1.940 - 1.960
6637/6638	2.000	1.990 - 2.010
6647/6648	2.050	2.040 - 2.060
All	3.000	2.990 - 3.010
All	4.000	3.990 - 4.010
All	5.000	4.990 - 5.010
All	6.000	5.990 - 6.010
All	7.000	6.990 - 7.010
All	7.950	7.940 - 7.960
All	8.050	8.040 - 8.060
All	9.000	8.990 - 9.010
All	10.000	9.990 - 10.010
All	11.000	10.990 - 11.010
All	12.350	12.340 - 12.360
All	13.000	12.990 - 13.010
All	14.000	13.990 - 14.010
All	15.000	14.990 - 15.010
All	16.000	15.990 - 16.010
All	17.000	16.990 - 17.010
6637/6647	18.600	18.590 - 18.610
6638/6648	19.000	18.990 - 19.010
6638/6648	20.000	19.990 - 20.010

5. Press RESET on sweeper.

6. Verify counter readings, as shown below, for other CW settings.

PARAMETER	COUNTER READING
CW F0 (all)	9.990 - 10.010
CW F2 (all)	17.990 -18.010
CW M1 (6637/6638)	2.990 -3.010
CW M1 (6647/6648)	1.990 -2.010
CW M2 (all)	16.990 -17.010

b. Sweep Frequency Accuracy Tests

1. Press FREQUENCY RANGE ΔF F0, and set ΔF for 50 MHz.

2. Press MANUAL SWEEP.

3. Rotate MANUAL SWEEP control fully counterclockwise.

4. Verify that counter reads 9975 ±15 MHz.

5. Rotate MANUAL SWEEP control fully clockwise.

6. Verify that counter reads 10025 ±15 MHz.

c. Frequency Vernier Accuracy Tests

1. Press RESET.

2. Press CW F0.

3. Record the counter's frequency readout.

4. Press FREQUENCY VERNIER OFF.

5. Press FREQUENCY VERNIER INCREASE and hold depressed for approximately 10 seconds.

6. Verify that the counter's frequency readout increased by ≥10 MHz from the frequency recorded in step 3.

7. Press FREQUENCY VERNIER OFF.

8. Press FREQUENCY VERNIER DECREASE and hold depressed for approximately 10 seconds.

9. Verify that the counter's frequency readout decreased by ≥10 MHz from the frequency recorded in step 3.

4-4 SWEEP TIME TEST

To verify the sweep generator's sweep time, perform the steps below. If the sweep time is found to be out of tolerance, perform the A2 Ramp Generator Adjustments in paragraph 5-5.

a. Connect the test equipment as shown in Figure 4-2, and turn the equipment on.

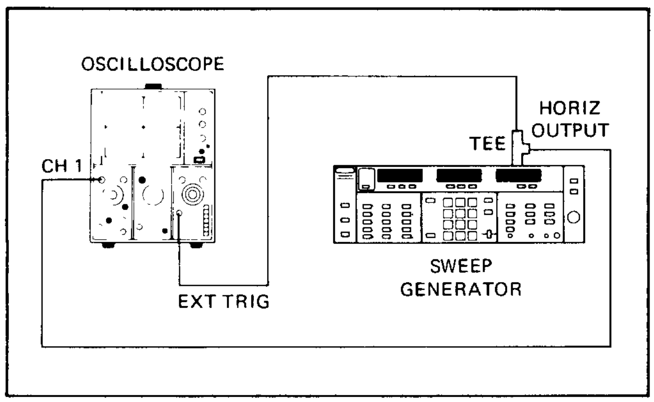


Figure 4-2. Test Equipment Setup for Sweep Time Test

b. Press RESET on sweep generator.

c. Press FREQUENCY RANGE ΔF F0.

d. Press SWEEP TIME and set for 10 ms.

e. Verify that the oscilloscope displays a

10 ms ±2.0 ms ramp, as shown in Figure 4-3.

f. Reset sweep time for 1 second.

g. Verify that the oscilloscope displays a 1 ±0.2 second ramp, as shown in Figure 4-4.

h. Reset sweep time for 10 seconds.

i. Verify that the oscilloscope displays a 10 ±2 second ramp.

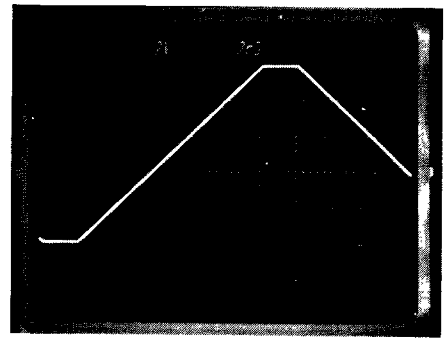


Figure 4-3. A2 Sweep Ramp, 10 ms Sweep

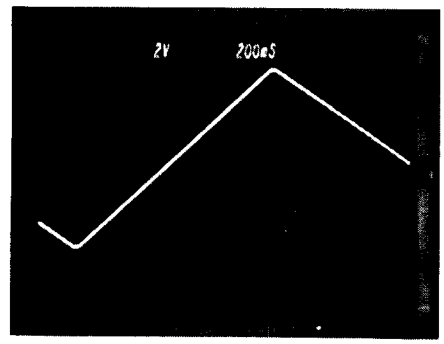
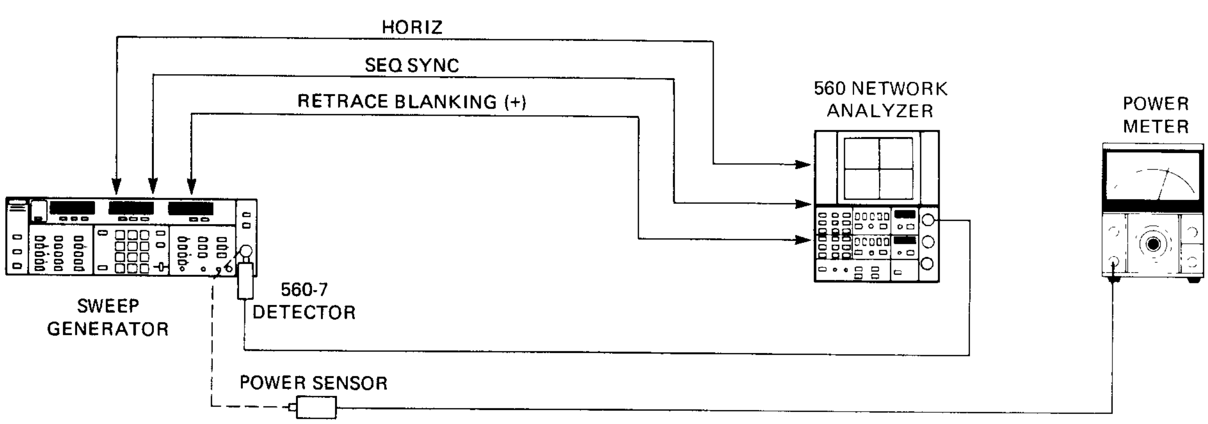


Figure 4-4. A2 Sweep Ramp, .1 s Sweep

4-5 OUTPUT POWER TESTS

To verify the sweep generator's output power level, perform the steps below. If the output power level is found to be out of tolerance, perform the ALC Calibration adjustments in paragraph 5-14.

a. Connect test equipment as shown in Figure 4-5, and turn the equipment on.



560 Control Settings

CHANNEL A ON: On
MEMORY: Off
dB PER DIVISION: 1
REFERENCE dB/dBm: dBm

REFERENCE POSITION
LOCATE: Center graticule line
OFFSET dB: 10
CHANNEL B ON: Off

REAL TIME: On
MARKERS: Off
SMOOTHING: Off

igure 4-5. Test Equipment Setup for Output Power Tests

b. Press RESET on sweep generator (sweeper).

c. Verify that the RF SLOPE control is OFF.

d. Press DETECTOR leveling.

e. On 560, adjust CHANNEL A OFFSET control to position the trace's minimum power point on the center graticule line; see Figure 4-6.

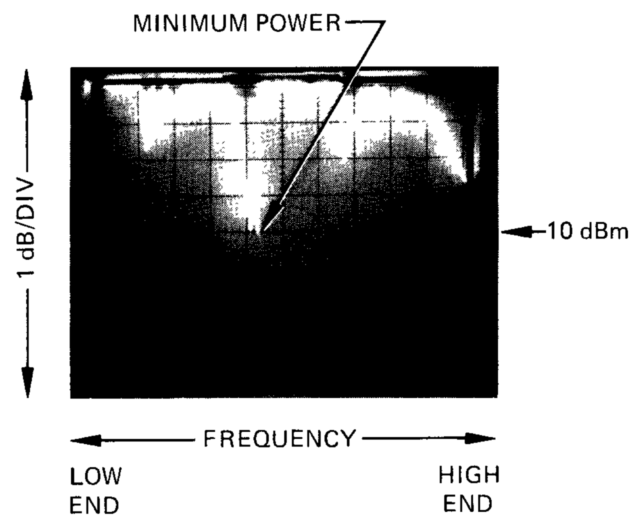


Figure 4-6. Unleveled Power

f. Verify that the OFFSET dB display reads >10.2 dBm.

g. On 560, press CHANNEL A .2 dB PER DIVISION.

h. On sweeper, press INTERNAL leveling.

i. Verify that the peak-to-peak ripple on the 560 trace is <1.8 dB; see Figure 4-7.

j. Disconnect the 560 detector from the sweeper, and connect the power sensor in its place.

k. On sweeper, press CW F0 and set F0 for 2.050 GHz.

l. Press MANUAL SWEEP.

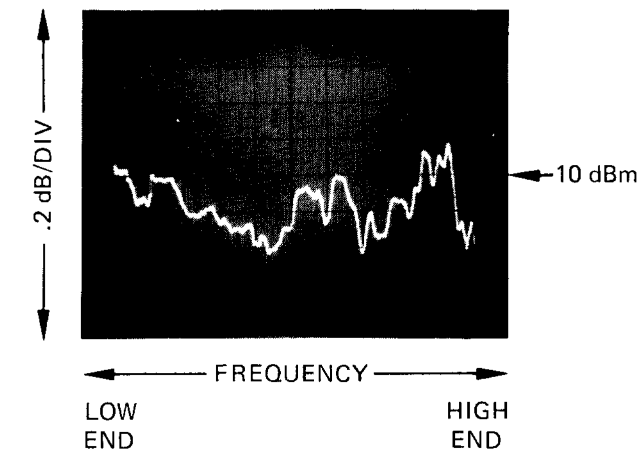


Figure 4-7. Leveled Power

m. Verify that the power meter reads 10 ±0.2 dBm.

n. On sweeper, press LEVEL and set output power for 0 dBm.

o. Verify that the power meter reads 0 ±0.2 dBm.

p. Reset sweeper for +5 dBm.

q. Verify that the power meter reads 5 ±0.2 dBm.

r. On sweeper, press F0 and set for high-end frequency.

s. Record power meter reading.

t. Rotate RF SLOPE fully clockwise.

u. Verify that the power meter reading increased by ≈3 dB.

4-6 RESIDUAL AM TEST

To verify that the residual amplitude modulation signals in the sweep generator are tolerable, perform the steps below. If the residual AM is found to be out of tolerance, contact WILTRON Customer Service.

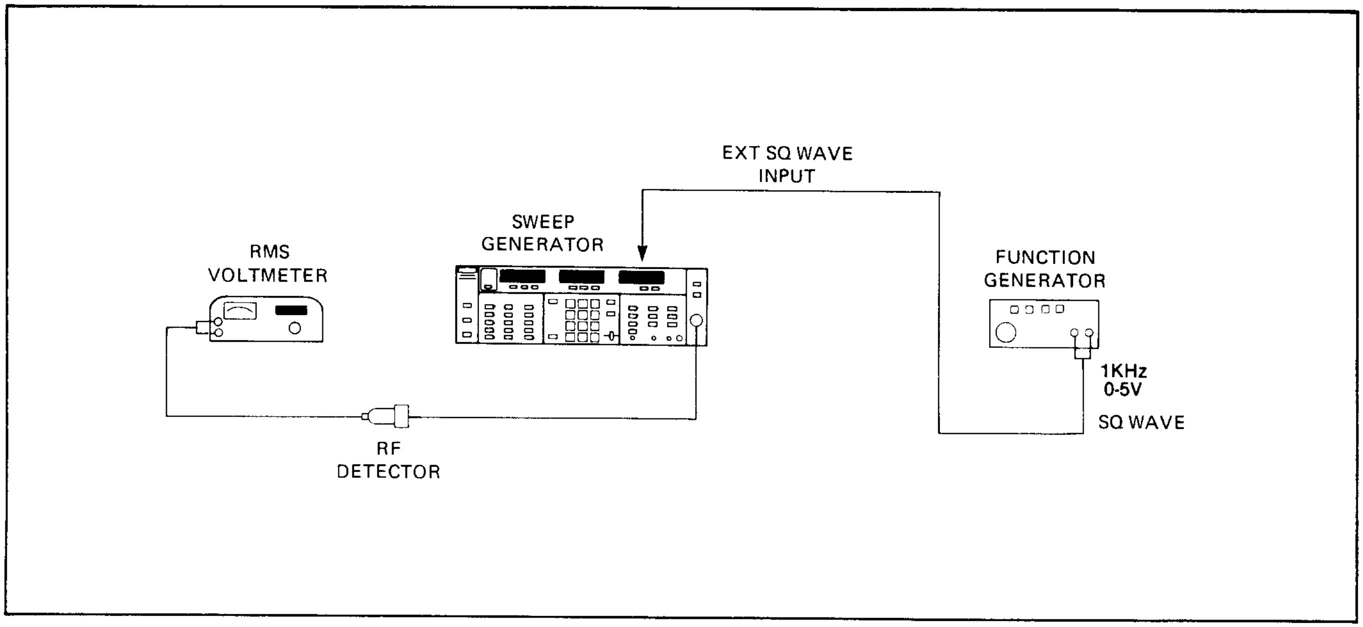


Figure 4-8. Test Equipment Setup for Residual AM Test

a. Connect test equipment as shown in Figure 4-8, and turn the equipment on.

b. Press RESET on sweep generator (sweeper).

c. Press CW F1 and set to 50 MHz (6647/6648) or 2.2 GHz (6637/6638).

d. Record RMS voltmeter reading.

e. Turn function generator off.

f. Record second RMS voltmeter reading.

g. Calculate the sweeper's residual AM per the following formula:

Residual AM (-dBc)* =

$$- \left[\left| \text{step d reading} \right| + \left| \text{step f reading} \right| + 9 \text{ dB} \right],$$

* dB below the carrier.

h. Residual AM should be less than -50 dBc.

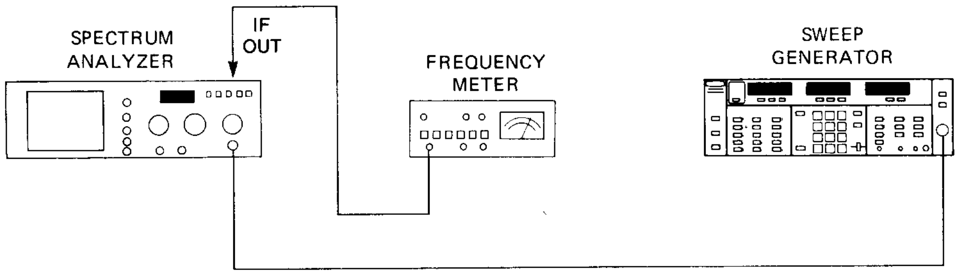
i. Turn the function generator back on.

j. Repeat steps c. thru h. for the following frequencies:

1.8 GHz (6647/6648)
2.2 GHz (all)
7.8 GHz (all)
8.2 GHz (all)
12.2 GHz (all)
12.6 GHz (all
18.6 GHz (6637/6647)
20.0 GHz (6638/6648)

4-7 RESIDUAL FM TEST

To verify that the residual frequency modulation signals in the sweep generator are tolerable, perform the steps below. If the residual FM is found to be out of tolerance, contact WILTRON Customer Service.



Control Settings

Frequency Meter

Supply: On
Deviation: X1
Other Controls:

0 dB
FM
+
5

Spectrum Analyzer

FREQUENCY BAND: .01-1.8 GHz
RESOLUTION BW: 1 MHz
REF LEVEL: 10 dBm
INPUT ATTN: 20 dB
LOG SCALE: 10 dBm/Div.
FREQUENCY: 0.050 GHz
FREQUENCY SPAN/DIV: 5 MHz
FREQ SPAN MODE: PER DIV
SWEEP SOURCE: INT
SWEEP TRIGGER: FREE RUN
SWEEP TIME/DIV: AUTO

Figure 4-9. Test Equipment Setup for Residual FM Test

a. Connect test equipment as shown in Figure 4-9, and turn the equipment on.

b. On sweep generator, press CW F0 and set for 50 MHz.

c. On spectrum analyzer, adjust the TUNING control to center the sweeper's fundamental frequency on the display's CENTER FREQUENCY graticule line; see Figure 4-10.

d. On spectrum analyzer,

1. press ZERO SPAN and

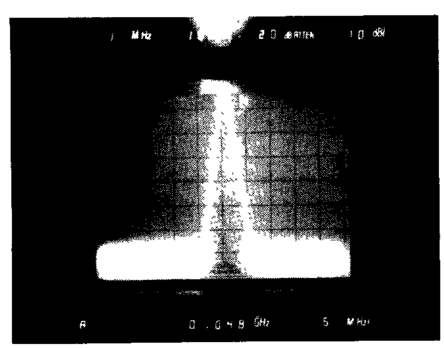


Figure 4-10. Fundamental Frequency, Spectrum Analyzer Display

2. adjust the TUNING control to place the trace at the top of the display; see Figure 4-11.

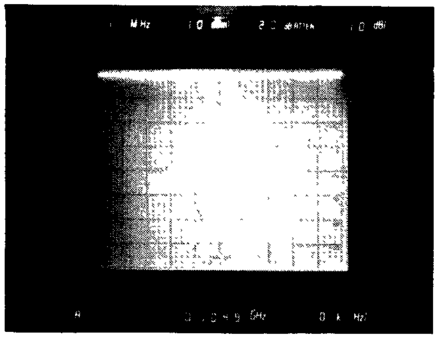


Figure 4-11. Spectrum Analyzer ZERO SPAN Display

e. Verify that the frequency meter reads <10 kHz peak.

f. On spectrum analyzer, reset FREQ SPAN MODE to PER DIV.

g. Refer to Table 4-3 and repeat steps c. thru f. for frequencies 1.8 thru 20 GHz, as applicable.

NOTE

On the spectrum analyzer, change the FREQUENCY BAND settings as necessary to observe the sweeper's fundamental frequency.

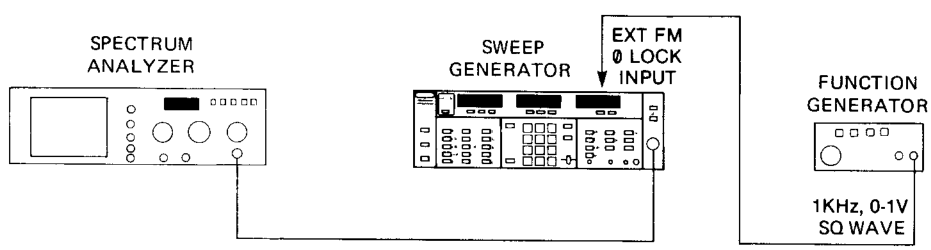
Table 4-3. Residual FM Test Frequencies

F0 FREQUENCY
0.05 GHz (6647/6648)
1.8 GHz (6647/6648)
2.2 GHz (all)
7.8 GHz (all)
8.2 GHz (all)
12.2 GHz (all)
12.6 GHz (all)
18.6 GHz (6637/6647)
20.0 GHz (6638/6648)

4-8 EXTERNAL FM AND PHASE LOCK TESTS

To verify that the sweep generator exhibits the proper response to external frequency modulation and phase-lock signals, perform the steps below. If the response to FM and phase-lock signals is found to be out of tolerance, contact WILTRON Customer Service.

a. Connect test equipment as shown in Figure 4-12, and turn the equipment on.



Spectrum Analyzer Control Settings

FREQUENCY BAND: .01 - 1.8 GHz
RESOLUTION BW: 1 MHz
REF LEVEL: 9 dBm
INPUT ATTN: 20 dB
LOG SCALE: 10 dBm/Div.
FREQUENCY: 2.050 GHz
FREQ SPAN MODE: PER DIV
FREQUENCY SPAN/DIV: 2 MHz
SWEEP SOURCE: INT
SWEEP TRIGGER: FREE RUN
SWEEP TIME/DIV: AUTO

Figure 4-12. Test Equipment Setup for External FM and Phase Lock Test

b. On sweep generator,

   1. press RESET;
   2. press FM AND PHASELOCK;
   3. press CW F0 and set for 2.050 GHz.

c. On spectrum analyzer, adjust TUNING control to position trace near center screen, as shown in Figure 4-13.

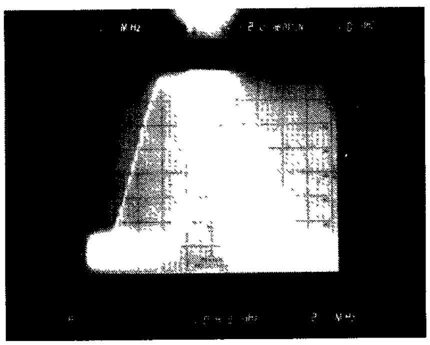


Figure 4-13. Frequency Modulation

d. Verify that FM deviation is ≈6 MHz.

e. On spectrum analyzer, select 8.5-18 GHz FREQUENCY BAND.

f. On sweeper, reset F0 frequency for 9 GHz.

g. Repeat steps c. and d.

h. Reset F0 frequency for 13 GHz.

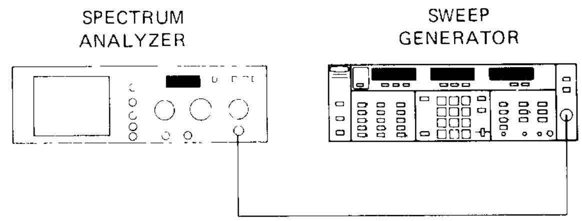
i. Repeat steps c. and d.

4-9 RF OUTPUT SIGNAL TESTS

To verify that the sweep generator's RF output signal meets the harmonic, spurious, purity, and frequency-pulling specifications, perform the steps in subparagraphs a thru d below. If any of the output-signal tests are found to be out of tolerance, contact WILTRON Customer Service.

a. <u>2nd Harmonic Attenuation Tests</u>

   1. Connect test equipment as shown in Figure 4-14, and turn the equipment on.



<u>Spectrum Analyzer Control Settings</u>

FREQUENCY BAND: .01 - 1.8 GHz for 6647/6648; 1.7 - 4.1 GHz for 6637/6638
RESOLUTION BW: 1 MHz
REF LEVEL: 10 dBm
INPUT ATTN: 30 dB
FREQUENCY SCAN/DIV: 20 MHz
FREQ SPAN MODE: PER DIV
LOG SCALE: 10 dB
SWEEP SOURCE: INT
SWEEP TRIGGER: FREE RUN
SWEEP TIME/DIV: AUTO

Figure 4-14. Test Equipment Setup for RF Output Signal Tests

   2. On sweep generator (sweeper),

      (a) press RESET;
      (b) press CW F0 and set to low-end frequency.

   3. On spectrum analyzer, adjust TUNING control to position the sweeper's fundamental frequency near the CENTER FREQUENCY graticule line; see Figure 4-15.

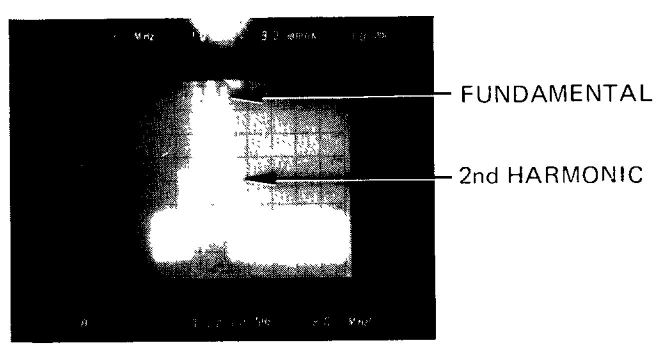


Figure 4-15. Fundamental and 2nd Harmonic Frequencies

4. While observing the spectrum analyzer's display,

   (a) move the sweeper's INCREASE-DECREASE lever toward INCREASE, so that the displayed signals move slowly upward in frequency, and

   (b) at the same time, adjust the spectrum analyzer's TUNING control clockwise to keep the 2nd harmonic on screen.

   NOTE

   Change the spectrum analyzer's FREQUENCY RANGE setting as necessary in order to observe the sweep generator's entire frequency range.

5. Verify that the 2nd harmonic is attenuated as shown below.

FREQUENCY	ATTENUATION
10 - 30 MHz (6647/6648)	-20 dBc
.03 - 2 GHz (6647/6648)	-30 dBc
2 - 18.6 GHz (all)	-40 dBc
18.6 - 20 GHz (6638/6648)	-40 dBc

b. Spurious Signal Test

1. On sweeper, move the INCREASE-DECREASE lever to maximum DECREASE, and return F0 to the low-end frequency.

2. On spectrum analyzer,

   (a) press FREQUENCY BAND .01-1.8 GHz (or 1.7-4.1 GHz), and

   (b) adjust TUNING for sweeper's low-end frequency.

3. While observing spectrum analyzer for non-harmonically-related (spurious) signals, move the sweeper's INCREASE-DECREASE lever toward INCREASE.

4. Verify that spurious signals, if present, are >-35 dBc for the .01-2 GHz band, and >-60 dBc for the remaining 2 to 18.6 (or 20) GHz frequency range.

   NOTE

   Spurious signals may be generally characterized as follows: they will (1) be weak in power, (2) "pop up" abruptly and track oppositely to the fundamental and harmonic signals, and (3) disappear abruptly. An example of a spurious response at 984 MHz is shown in Figure 4-16.

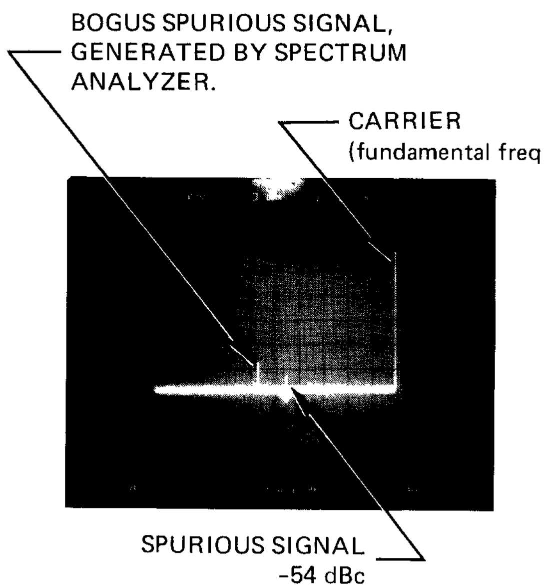


Figure 4-16. Example of a Spurious Signal

c. Signal Purity Test

1. On sweeper, press CW F1 and set for 2.050 GHz.

2. On spectrum analyzer,

   (a) press FREQUENCY BAND 1.7-4.1 GHz;

   (b) adjust FREQUENCY SPAN/DIV for 100 kHz;

(c) adjust RESOLUTION BW for 10 kHz;

(d) adjust TUNING to center the sweeper's fundamental frequency on the CENTER FREQUENCY graticule line, as shown in Figure 4-17.

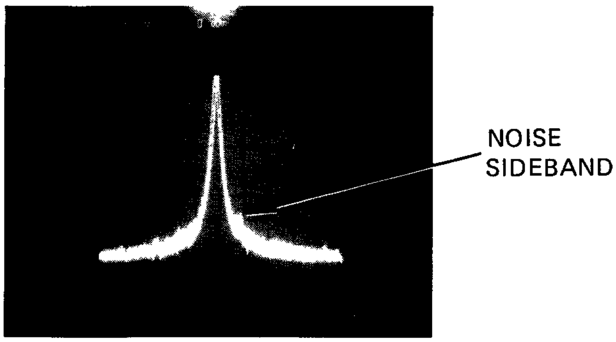


Figure 4-17. Noise Sidebands

3. Verify that the noise sidebands located 100 kHz away from the sweeper's fundamental frequency are >-60 dBc.

4. Repeat the Signal Purity Test for the following frequencies:

   (a) 8.05 GHz

   (b) 12.35 GHz

   (c) 12.45 GHz

   (d) 18.6 GHz (6637/6647)

   (e) 20.0 GHz (6638/6648)

d. Frequency Pulling Test

1. On sweeper,

   (a) press CW F0 and set for 2.050 GHz;

   (b) press LEVEL and set for 10 dBm.

2. On spectrum analyzer,

   (a) press FREQUENCY BAND 1.7-4.1 GHz;

   (b) adjust FREQUENCY SPAN/DIV to 100 kHz.

   (c) adjust RESOLUTION BW for 30 kHz;

   (d) adjust TUNING to center the sweeper's fundamental frequency on the CENTER FREQUENCY graticule line.

3. On sweeper, press LEVEL and set for 0 dBm.

4. On spectrum analyzer, displayed signal moves less than 500 kHz.

NOTE

The waveform photograph in Figure 4-18 shows a representative frequency shift. The photograph is a double exposure: the first exposure is the signal at 10 dBm and the second is the same signal at 0 dBm.

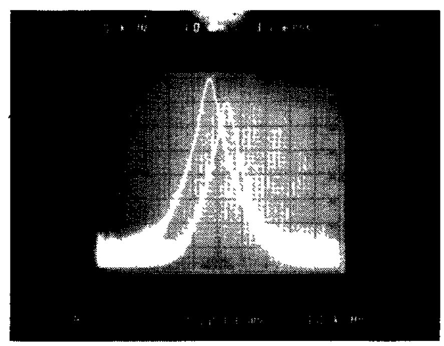


Figure 4-18. Example of Frequency Pulling

5. Repeat the Frequency Pulling test for the following frequencies:

   (a) 8.05 GHz

   (b) 12.35 GHz

   (c) 12.45 GHz

   (d) 18.6 GHz (6637/6647)

   (e) 20.0 GHz (6638/6648)

SECTION V

CALIBRATION AND ADJUSTMENTS

5-1 INTRODUCTION

This section contains adjustment and calibration instructions, and is organized as follows:

Para.	Adjustment or Calibration
5-4	Power Supply
5-5	A2 Ramp Generator
5-6	A5 Frequency Instruction
5-7	A3 Marker Generator
5-8	A6 Het/YIG Driver
5-9	A7 YIG Driver
5-10	A8 YIG Driver
5-11	Frequency Calibration
5-12	Tracking Filter
5-13	Sweep Rate Compensation
5-14	ALC Loop Calibration

5-2 RECOMMENDED TEST EQUIPMENT

The test equipment recommended for calibration of the sweep generator is listed in Table 4-1.

5-3 ADJUSTMENTS FOLLOWING PCB OR COMPONENT REPAIR OR REPLACEMENT

Table 5-1 lists the adjustments that should be performed following the repair or replacement of PCBs and components.

5-4 POWER SUPPLY ADJUSTMENTS

This paragraph provides instructions for adjusting the +5V and -38V supplies and the OUT OF REG, HIGH LINE, and LOW LINE motherboard LEDs. These adjustments should be performed when (1) power supply troubles are suspected and (2) after maintenance on any of the A13/A14 power supply circuits has been performed. The test equipment setup for the adjustments in subparagraphs d. and e. is shown in Figure 5-1.

a. <u>+5 Volt Adjustment</u>

1. Remove the top, bottom, and right-side covers. Refer to paragraph 7-3.1 for instructions.

CAUTION

If maintenance has been performed on the A13/A14 power supply, perform steps 2 thru 8; otherwise, proceed to step 9.

2. Remove the A1 (Option 3) and A2 thru A10 PCBs (Figure 5-2).

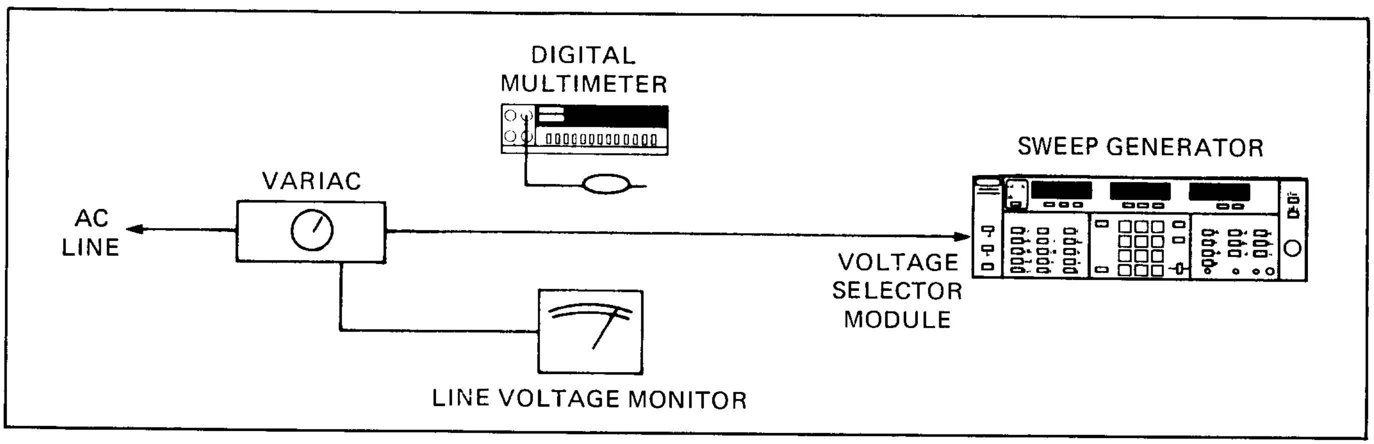


Figure 5-1. Test Equipment Setup for Low- and High-Line Adjustments

Table 5-1. Recommended Adjustments Following Repair Actions

IF A REPAIR OR REPLACEMENT ACTION WAS MADE TO:	PERFORM THE FOLLOWING ADJUSTMENTS IN PARAGRAPH(S):
A1 PCB	None
A2 PCB	5-5, 5-6, 5-8, & 5-11 thru 5-14.
A3 PCB	5-7
A4 PCB	5-14
A5 PCB	5-6 & 5-11 thru 5-14
A6 PCB	5-6, 5-8, & 5-11 thru 5-14
CAUTION After either performing maintenance on the A6-A8 PCBs or installing a replacement YIG, check the YIG bias before applying power to the YIG. Refer to paragraphs 5-8 thru 5-10.	
A7 PCB	5-6, 5-9, & 5-11 thru 5-14
A8 PCB	5-6 & 5-10 thru 5-14
A10 PCB	5-6 & 5-11 thru 5-14
A11 PCB	None
A12 PCB	None
A13/A14 PCBs	5-4 thru 5-14
Osc 1 YIG	Same as for the A6 PCB.
Osc 2 YIG	Same as for the A7 PCB.
Osc 3 YIG	Same as for the A8 PCB.
PIN Switch, Coupler or Model 720 Directional Detector	A4 Log Amplifier (This adjustment requires specialized test equipment, available only at factory authorized service centers.)

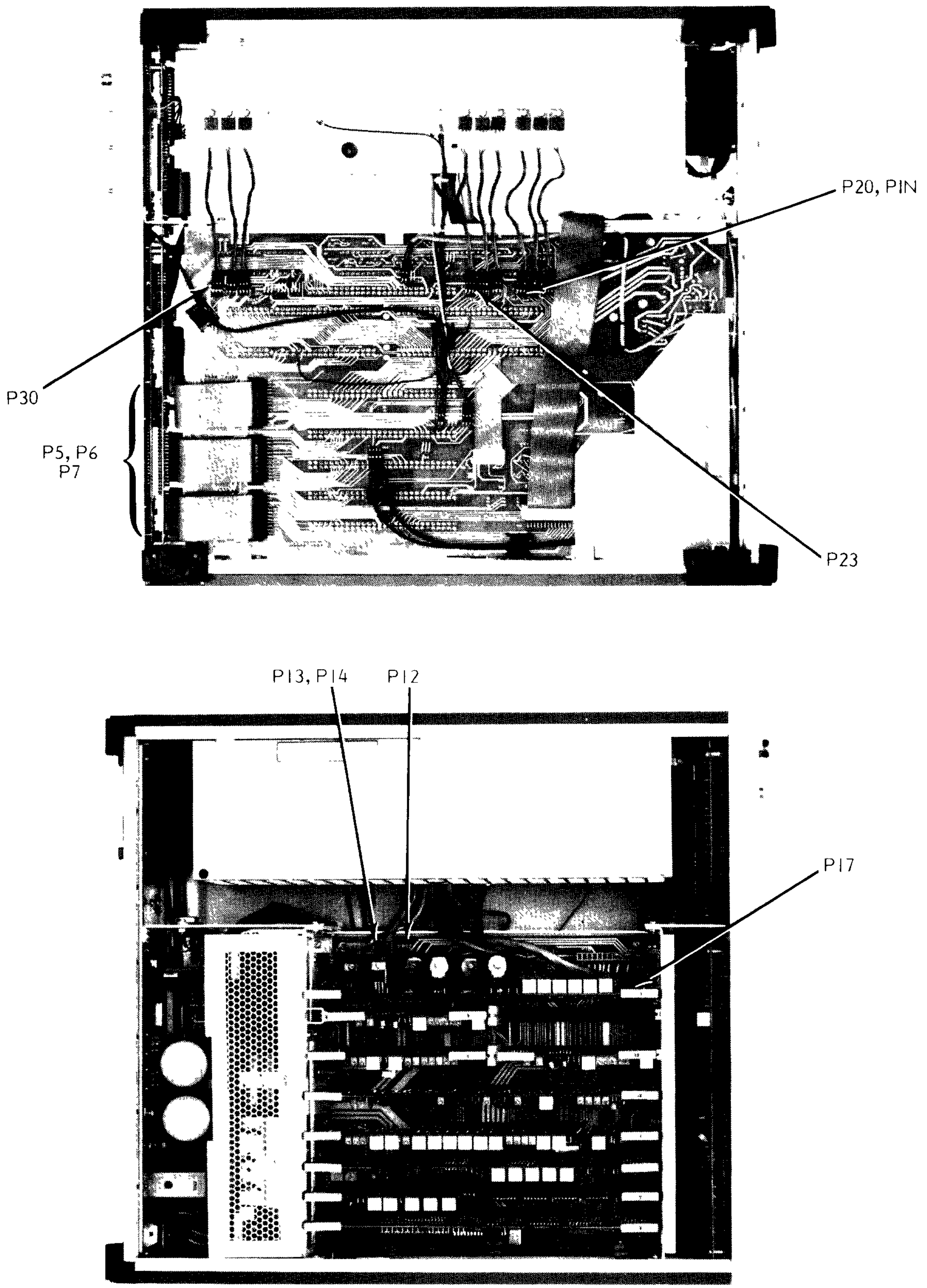


Figure 5-2. Connector Locations

3. Disconnect the following A14 connectors (Figure 5-2): P5, P6, P7, P12, P13, P14, P17, P20, P23, and P30.

4. Clip a 1/2W fixed resistor, 50 to 100Ω, between pins 13 and 26 on connector P3 (Figure 5-3), or between the +5V and GND test points.

5. Attach the digital multimeter (DMM) test leads to the resistor installed in step 4 above.

6. Press POWER to ON, and adjust A13R6 (Figure 5-4) for approximately 5 volts.

7. Press POWER to OFF, and disconnect the resistor from P3.

8. Reconnect the PCBs and connectors disconnected in steps 2 and 3.

9. Connect DMM test leads between pins 13 and 26 on P3, or between the +5V and GND test points.

10. Press POWER to ON and adjust A13R6 (Figure 5-4) for +5V ±1.0mV.

b. -38 Volt Adjustment

1. Disconnect the DMM from P3 and connect it between A14P20, pin 1 (Figure 5-2), and chassis ground.

2. Adjust A14R7 (Figure 5-4) for -38V ±100mV.

3. Remove the DMM from P20.

c. Out-of-Regulation Adjustment

1. Adjust A14R89 clockwise to its limit.

2. While observing the A14 OUT OF REG indicator, readjust A14R89 counterclockwise until the indicator goes out. Stop.

3. While counting the number of potentiometer turns, continue to adjust A14R89 counterclockwise until the indicator lights. Stop.

4. Readjust A14R89 clockwise halfway between the indicator's on and off states.

d. Low Line Voltage Adjustment

1. Press POWER to OFF.

2. Connect test equipment as shown in Figure 5-1.

3. Adjust the variac for 100 Vac, as observed on the line voltage monitor.

4. Adjust A14R79 to its clockwise limit; then readjust counterclockwise until the A14 LOW LINE indicator lights.

5. Readjust the variac for 115 Vac, and ensure the LOW LINE indicator is not lit.

e. High Line Voltage Adjustment

1. Adjust the variac for 130 Vac.

2. Adjust A14R80 to its clockwise limit, then readjust counterclockwise until the HIGH LINE indicator lights.

3. Readjust the variac for 115 Vac, and ensure the HIGH LINE indicator is not lit.

f. Voltage Regulation and Ripple Checks

The A13/A14 power supplies are well regulated and filtered. Also, the low- and high-line monitoring circuits are adjusted to flag their respective error codes well in advance of specified limits. Consequently, the power supply regulation and filtering (ripple) need not be checked on a periodic schedule. However, in the event that regulation or filtering problems are suspected, the specifications in Table 5-2 are provided.

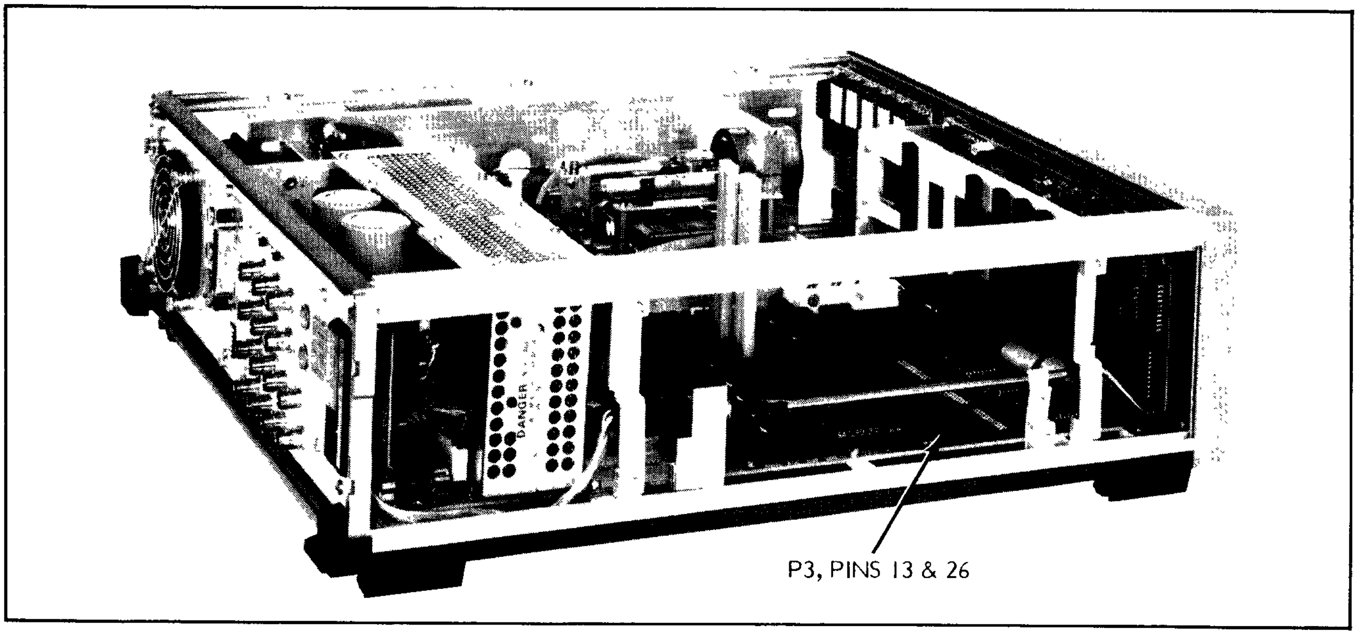


Figure 5-3. Connector P3, Pins 13 and 26

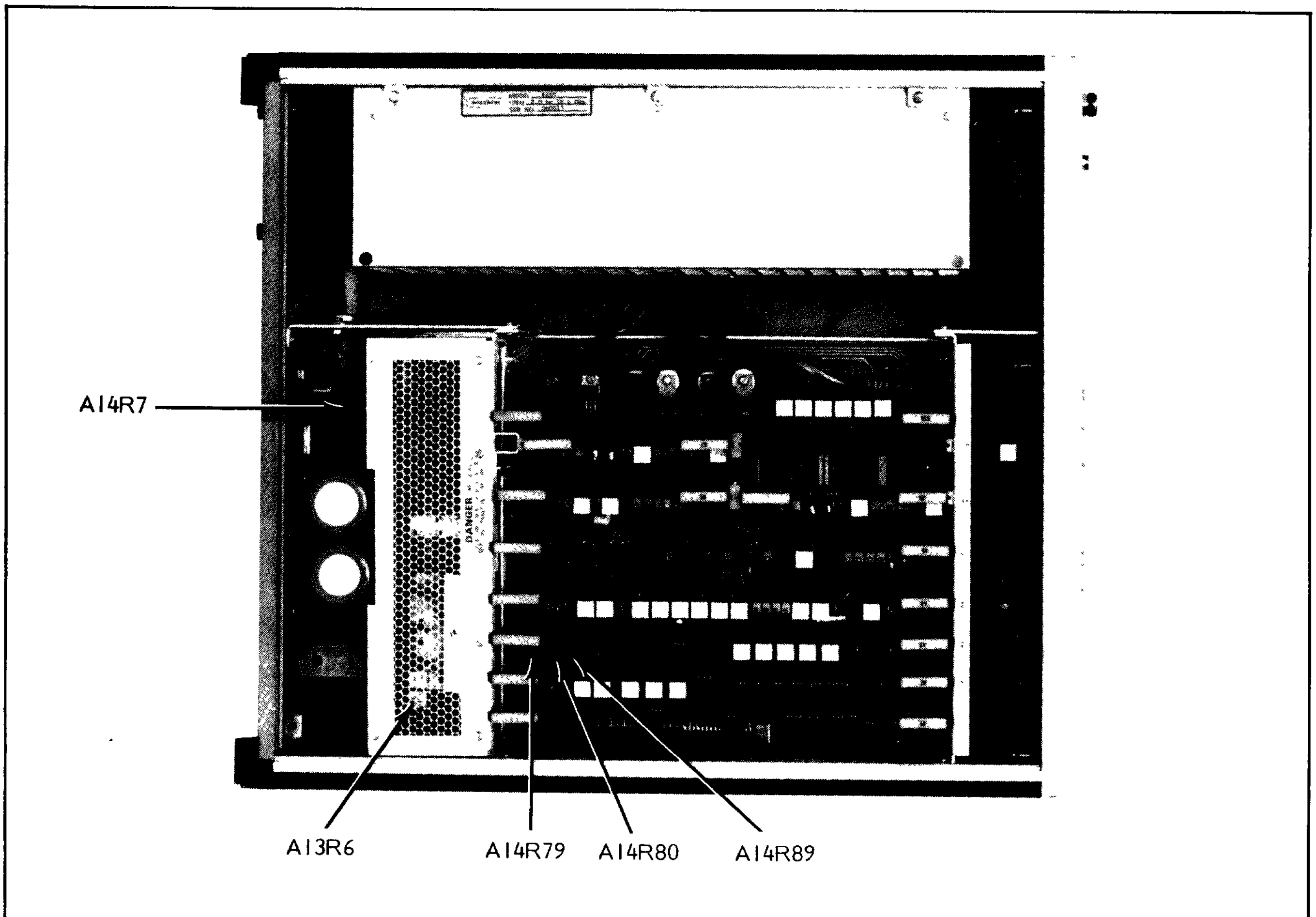


Figure 5-4. A13/A14 Power Supply Adjustments

Table 5-2. Power Supply Regulation and Ripple Specifications

VOLTAGE SUPPLY	MONITOR POINT	REGULATION TOLERANCE, 100% LOAD	REGULATION TOLERANCE, 10% LOAD	RIPPLE TOLERANCE, 100% LOAD (pk-pk)	RIPPLE TOLERANCE, 10% LOAD (pk-pk)
+5V	A14TP3 (P3-13)	±3mV	200mV	10mV	10mV
+15V LC	XA6-8	±300mV	±300mV	10mV	10mV
-15V LC	XA6-9	±300mV	±300mV	10mV	10mV
+15V HC	XA10-24	±300mV	±300mV	10mV	10mV
-15V HC	XA10-23	±300mV	±300mV	10mV	10mV
+12/-24V	XA6-1	±2V	±2V	50mV	50mV
+24V	A14P12-2	±300mV	±300mV	10mV	10mV
+28V	A14P13-4	±1V	±1V	50mV	50mV
-38V	A14P20-1	±300mV	±300mV	10mV	10mV

5-5 A2 RAMP GENERATOR ADJUSTMENTS

This paragraph provides instructions for adjusting the voltage and time of the A2 sweep ramp. These adjustments should be checked and, if necessary, adjusted (1) following maintenance on the A2 PCB and (2) when any of the frequency specifications are found to be out of tolerance. The voltage tolerance of the A2 sweep ramp is 1.0mV; consequently, an oscilloscope cannot be used to make this adjustment. To momentarily dwell the ramp at 0 and 10 volts – so that a digital voltmeter may be used – a special test fixture is required. A schematic of this test fixture is provided in Figure 5-6. The fixture's parts list is given in Table 5-3.

a. Reference Supply Verification

1. Connect test equipment as shown in Figure 5-5, and turn the equipment on.

2. Remove the top cover from the sweep generator (sweeper). Refer to paragraph 7-3.1 for instructions.

3. With digital multimeter (DMM) referenced to A2TP5, monitor A2U18:

   (a) pin 1 and verify the reference voltage is +12 ±1.0 volts;

   (b) pin 7 and verify the reference voltage is -12 ±1.0 volts.

b. Ramp Voltage Adjustment

1. Connect a test cable between the test fixture and the DMM, as shown in Figure 5-5.

2. On test fixture,

   (a) set S2 to A2 RAMP;

   (b) set S1 to 0V.

3. On sweeper,

   (a) press RESET;

   (b) press SWEEP TIME and set for 10 ms;

   (c) adjust A2R39 (Figure 5-7) for 0V ±1.0mV.

4. On test fixture, set S1 to 10V.

5. On sweeper, adjust A2R31 for 10V ±1.0mV.

6. On test fixture,

   (a) set S1 to 0V;

   (b) set S2 to HORIZ OUTPUT.

7. On sweeper, adjust A5R62 on the Frequency Instruction PCB for 0V (+0, -0.1mV).

8. On test fixture, set S1 to 10V.

9. Check that the DMM reads 10V ±50mV. If this voltage is out of tolerance, troubleshoot A5U21A, A5U21B, A5U23, and their associated resistors.

10. On sweeper,
    (a) press POWER to OFF;
    (b) disconnect the DIP clip from A2U25 and the cable from the HORIZ OUTPUT connector; remove the test fixture from the test setup.

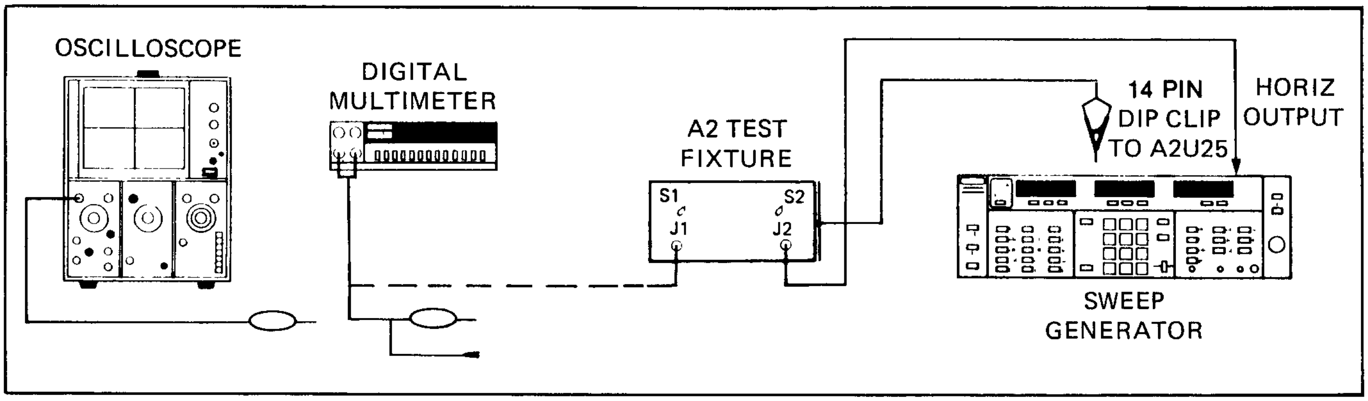
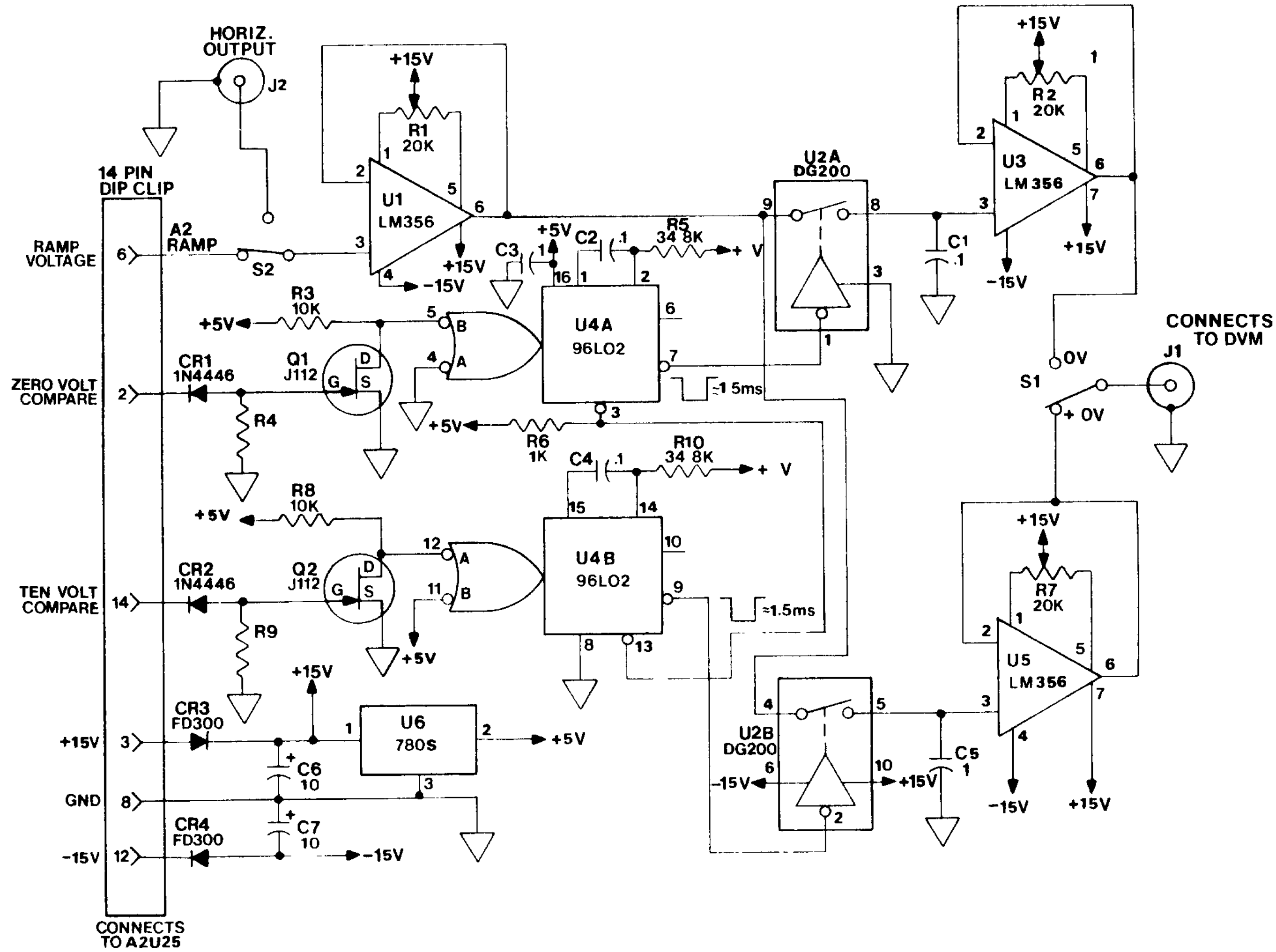


Figure 5-5. Test Equipment Setup for A2 Ramp Generator Adjustments

Table 5-3. A2 Test Fixture, Parts List

REF DES.	DESCRIPTION	WILTRON PART NO.
	CAPACITORS	
C1	0.1μF, Mylar	210-30
C2	0.1μF, Monolithic	230-37
C3	0.1μF, Monolithic	230-37
C4	0.1μF, Monolithic	230-37
C5	0.1μF, Mylar	210-30
C6	10μF, 25V, Tantalum	250-42
C7	10μF, 25V Tantalum	250-42
	DIODES	
CR1	Silicon	10-1N4446
CR2	Silicon	10-1N4446
CR3	FD300	10-FD300
CR4	FD300	10-FD300
	TRANSISTORS	
Q1	J112, JFET	20-17
Q2	J112, JFET	20-17
	RESISTORS	
R1	10-Turn Pot., 20k	157-20k
R2	10-Turn Pot., 20k	157-20k
R3	MF, 1/4W, 1%, 10k	110-10k-1
R4	MF, 1/4W, 1%, 100k	110-100k-1
R5	MF, 1/4W, 1%, 34.8k	110-34.8k-1
R6	MF, 1/4W, 1%, 1k	110-1k-1
R7	10-Turn Pot., 20k	157-20k
R8	MF, 1/4W, 1%, 10k	110-10k-1
R9	MF, 1/4W, 1%, 100k	110-100k-1
R10	MF, 1/4W, 1%, 34.8k	110-34.8k-1
	SWITCHES	
S1	SPDT, Toggle	420-5
S2	SPDT, Toggle	420-5
	INTEGRATED CIRCUITS	
U1	LM356, Op. Amp.	50-9
U2	DG200BA, Dual Analog Switch	50-DG200BA
U3	LM356, Op. Amp.	50-9
U4	96L02, Dual One-Shot	54-96L02
U5	LM356, Op. Amp.	50-9
U6	MC7805, +5V Reg.	54-MC7805CP
	MISCELLANEOUS	
J1, J2	Connector, BNC Female	510-5
—	14-Pin DIP Clip (Newark Electronics Stock No.: 65F127)	None



Calibrate (null) the A2 Test Fixture so that zero volts into U1, U3, and U5 produces zero volts out, as follows:

1. Connect test fixture DIP clip to A2U25.
2. On sweep generator, press POWER to ON.
3. On test fixture:
   a. Set S2 to HORIZ OUTPUT.
   b. Connect a grounding lead between pin 3 on U5 and pin 8 on the DIP clip.
   c. With DMM, monitor U5 pin 6, and adjust R7 for 0V ±50μV.
   d. In a similar manner, adjust R1 for 0V ±50μV from U1, and adjust R2 for 0V ±50μV from U3.

Figure 5-6. A2 Test Fixture, Schematic and Calibration Procedure

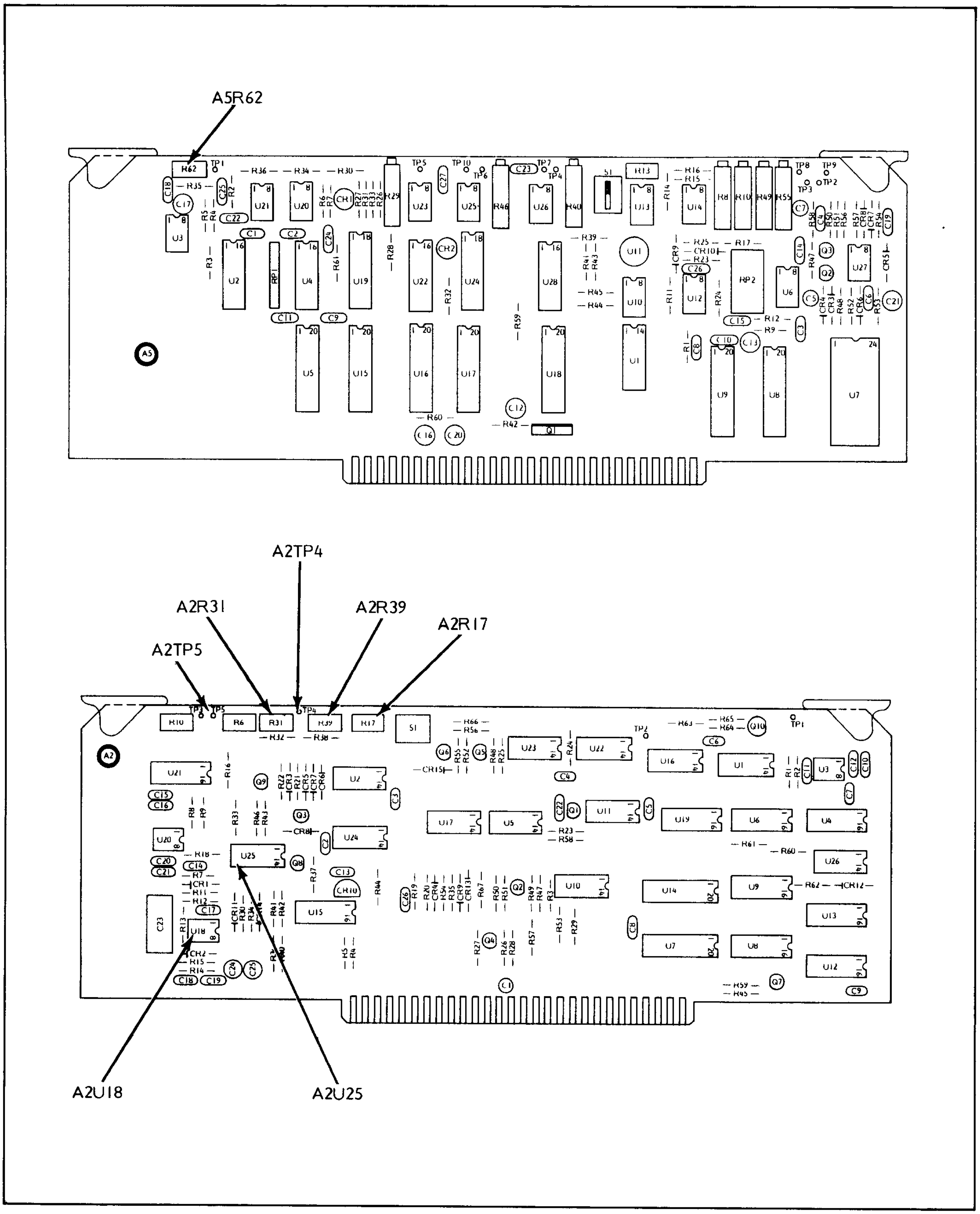


Figure 5-7. A2 Ramp Generator Adjustments

c. Sweep Time Adjustment

1. Connect the oscilloscope as follows:
   (a) probe to A2TP4,
   (b) ground to A2TP5.

2. Set oscilloscope controls as follows:
   (a) vertical to 2V per division,
   (b) horizontal to 200 ms per division.

3. On sweeper,
   (a) press POWER to ON;
   (b) press ΔF F0;
   (c) press SWEEP TIME and set for 0.999 seconds;
   (d) adjust A2R10 for a forward sweep duration (Figure 5-8) of 1.0 ±0.1 seconds.

4. Set oscilloscope horizontal for 2 ms per division.

5. On sweeper,
   (a) set SWEEP TIME for 10 ms;
   (b) adjust A2R6 for a forward sweep duration of 10 ±1 ms.

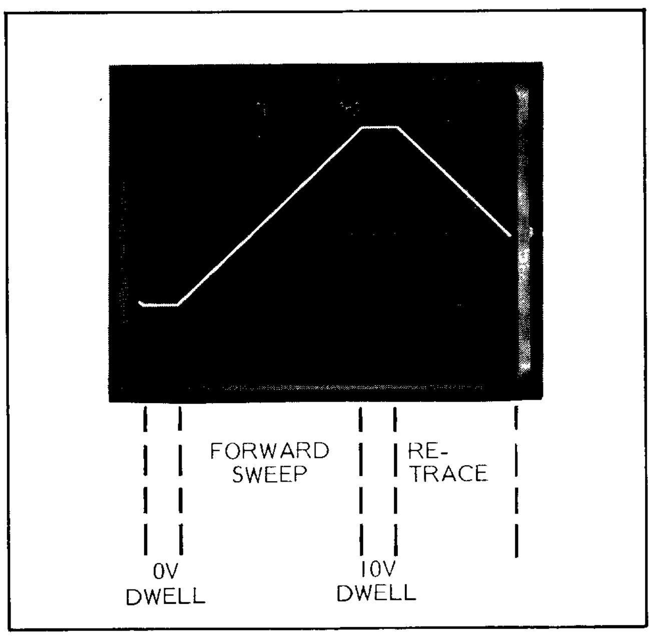


Figure 5-8. A2 Sweep Ramp

6. Set oscilloscope horizontal for 200 ms per division.

7. On sweeper,
   (a) set SWEEP TIME for 1 second;
   (b) adjust A2R17 for a forward sweep duration of 1.0 ±0.1 seconds.

8. With oscilloscope, verify retrace and dwell times at 10 ms and 1 second. Retrace and dwell time specifications are shown in Table 5-4. If the retrace time is out of tolerance, (1) check that +15V is present at A2R8 (Figure 7-29, Sheet 2) and (2) if +15V is present, troubleshoot A2U21D and associated resistors. If the dwell time is out of tolerance, troubleshoot the dwell timing circuit (paragraph 7-9.1b).

Table 5-4. Retrace and Dwell Time Specifications

SWEEP TIME	RETRACE TIME	DWELL TIME
10 ms to 0.999 s	10 ±1 ms	2 ±0.2 ms
1 s to 99 s	1 ±0.1 s	30 ±3 ms

5-6 A5 FREQUENCY INSTRUCTION ADJUSTMENTS

This paragraph provides instructions for adjusting the A5 sweep width (ΔF) ramp, the A5 F Center DAC voltages, and the A6-A8 bandswitch reference voltages. These adjustments should be checked and, if necessary, adjusted (1) following maintenance on the A5 PCB, (2) following maintenance on any of the A6-A8 PCBs, and (3) when any of the frequency specifications are found to be out of tolerance.

a. Bandswitch Reference Voltage Adjustment

1. Set up the test equipment as shown in Figure 5-9 and turn the equipment on.

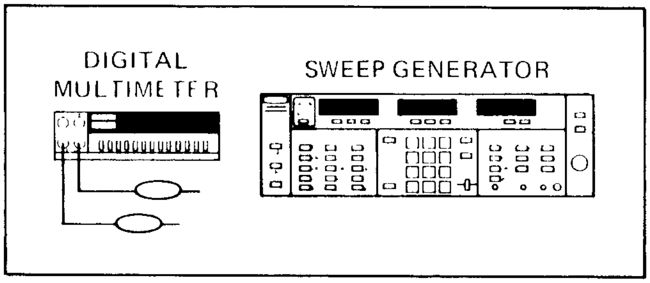


Figure 5-9. Setup for A5 Frequency Instruction Adjustments

2. Remove the top cover from the sweep generator (sweeper). Refer to paragraph 7-3.1 for instructions.

3. Connect the common lead on the digital multimeter (DMM) to A5TP3 (Figure 5-10) and the test lead to A5TP9.

4. Adjust A5R55 for +10V ±1.0mV.

5. Move the DMM test lead to A5TP8 and adjust A5R49 for -10 ±1.0mV.

b. <u>Sweep Width (ΔF) Signal Path Adjustments</u>

1. Press RESET.

2. Press MANUAL SWEEP.

3. Move the DMM test lead to A5TP5.

4. While observing the DMM, rotate the MANUAL SWEEP control from its counterclockwise to its clockwise limits and adjust A5R29 for equal positive and negative voltage excursions. Voltage excursions should range between ≈-5V and ≈+5V.

5. Move the DMM test lead to A5TP6.

6. Repeat step 4 for A5R46.

7. Move the DMM test lead to A5TP7.

8. Press ΔF F0, and set ΔF for 0 MHz.

9. Adjust A5R40 for 0V ±1.0mV.

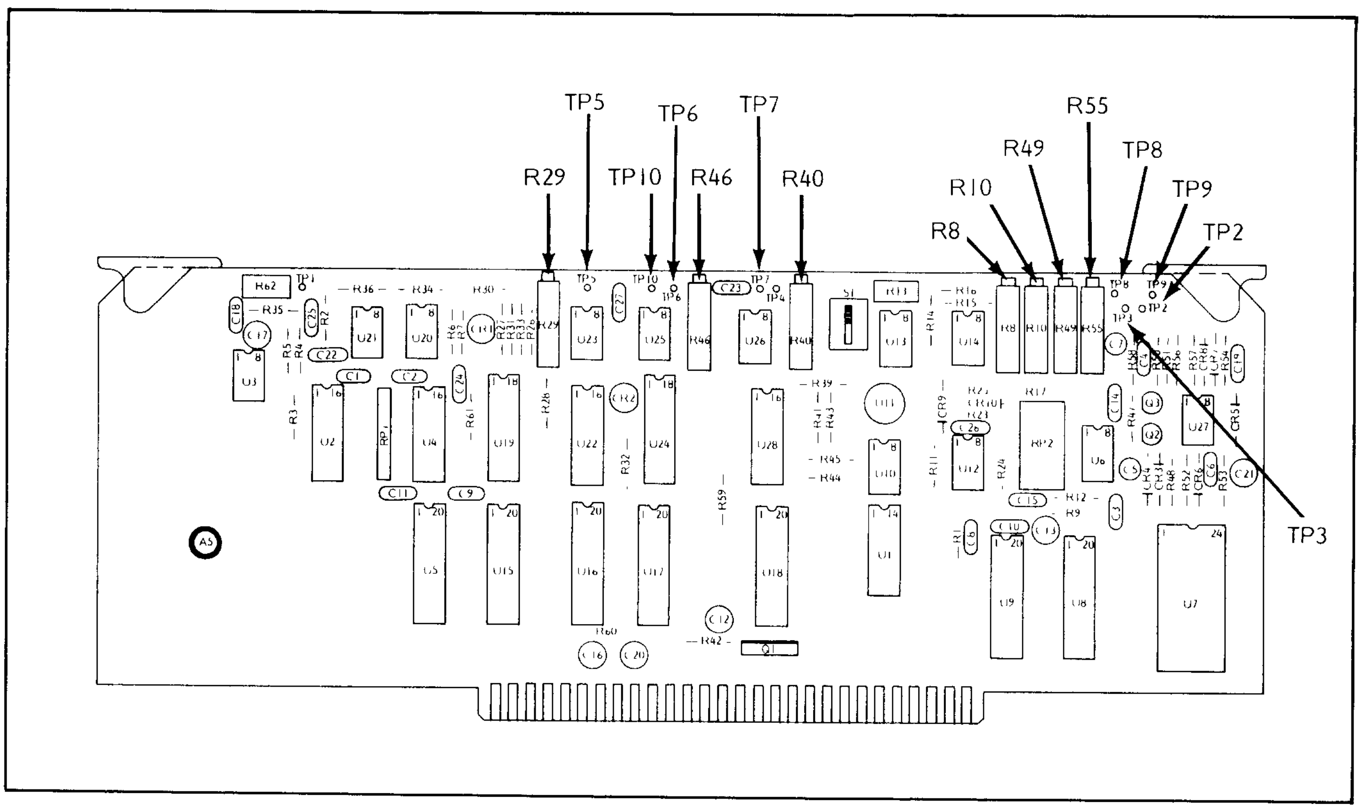


Figure 5-10. A5 Frequency Instruction Adjustments

c. F Center Adjustments

1. Press TRIGGER AUTO.

2. Press CW F1 and set for low-end frequency.

3. Move the DMM test lead to A5TP2.

4. Adjust A5R10 for the low-end frequency voltage, as shown below:

Model	Voltage	Tolerance
6637	1.0752V	0.1mV
6638	1.0000V	0.1mV
6647	5.3mV	0.1mV
6648	5.0mV	0.1mV

5. Press CW F2 and set for high-end frequency.

6. Adjust A5R8 for 10V ±0.1mV.

7. Using CW F1 and CW F2, repeat (if necessary) the low- and high-end frequency adjustments until the voltages specified above are achieved.

5-7 A3 MARKER GENERATOR ADJUSTMENTS

This paragraph provides instructions for adjusting both the F0, M1, and M2 marker frequencies and the MODIFY SIGNAL output voltage from the front panel INCREASE-DECREASE lever. These adjustments should be checked and, if necessary, adjusted following maintenance on the A3 PCB.

Two methods for adjusting the marker frequencies are provided: (1) using the Model 560 Scalar Network Analyzer and (2) using an oscilloscope. The method using the 560 (subparagraph c) is preferred. If a 560 is not available, an alternate procedure using an oscilloscope is described in subparagraph b.

The reference voltage check, in subparagraph a below, should be performed before adjusting the marker frequencies.

a. A3 Reference Voltage Check

1. Remove the top cover from the sweep generator (sweeper). Refer to paragraph 7-3.1 for instructions.

2. Press POWER to ON.

3. With a digital multimeter (DMM) referenced to A3TP1 (Figure 5-12),

   (a) monitor A3U3 pin 1, and verify the voltage is -10 ±0.25V;

   (b) monitor A3U3 pin 7, and verify the voltage is -10 ±0.25V.

4. If either voltage is out of tolerance, troubleshoot A3U3 and its associated components before continuing with this procedure.

b. Marker Frequency Calibration Using an Oscilloscope

1. Set up the test equipment as shown in Figure 5-11, and turn the equipment on.

2. On test fixture, set S1 to 0V.

3. On sweeper,

   (a) press RESET;

   (b) adjust A5R62 (Figure 5-12) for 0V ±1.0mV.

4. On test fixture, set S1 to 10V.

5. Check that the DMM reads 10V ±50mV. If this voltage is out of tolerance, perform the A2 Ramp Generator Adjustments in paragraph 5-5.

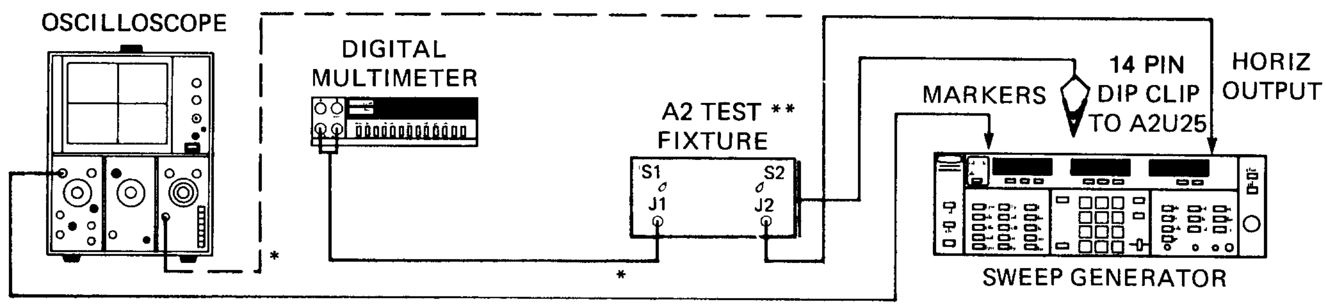
6. On sweeper,

   (a) press POWER to OFF;

   (b) disconnect the DIP clip from A2U25;

   (c) press POWER to ON.

7. Disconnect the cable from J2 on the test fixture, and connect it to the External Horizontal Input jack on the oscilloscope.



* Connect as directed by procedure.
** Refer to paragraph 5-5.

Figure 5-11. Test Equipment Setup for A3 Marker Generator Adjustments

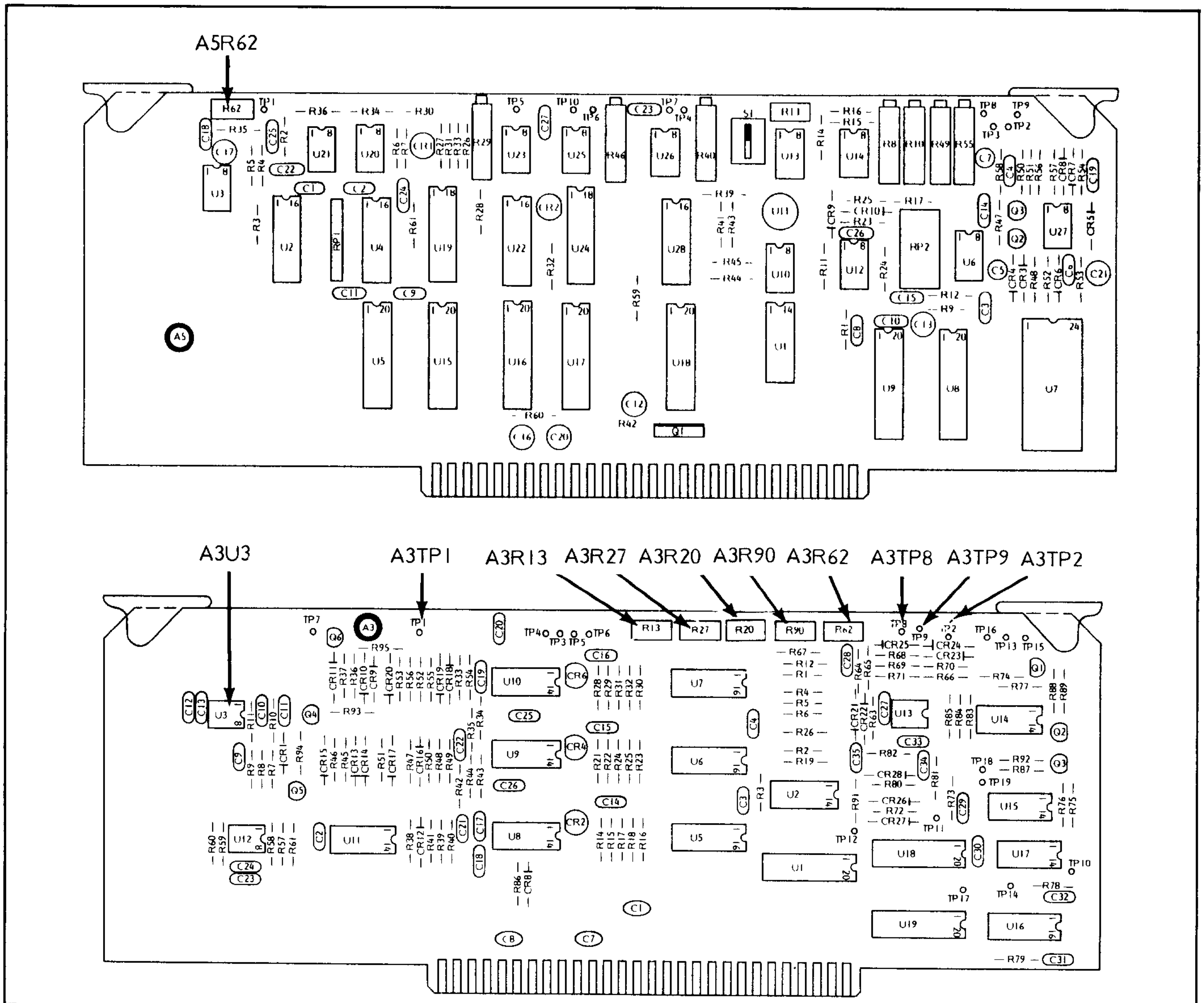


Figure 5-12. A3 Marker Generator Adjustments

8. On sweeper,

   (a) press MARKERS VIDEO;

   (b) rotate MARKERS AMPLITUDE fully clockwise;

   (c) press F0 and set for high-end frequency;

   (d) adjust A3R13 (Figure 5-12) until the F0 marker is just visible on the right edge of the oscilloscope display, as shown in Figure 5-13;

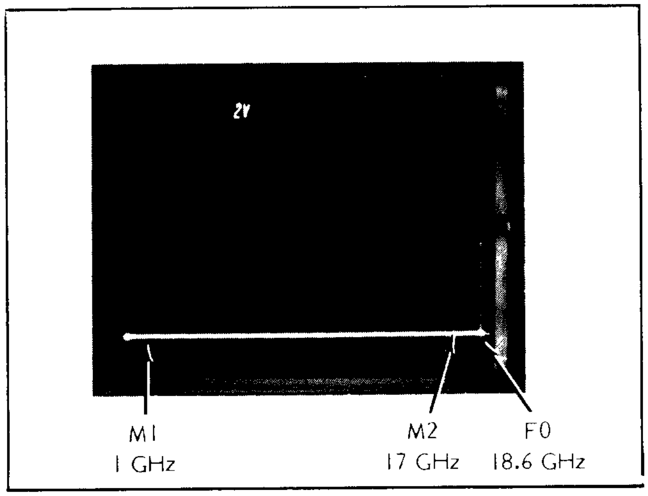


Figure 5-13. F0, M1, and M2 Markers

   (e) set F0 for 10 GHz;

   (f) press M1 and set for high-end frequency;

   (g) using A3R20, repeat step (d) above for the M1 marker;

   (h) set M1 for 12 GHz;

   (i) press M2 and set for high-end frequency;

   (j) using A3R27, repeat step (d) above for the M2 marker.

c. Marker Frequency Calibration Using the Model 560 Scalar Network Analyzer

1. Set up the test equipment as shown in Figure 5-15, and turn the equipment on.

2. On sweeper,

   (a) press RESET;

   (b) press MARKERS VIDEO;

   (c) rotate MARKERS AMPLITUDE fully clockwise.

3. On 560,

   (a) adjust Channel A OFFSET to position the trace in the center of the display;

   (b) adjust MARKERS THRESHOLD, if necessary, to obtain markers.

4. On sweeper,

   (a) press F0 and set for high-end frequency;

   (b) adjust A3R13 (Figure 5-12) until the F0 marker is just visible on the right edge of the 560 display, as shown in Figure 5-14.

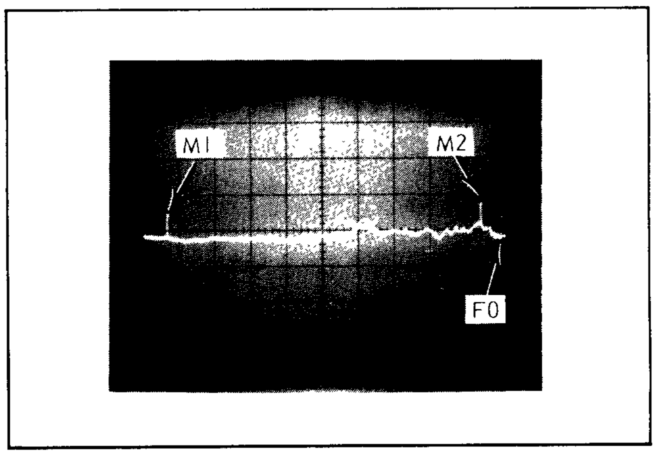


Figure 5-14. Model 6637 Markers, as shown on 560 Display

   (c) set F0 for low-end frequency;

   (d) adjust A5R62, if necessary, to position the F0 marker at the left edge of the display;

   (e) set F0 for 10 GHz;

   (f) press M1 and set for high-end frequency;

   (g) using A3R20, repeat step (b) above for the M1 marker;

   (h) set M1 for 12 GHz;

   (i) press M2 and set for high-end frequency;

(j) using A3R27, repeat step (b) above for the M2 marker.

d. INCREASE-DECREASE Lever Voltage Adjustment

1. Connect the common lead on the DMM to A3TP2, and the test lead to A3TP8.

2. Move the INCREASE-DECREASE lever to full INCREASE; release the lever and allow it to spring back to the center. Note the voltage value.

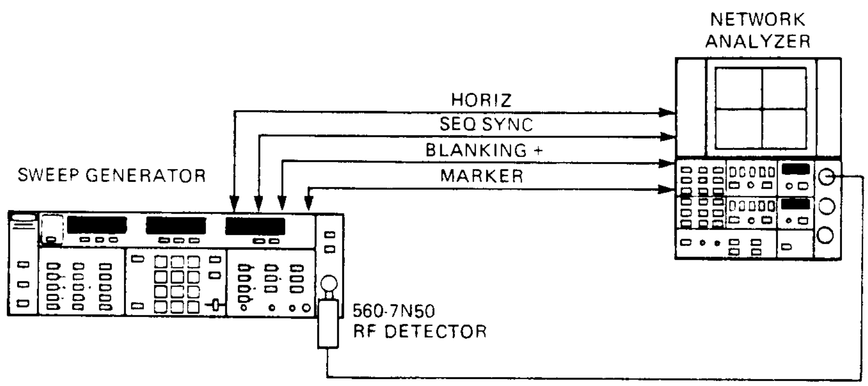
3. Move the INCREASE-DECREASE lever to full DECREASE; release the lever and allow it to spring back to the center. Note the voltage value.

4. Repeat steps 3 and 4, and adjust A12R46 (Figure 5-16) until the noted voltages are equal, ±200mV. Voltage value should be between 0 and ±0.5V.

5. Transfer the DMM test lead to A3TP9.

6. Move the INCREASE-DECREASE lever to its full INCREASE position, and adjust A3R62 (Figure 5-12) for +4.8V ±20mV.

7. Move the INCREASE-DECREASE lever to its full DECREASE position, and adjust A3R90 for +4.8V ±20mV.



Initial Control Settings

Sweep Generator

MARKER AMPLITUDE: Fully CW
HORIZ OUTPUT DURING CW (rear panel): ON
SLOPE: OFF

Scalar Network Analyzer

CHANNEL A ON: On
INPUT: A
MEMORY: Off
dB PER DIVISION: 5
REFERENCE dB/dBm: dBm
SET (screwdriver pot): Midrange
OFFSET: +10
CHANNEL B: Not used
MARKER THRESHOLD: Midrange
REAL TIME: On
SMOOTHING: Off
POWER: On

Figure 5-15. Test Setup for Marker Frequency Adjustment Using the Model 560 Scalar Network Analyzer

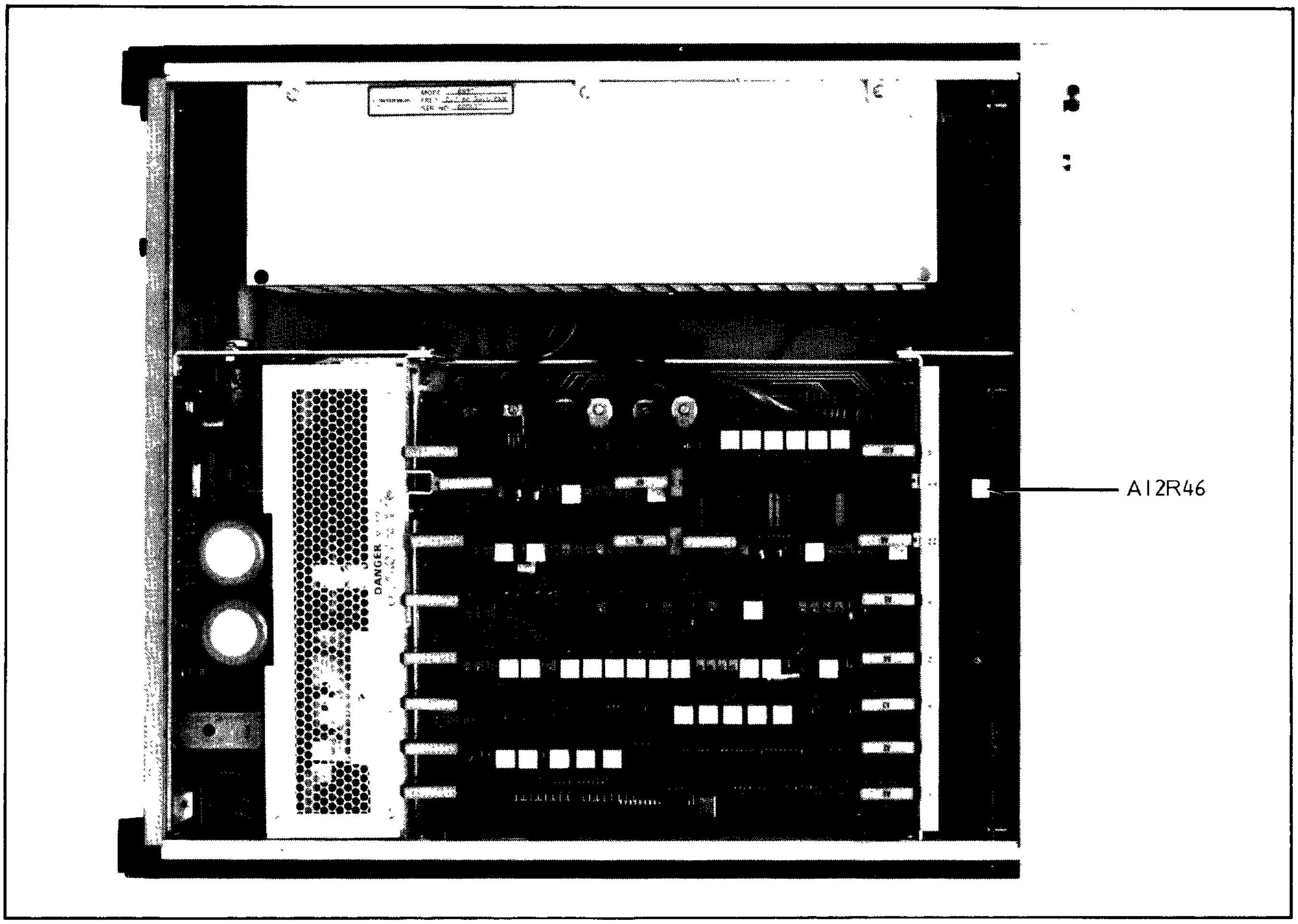


Figure 5-16. A12R46 Adjustment Location

5-8 A6 HET/YIG DRIVER ADJUSTMENTS

This paragraph provides instructions for adjusting the A6 PCB's Start of Next Band (SNB) and Start of Next ROM (SNR) adjustments, and for checking the Osc 1 YIG bias voltage. These adjustments should be performed following maintenance on the A6 PCB, and whenever a replacement YIG is installed.

CAUTION

After either performing maintenance on the A6 PCB or installing a replacement YIG, check the YIG bias before applying power to the YIG, as follows:

- remove the connector from A14P14 (Figure 5-2);
- connect a grounding lead between P14 pin 2 and the chassis;
- perform the instructions in subparagraph b below;
- reinstall the connector on P14;
- perform the adjustments outlined in Table 5-1.

a. Start of Next Band (SNB) Adjustments

1. Set up the test equipment as shown in Figure 5-17, and turn the equipment on.

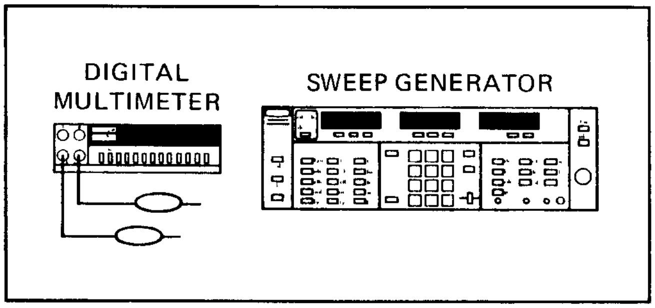


Figure 5-17. Test Equipment Setup for Het/YIG Driver Adjustments

2. Remove the top cover from the sweep generator (sweeper). Refer to paragraph 7-3.1 for instructions.

3. Press RESET.

4. Press CW F1.

NOTE

Steps 5 thru 8 are for Models 6647 and 6648 only; proceed to step 9 for Models 6637 and 6638.

5. Press F1 and set for 2 GHz.

6. Connect the common lead on the digital multimeter (DMM) to A6TP1 (Figure 5-18) and the test lead to A6TP5.

7. Adjust A6R65 clockwise until the DMM reads ≈0V (TTL low).

8. Readjust R65 counterclockwise until the SNB line just switches HIGH and the DMM reads ≈+5V (TTL high).

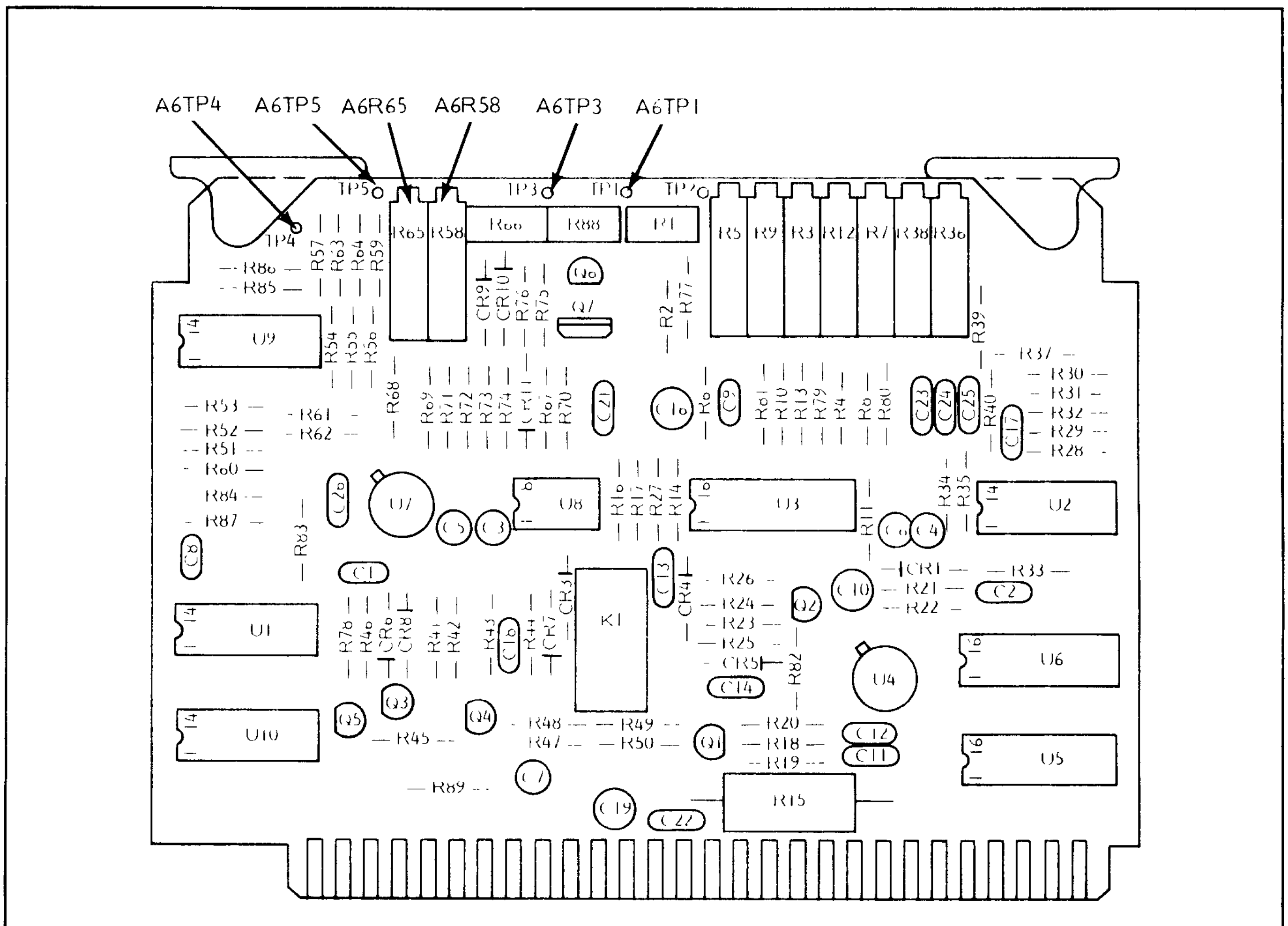


Figure 5-18. A6 Het/YIG Driver Adjustments

9. Set F1 for 8 GHz.

10. Move the DMM test lead to A6TP4.

11. Adjust A6R58 clockwise until the DMM reads ≈0V (TTL low).

12. Readjust R58 counterclockwise until the SNB line just switches HIGH and the DMM reads ≈+5V (TTL high).

b. YIG Bias Voltage Check

1. Move the DMM test lead to A6TP3.

2. Verify the DMM reads -5 ±0.2V.

3. Press RF ON to OFF, and verify the DMM reads 0 ±0.5V.

5-9 A7 YIG DRIVER ADJUSTMENTS

This paragraph provides instructions for performing the Start of Next Band (SNB) and Start of Next ROM (SNR) adjustments on A7, the Volts Per Frequency (VPF) adjustment on A5, and the Osc 2 YIG bias adjustments for the 660-D-8008 (-Bias) assembly. It also provides instructions for checking the YIG bias on the 660-D-8009 (+Bias) assembly. These adjustments should be performed following maintenance on the A7 PCB, and whenever a replacement YIG has been installed.

CAUTION

After either performing maintenance on the A7 PCB or installing a replacement YIG, check the YIG bias before applying power to the YIG, as follows:

- 660-D-8009 assembly: remove the connector from A14P13 (Figure 5-2).
- 660-D-8009 assembly: connect a grounding lead between P13 pin 2 and the chassis.
- 660-D-8008 assembly: adjust A7R47 fully clockwise and A7R42 fully counterclockwise.
- Perform the instructions in subparagraphs b. and c. or d. below.
- Reinstall the connector on P13.
- Perform the adjustments outlined in Table 5-1.

a. Start of Next Band (SNB) Adjustments

1. Set up the test equipment as shown in Figure 5-19, and turn the equipment on.

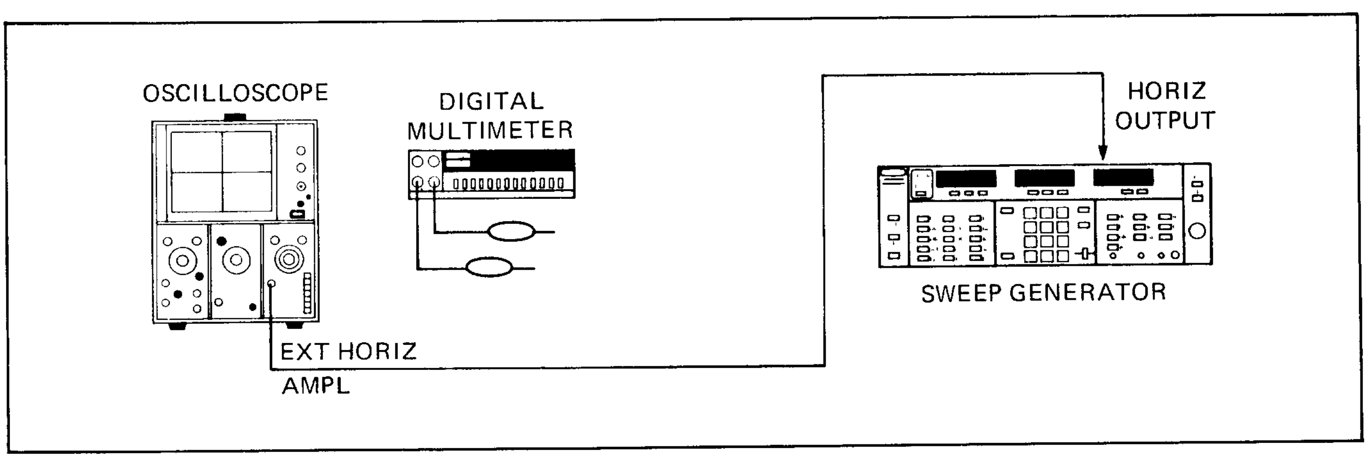


Figure 5-19. Test Equipment Setup for the A7 YIG Driver Adjustments

2. Remove the top cover from the sweep generator (sweeper). Refer to paragraph 7-3.1 for instructions.

3. Press RESET.

4. Press CW F1 and set for 12.4 GHz.

5. Connect the common lead on the digital multimeter (DMM) to A7TP1 (Figure 5-21) and the test lead to A7TP4.

6. Adjust A7R68 clockwise until the DMM reads ≈0V (TTL low).

7. Readjust R68 counterclockwise until the SNB line just switches HIGH and the DMM reads ≈+5V (TTL high).

b. Osc 2 Volts-Per-Frequency (VPF) Adjustment

1. Press FREQUENCY RANGE ΔF F0.

2. Press F0 and set for 12.4 GHz.

3. Adjust the oscilloscope vertical controls to obtain a horizontal trace, as shown in Figure 5-20.

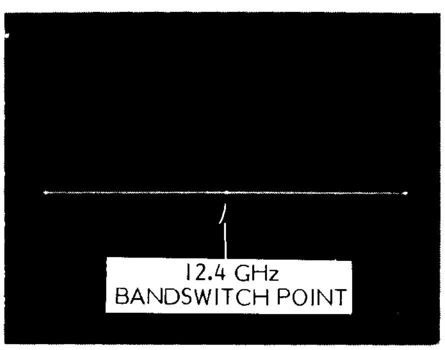


Figure 5-20. Bandswitch Dwell Signal

4. Adjust A5R13 on the Frequency Instruction PCB to center the 12.4 GHz bandswitch point on the oscilloscope display (Figure 5-20).

NOTE

Before proceeding to step c., remove the A7 PCB and determine whether it is a 660-D-8008 or a 660-D-8009 assembly. If it is an -8008, perform step c. If it is an -8009, perform step d.

c. Osc 2 YIG Bias Adjustment, 660-D-8008 Assembly

1. Move the DMM test lead to A7TP3.

2. Press FREQUENCY RANGE F1-F2.

3. Press F1 and set for 8 GHz.

4. Press F2 and set for 12.4 GHz.

5. Press MANUAL SWEEP and rotate the associated control fully counterclockwise.

6. Adjust A7R47 for the bias voltage specified for 8 GHz. This voltage value can be found either on the YIG's label or in the data sheet that accompanies the YIG.

7. Rotate the MANUAL SWEEP control fully clockwise.

8. Adjust A7R42 for the bias voltage specified for 12.4 GHz.

d. Osc 2 YIG Bias Check, 660-D-8009 Assembly

1. Move the DMM test lead to A7TP3.

2. Press FULL.

3. Verify the DMM reads +15 ±0.5 volts.

4. Press RF ON to OFF.

5. Verify the DMM reads 0 ±0.5 volts.

5-10 A8 YIG DRIVER ADJUSTMENTS

This paragraph provides instructions for adjusting or checking the Osc 3 YIG bias. On

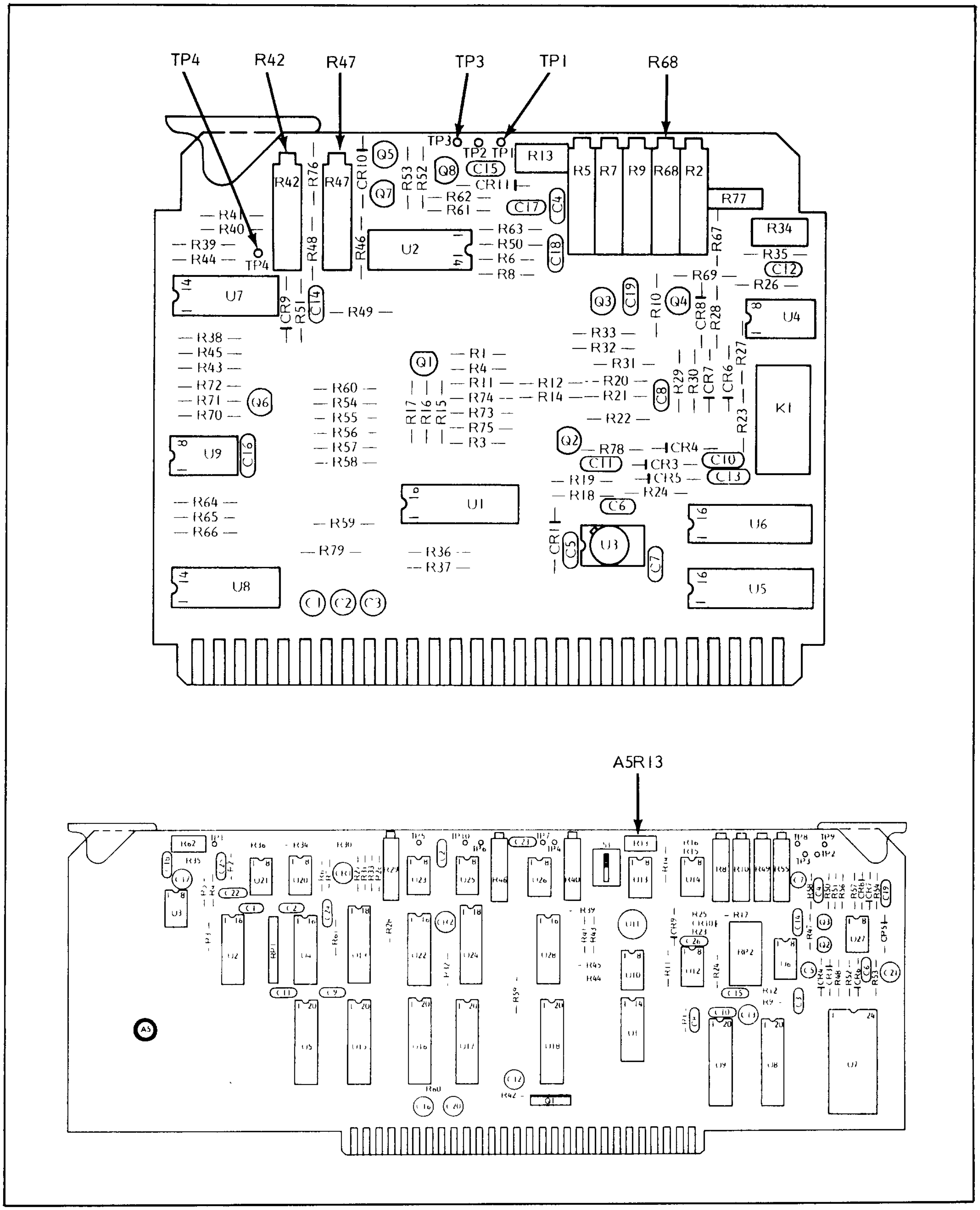


Figure 5-21. A7-A8 YIG Driver Adjustments

the 660-D-8008 (-Bias) assembly, the YIG bias is adjustable; on the 660-D-8009 (+Bias) assembly, the YIG bias is fixed. These adjustments or checks should be performed following maintenance on the A8 PCB, and whenever a replacement YIG has been installed.

CAUTION

After either performing maintenance on the A8 PCB or installing a replacement YIG, check the YIG bias before applying power to the YIG, as follows:

- 660-D-8009 assembly: remove the connector from A14P17 (Figure 5-2).
- 660-D-8009 assembly: connect a grounding lead between P17 pin 2 and the chassis.
- 660-D-8008 assembly: adjust A8R47 fully clockwise and A8R42 fully counterclockwise.
- Perform the instructions in subparagraph a. or b. below.
- Reinstall the connector on P17.
- Perform the adjustments outlined in Table 5-1.

NOTE

Before proceeding to step a., remove the A8 PCB and determine whether it is a 660-D-8008 or -8009 assembly. If it is an -8008, perform step a. If it is an -8009, perform step b.

a. Osc 3 YIG Bias Adjustment, 660-D-8008 Assembly

1. Set up test equipment as shown in Figure 5-22, and turn the equipment on.

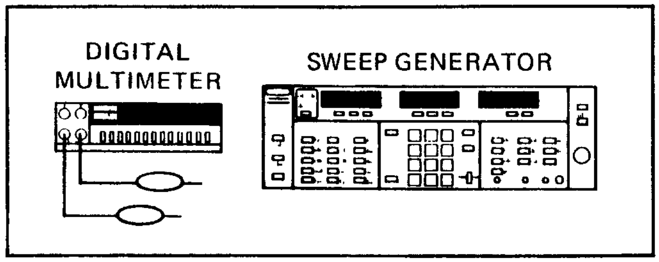


Figure 5-22. Test Equipment Setup for A8 YIG Driver Adjustments

2. Remove the top cover from the sweep generator. Refer to paragraph 7-3.1 for instructions.

3. Connect the common lead on the digital multimeter (DMM) to A8TP1 (Figure 5-21) and the test lead to A8TP3.

4. Press RESET.

5. Press FREQUENCY RANGE F1-F2.

6. Press F1 and set for 12.4 GHz.

7. Press F2 and set for 18.6 (or 20) GHz.

8. Press MANUAL SWEEP and rotate the associated control fully counterclockwise.

9. Adjust A8R47 for the bias voltage specified for 12.4 GHz. This voltage value can be found either on the YIG's label or in the data sheet that accompanies the YIG.

10. Rotate the MANUAL SWEEP control fully clockwise.

11. Adjust A8R42 for the bias voltage specified for 18.6 (or 20) GHz.

b. Osc 3 YIG Bias Check, 660-D-8009 Assembly

1. Set up the test equipment as shown in Figure 5-22, and turn the equipment on.

2. Remove the top cover from the sweep generator. Refer to paragraph 7-3.1 for instructions.

3. Connect the common lead on the digital multimeter (DMM) to A8TP1 (Figure 5-21) and the test lead to A8TP3.

4. Press RESET.

5. Verify the DMM reads +15 ±0.5 volts.

6. Press RF ON to OFF.

7. Verify the DMM reads 0 ±0.5 volts.

5-11 FREQUENCY CALIBRATION

This paragraph provides instructions for calibrating the sweep generator's frequency. The calibrating adjustments are organized by frequency band (Osc 1, HET, Osc 2, and Osc 3). The sweep generator frequency should be checked, and adjusted if necessary, following maintenance on the A2, A5, and A6-A8 PCBs, and when any of the YIG oscillators are replaced.

a. <u>2-8 GHz Band (Osc 1) Frequency Calibration</u>

1. Set up test equipment as shown in Figure 5-23, and turn the equipment on.

2. Remove the top cover from the sweep generator (sweeper). Refer to paragraph 7-3.1 for instructions.

3. Press RESET on sweeper.

CAUTION

To prevent misalignment due to being on the wrong side of the YIG oscillator's hysteresis curve, steps 4 thru 10 should be followed exactly as written.

4. Press CW F1 and set for 2.050 GHz; wait ≈10 s for the frequency to settle.

5. Press CW F2 and set for 7.950 GHz; wait ≈10 s for the frequency to settle.

6. Press CW F1.

7. Using care to prevent the frequency from going below 2.000 GHz, adjust A6R5 (Figure 5-24) for 2.050 GHz ±1 MHz, as indicated on the counter.

8. Press CW F2.

9. Using care to prevent the frequency from going above 8.000 GHz, adjust A6R7 for 7.950 GHz ±1 MHz, as indicated on the counter.

NOTE

In steps 8 and 9, if the frequency goes below 2.000 GHz or above 8.000 GHz, the adjustments are invalid. If this happens, repeat steps 4 thru 9.

10. Repeat steps 6 thru 9, as necessary, until the two frequencies are within tolerance.

11. Press FREQUENCY RANGE F1-F2.

12. Press MANUAL SWEEP and set the associated control fully counterclockwise.

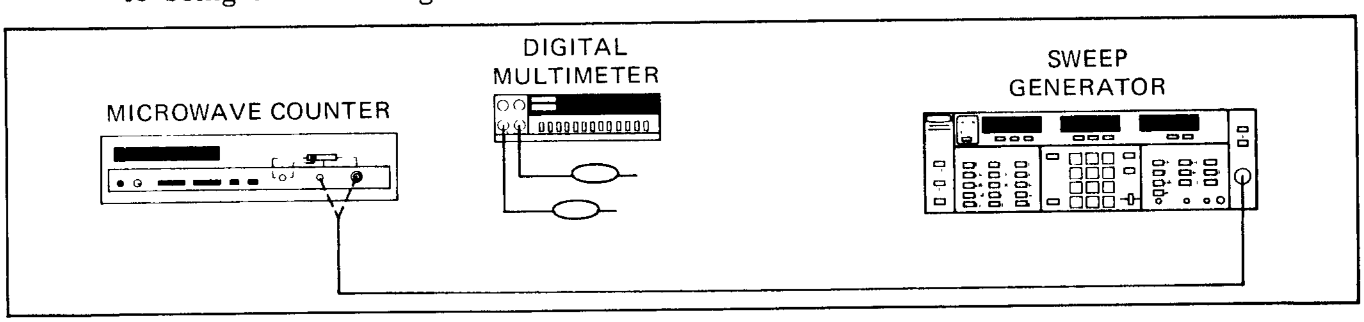


Figure 5-23. Test Equipment Setup for Frequency Calibration

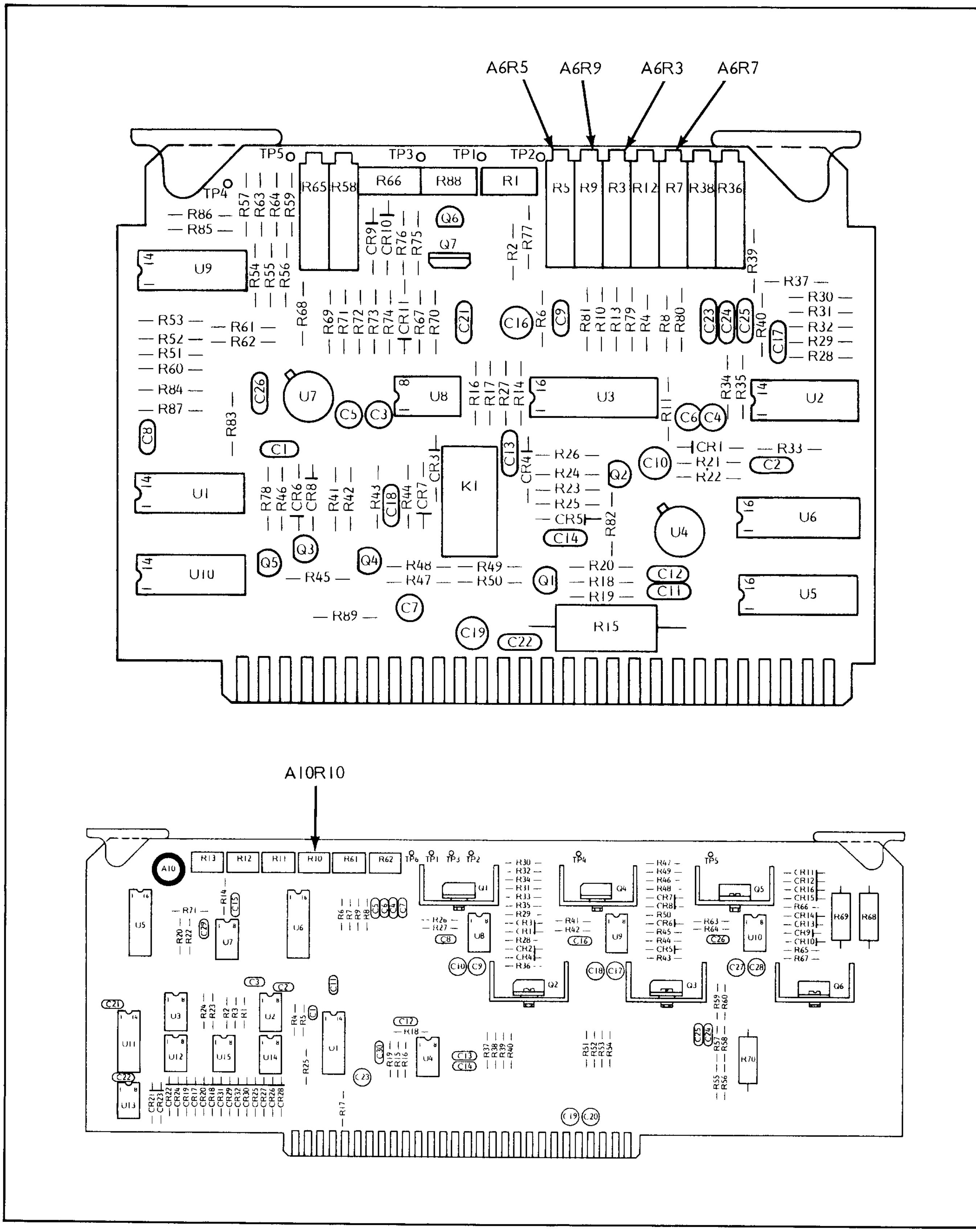


Figure 5-24. 2-8 GHz (Osc 1) Band Frequency Adjustments

13. Adjust A6R3 for a reading of 2.050 GHz ±1 MHz, as indicated on the counter.

14. Press CW F0 and set for 5 GHz.

15. After the frequency has settled, observe and record the counter reading.

16. Press FREQUENCY VERNIER INCREASE and hold depressed until the frequency stops increasing.

17. Adjust A6R9 until the counter reads 12.7 ±0.1 MHz above the frequency recorded in step 15.

18. Press FREQUENCY VERNIER OFF, and note that the counter reads the frequency recorded in step 15.

19. Press FREQUENCY VERNIER DECREASE and hold depressed until the frequency stops decreasing.

20. Verify that the counter reading decreased by 12.7 ±0.1 MHz from the value recorded in step 15.

21. Press FREQUENCY VERNIER OFF.

22. Press FREQUENCY RANGE ΔF F0.

23. Press ΔF and set for 0 MHz.

24. Using the FREQUENCY VERNIER pushbuttons, set the F0 frequency for a counter reading of 5.000 GHz.

25. Rotate the MANUAL SWEEP control between its clockwise and counterclockwise ends and note the frequency at each end.

26. Adjust A10R10 on the FM/Attenuator PCB so that the frequency excursions from 5 GHz are equal, ± 0.5 MHz, at each end of the MANUAL SWEEP control.

b. .01-2 GHz Band (Heterodyne) Frequency Calibration

1. Press CW F1.

2. Press F1 and set for 5.6 GHz.

3. Using the FREQUENCY VERNIER pushbuttons, set the F1 frequency for 5.600 GHz ±1 MHz, as indicated on the counter.

4. With the digital multimeter (DMM) referenced to A6TP1 (Figure 5-25), measure and record the voltage at A6TP2.

5. Reset F1 to 1 GHz.

6. With the DMM still connected to TP2, adjust A6R12 until the DMM reads the same voltage value recorded in step 4.

7. Referring to Figure 5-25, adjust the Heterodyne Down Converter's oscillator for 1.000 GHz ±1 MHz, as indicated on the counter.

c. 8-12.4 GHz Band (Osc 2) Frequency Calibration

CAUTION

To prevent misalignment due to being on the wrong side of the YIG oscillator's hysteresis curve, steps 1 thru 7 should be followed exactly as written.

1. Press FREQUENCY RANGE F1-F2.

2. Press F1 and set for 8.050 GHz; wait ≈10 s for the frequency to settle.

3. Press F2 and set for 12.350 GHz; wait ≈10 s for the frequency to settle.

4. Press CW F1.

5. Using care to prevent the frequency from going below 8.000 GHz, adjust A7R2 (Figure 5-26) for 8.050 GHz ± 1 MHz, as indicated on the counter.

6. Press CW F2.

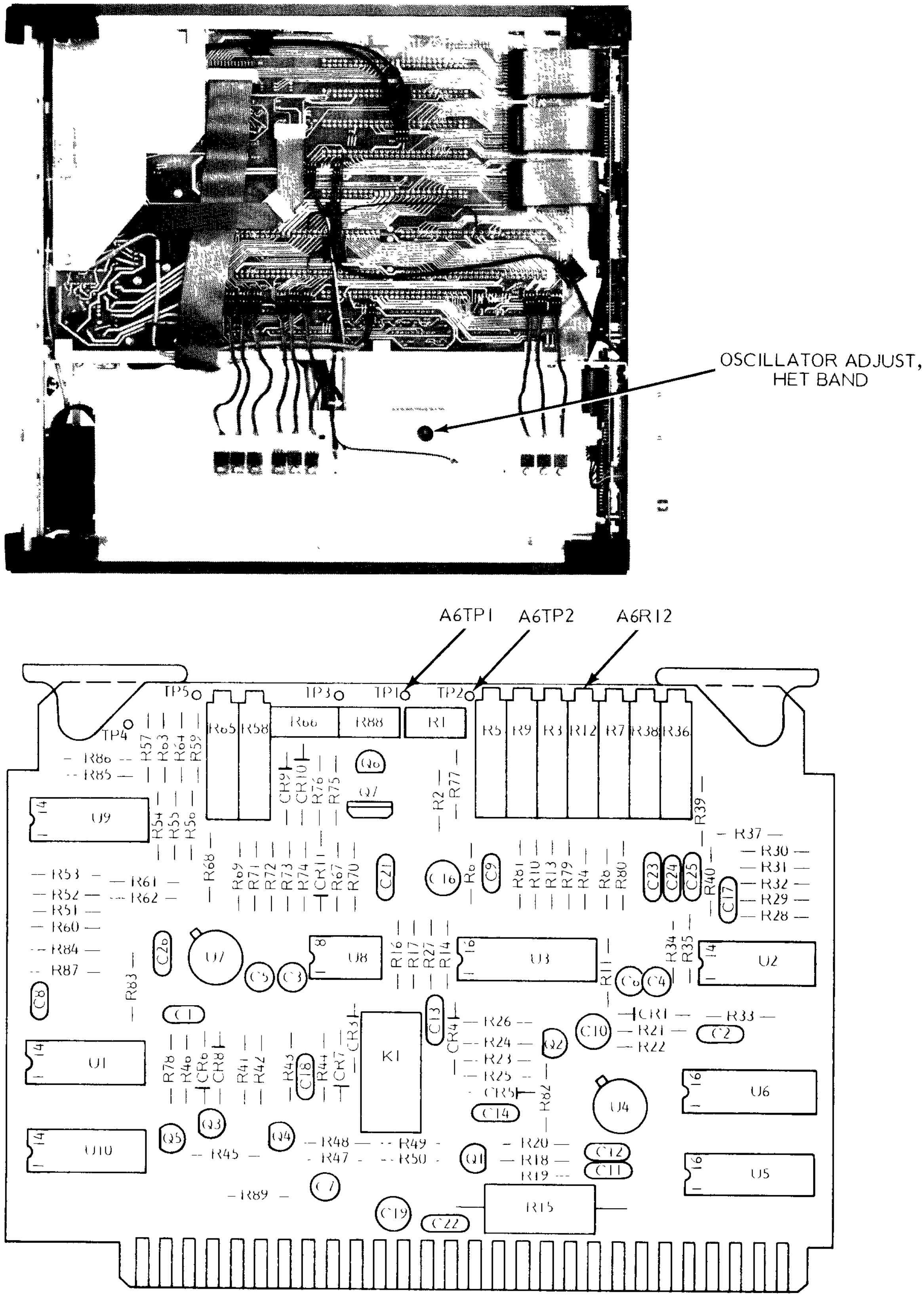
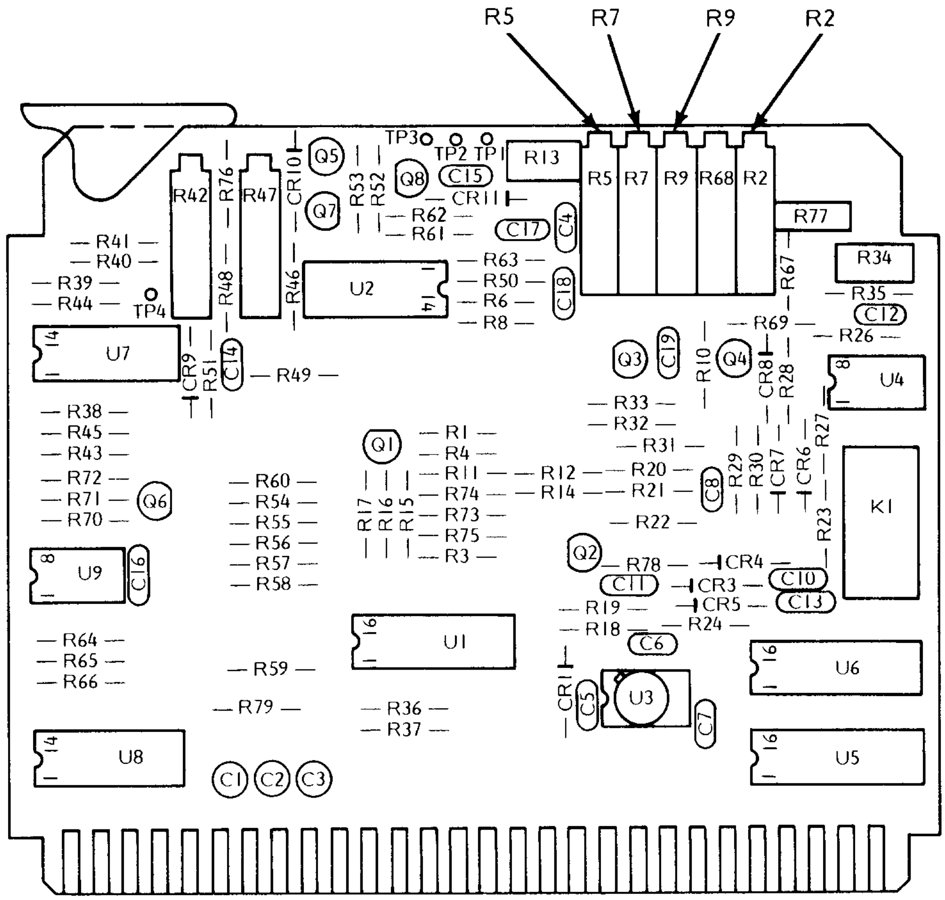


Figure 5-25. .01-2 GHz (Heterodyne) Band Frequency Adjustments



A7, A8 YIG Driver PCBs

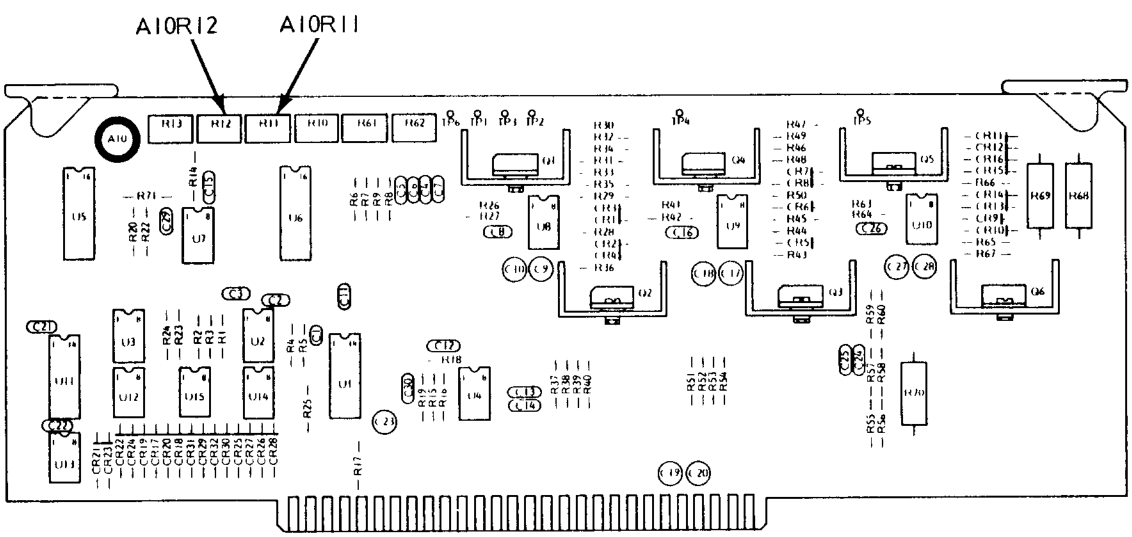


Figure 5-26. 8-12.4 and 12.4-18.6 (or 20) GHz Band (Osc 2 and 3) Frequency Adjustments

7. Using care to prevent the frequency from going above 12.400 GHz, adjust A7R7 for 12.350 GHz ±1 MHz, as indicated on the counter.

NOTE

In steps 5 and 7, if the frequency goes below 8.000 or above 12.400 GHz, the adjustments are invalid. If this happens, repeat steps 1 thru 7.

8. Repeat steps 4 thru 7, as necessary, until the two frequencies are within tolerance.
9. Press FREQUENCY RANGE F1-F2.
10. Press MANUAL SWEEP and set the associated control fully counterclockwise.
11. Adjust A7R5 for a reading of 8.050 GHz ±1 MHz, as indicated on the counter.
12. Press CW F0, and set to 10 GHz.
13. After the frequency has settled, observe and record the counter reading.
14. Press FREQUENCY VERNIER INCREASE and hold depressed until the frequency stops increasing.
15. Adjust A7R9 until the counter reads 12.7 ±0.1 MHz above the frequency recorded in step 13.
16. Press FREQUENCY VERNIER OFF, and note that the counter reads the frequency recorded in step 13.
17. Press FREQUENCY VERNIER DECREASE and hold depressed until the frequency stops decreasing.
18. Verify that the counter reading decreased by 12.7 ±0.1 MHz from the value recorded in step 13.
19. Press FREQUENCY VERNIER OFF.
20. Press FREQUENCY RANGE ΔF F0.
21. Press F0 and set for 10 GHz.
22. Press ΔF and set for 0 MHz.
23. Using the FREQUENCY VERNIER pushbuttons, set the F0 frequency for a counter reading of 10.000 GHz.
24. Rotate the MANUAL SWEEP control between its clockwise and counterclockwise ends and note the frequency at each end.
25. Adjust A10R11 on the FM/Attenuator PCB so that the frequency excursions from 10 GHz are equal, ±0.5 MHz, at each end of the MANUAL SWEEP control.

d. 12.4-18.6 (or 20)* GHz Band (Osc 3) Frequency Calibration

CAUTION

To prevent misalignment due to being on the wrong side of the YIG oscillator's hysteresis curve, steps 1 thru 7 should be followed exactly as written.

1. Press FREQUENCY RANGE F1-F2.
2. Press F1 and set for 12.450 GHz; wait ≈10 s for the frequency to settle.
3. Press F2 and set for 18.550 (or 19.950) GHz; wait ≈10 s for the frequency to settle.
4. Press CW F1.
5. Using care to prevent the frequency from going below 12.400 GHz, adjust A8R2 (Figure 5-26) for 12.450 GHz ±1 MHz, as indicated on the counter.

*In this section, the frequency value in parenthesis applies to Models 6638 and 6648.

6. Press CW F2.

7. Using care to prevent the frequency from going above 18.600 (or 20.000) GHz, adjust A8R7 for 18.550 (or 19.950) GHz ±1 MHz, as indicated on the counter.

NOTE

In steps 5 and 7, if the frequency goes below 12.400 or above 18.600 (or 20.000) GHz, the adjustments are invalid. If this happens, repeat steps 4 thru 7.

8. Repeat steps 4 thru 7, as necessary, until the two frequencies are within tolerance.

9. Press FREQUENCY RANGE F1-F2.

10. Press MANUAL SWEEP and set the associated control fully counterclockwise.

11. Adjust A8R5 for a reading of 12.450 GHz ±1 MHz, as indicated on the counter.

12. Press CW F0, and set for 15 GHz.

13. After the frequency has settled, observe and record the counter reading.

14. Press FREQUENCY VERNIER INCREASE and hold depressed until the frequency stops increasing.

15. Adjust A8R9 until the counter reads 12.7 ±0.1 MHz above the frequency recorded in step 13.

16. Press FREQUENCY VERNIER OFF, and note that the counter reads the frequency recorded in step 13.

17. Press FREQUENCY VERNIER DECREASE and hold depressed until the frequency stops decreasing.

18. Verify that the counter reading decreased by 12.7 ±0.1 MHz below the value recorded in step 13.

19. Press FREQUENCY VERNIER OFF.

20. Press FREQUENCY RANGE ΔF F0.

21. Press F0 and set for 15 GHz.

22. Press ΔF and set for 0 MHz.

23. Using the FREQUENCY VERNIER pushbuttons, set the F0 frequency for a counter reading of 15.000 GHz.

24. Rotate the MANUAL SWEEP control between its clockwise and counterclockwise ends and note the frequency at each end.

25. Adjust A10R12 on the FM/Attenuator PCB so that the frequency excursions from 15 GHz are equal, ± 0.5 MHz, at each end of the MANUAL SWEEP control.

5-12 2-8 GHz BAND (OSC 1) TRACKING FILTER ADJUSTMENTS

This paragraph provides instructions for adjusting the 2-8 GHz band (Osc 1) tracking filter. These adjustments should be performed following maintenance on the A6 PCB or when the power output of the sweep generator is below its specified tolerance in the 2-8 GHz band.

a. Connect test equipment as shown in Figure 5-27, and turn the equipment on.

b. Remove the top cover from the sweep generator (sweeper). Refer to paragraph 7-3.1 for instructions.

c. Press RESET on sweeper.

d. Press FREQUENCY RANGE F1-F2.

e. Press F1 and set for 2 GHz.

f. Press F2 and set for 8 GHz.

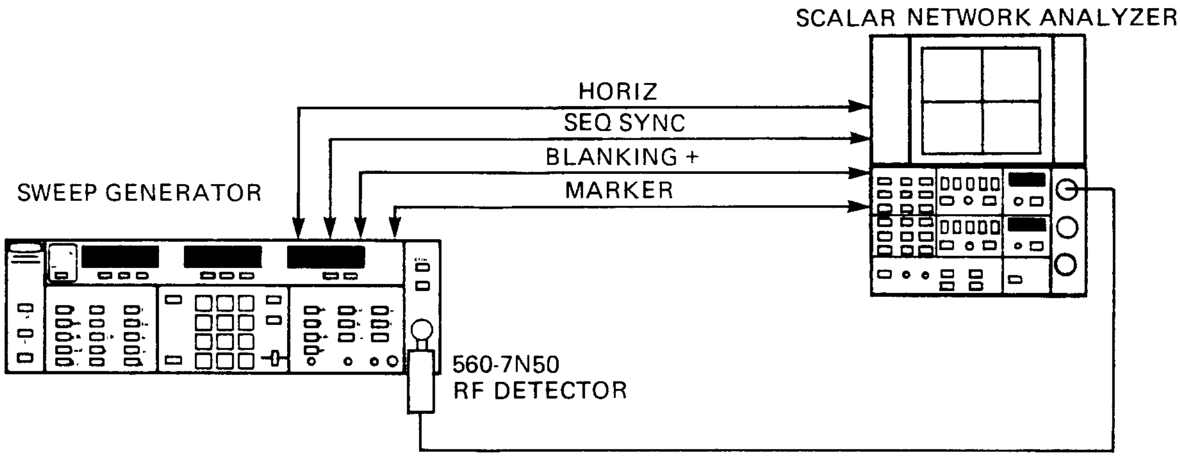
g. Press INTERNAL leveling to the off position (indicator not lit).

h. On 560,

   1. press Channel A REF POS LOCATE and adjust the associated SET potentiometer so that the reference line is positioned on the display's center graticule line;

   2. release REF POS LOCATE;

   3. a trace similar to that shown in Figure 5-28 should be observed.



Initial Control Settings

Scalar Network Analyzer

CHANNEL A ON: On
INPUT: A
MEMORY: Off
dB PER DIVISION: 2
REFERENCE dB/dBm: dBm
SET (screwdriver pot): Midrange
OFFSET: +10.2
CHANNEL B: Not used
MARKER THRESHOLD: Off
REAL TIME: On
SMOOTHING: Off

Figure 5-27. Test Equipment Setup for Tracking Filter Adjustments

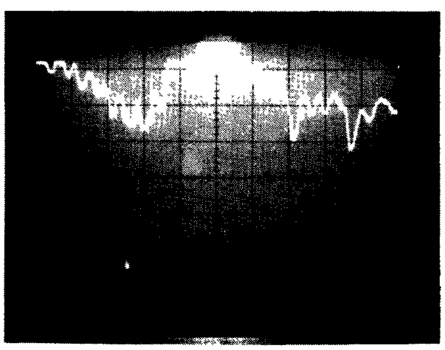


Figure 5-28. F1-F2 Sweep, Unleveled Power

i. On sweeper,

1. alternately adjust A6R36 and A6R38 (Figure 5-30) to obtain maximum output power across the frequency band. A6R36 will adjust power at the low- and A6R38 at the high-end of the frequency band;
2. press INTERNAL leveling;
3. press FULL.

j. On 560, press Channel A .2 dB PER DIVISION.

k. On sweeper,

1. press LEVEL;
2. operate the INCREASE-DECREASE lever to place the minimum-power point of the 560's displayed trace (Figure 5-29) on the center graticule line.

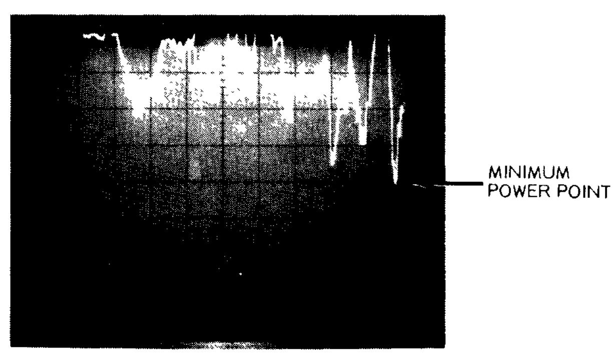


Figure 5-29. Minimum Power Point on Leveled Output Power Signal

3. press ΔF F0;
4. press ΔF and set for 50 MHz;
5. press F0 and set for 2.000 GHz.

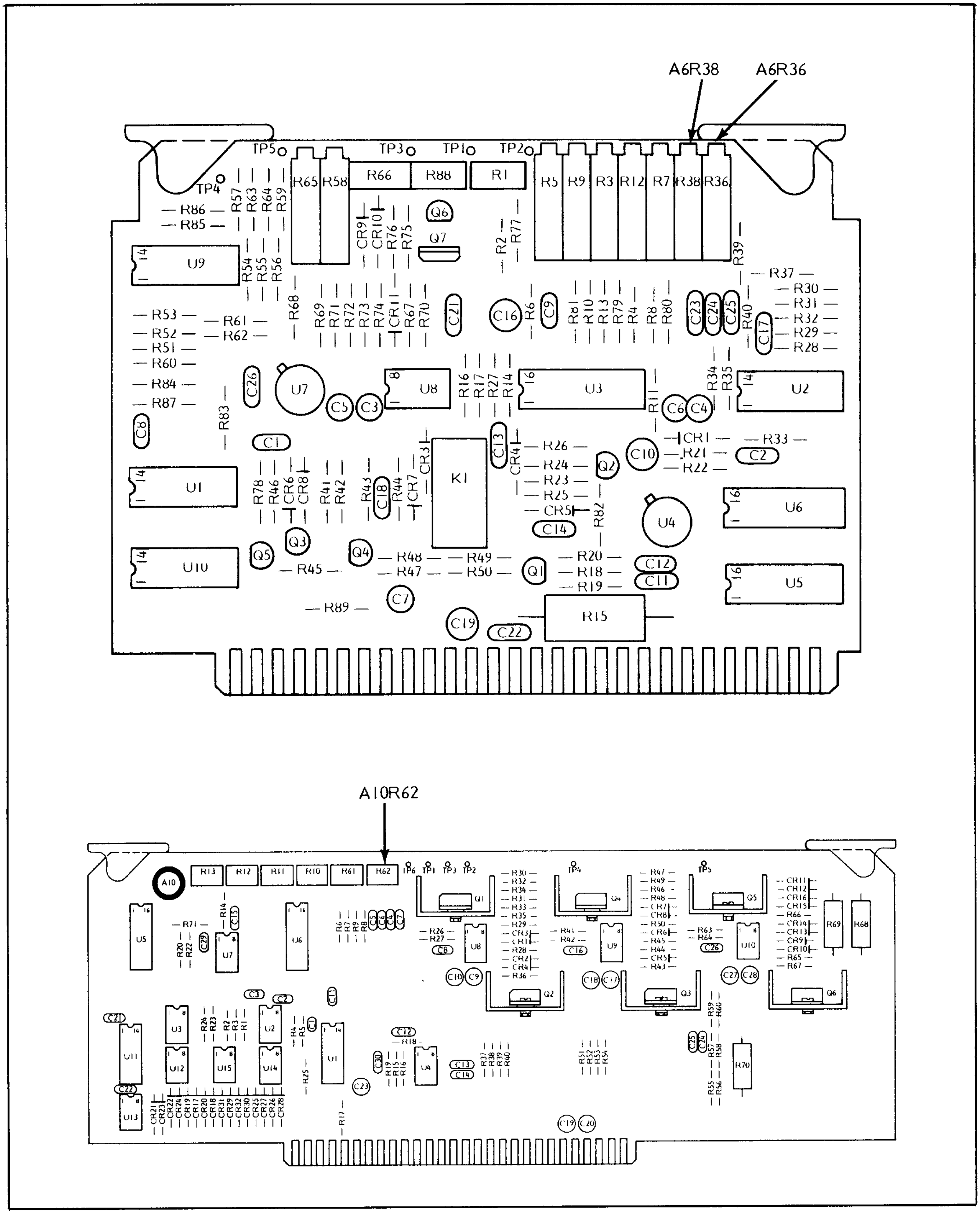


Figure 5-30. Tracking Filter Adjustments

l. On 560, press Channel A .5 dB PER DIVISION. The trace should appear on the top half of the display (Figure 5-31).

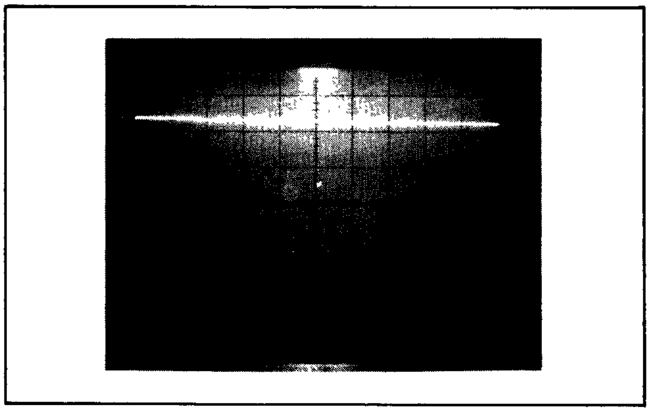


Figure 5-31. Narrow-Band Sweep, Leveled Power

m. On sweeper, move the INCREASE-DECREASE lever toward INCREASE so that the F0 frequency slowly advances, as indicated on the LED numeric display.

n. Observe the 560 display and ensure that the trace does not go unleveled (Figure 5-32) at any frequency between 2 and 8 GHz.

o. If the trace goes unleveled, adjust A10R62 until it becomes leveled (Figure 5-31).

p. Using the INCREASE-DECREASE lever, recheck the ΔF F0 narrow-band sweep and ensure that it has leveled power at all frequencies between 2 and 8 GHz.

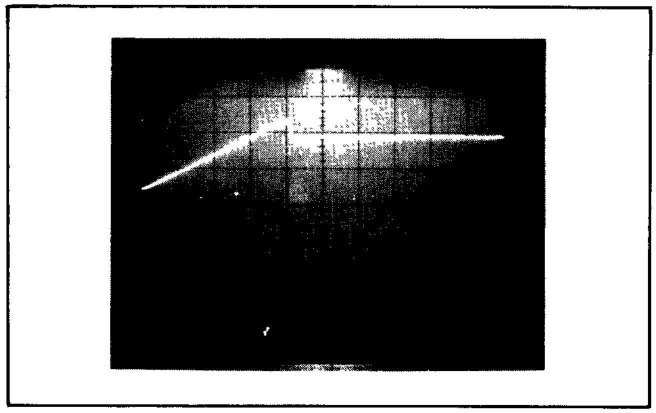


Figure 5-32. Narrow-Band Sweep, Unleveled Power

5-13 SWEEP RATE COMPENSATION ADJUSTMENT

This paragraph provides instructions for adjusting the sweep generator so that the frequency shift is minimum when the sweep rate is varied. This adjustment should be performed following maintenance on any of the A6-A8 PCBs, or when a frequency shift is detected while increasing or decreasing sweep speed.

a. Connect the test equipment as shown in Figure 5-33, and turn the equipment on.

b. Remove the top cover from the sweep generator (sweeper). Refer to paragraph 7-3.1 for instructions.

c. Press RESET.

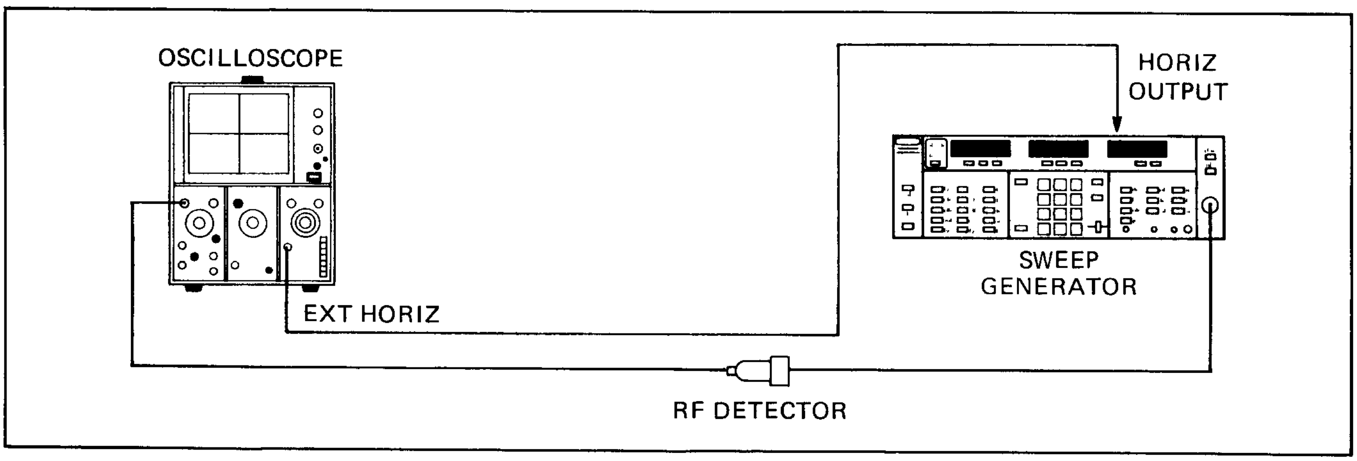


Figure 5-33. Test Equipment Setup for Sweep Rate Compensation Adjustments

d. Press INTERNAL leveling to off (indicator not lit).

e. Press SWEEP TIME and set for 10 ms.

f. Adjust oscilloscope vertical control to obtain a waveform similar to that shown in Figure 5-34.

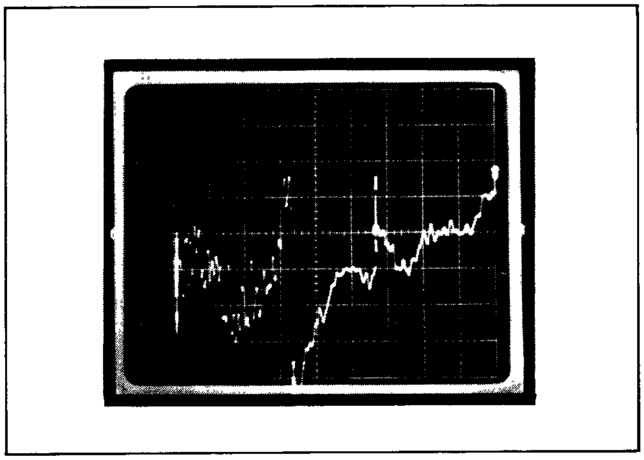


Figure 5-34. Model 6647 Unleveled Full-Band Sweep

g. While monitoring the oscilloscope,

1. select a perturbation to observe in the Osc 1 (2-8 GHz) band (Figure 5-35),

2. alternately change the SWEEP TIME between 10 and 30 ms, and

3. adjust A6R1 (Figure 5-36) for a minimum frequency shift, as indicated by the selected perturbation.

h. Repeat step g. for the Osc 2 and Osc 3 YIG bands. Adjust A7R13 for Osc 2 and A8R13 for Osc 3.

5-14 ALC LOOP CALIBRATION

This paragraph provides instructions for calibrating the sweep generator's ALC (automatic level control) loop. The calibration adjustments in subparagraphs a. thru d. below should be performed following the repair or replacement of any of the ALC loop components (paragraph 7-11.1).

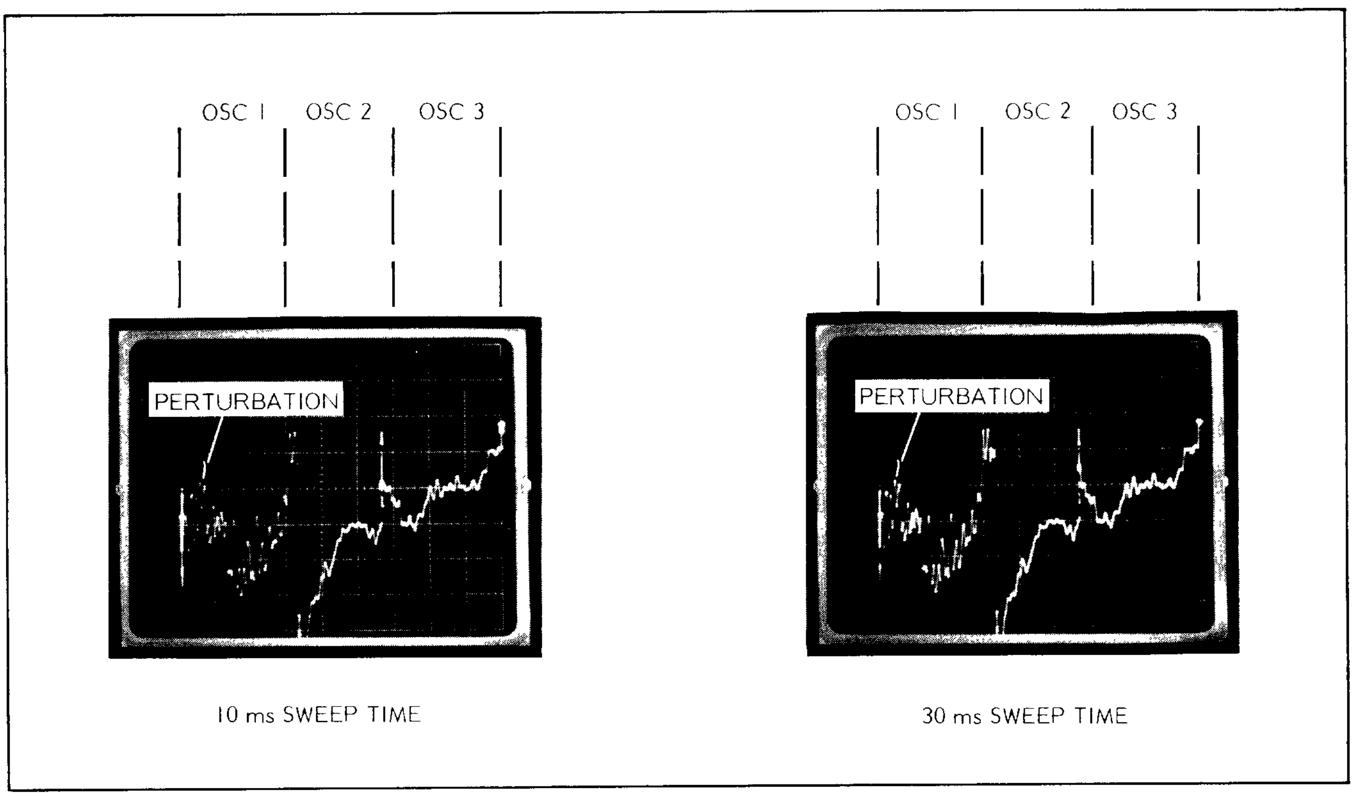


Figure 5-35. Waveforms Showing Frequency Shift with Sweep Time Change

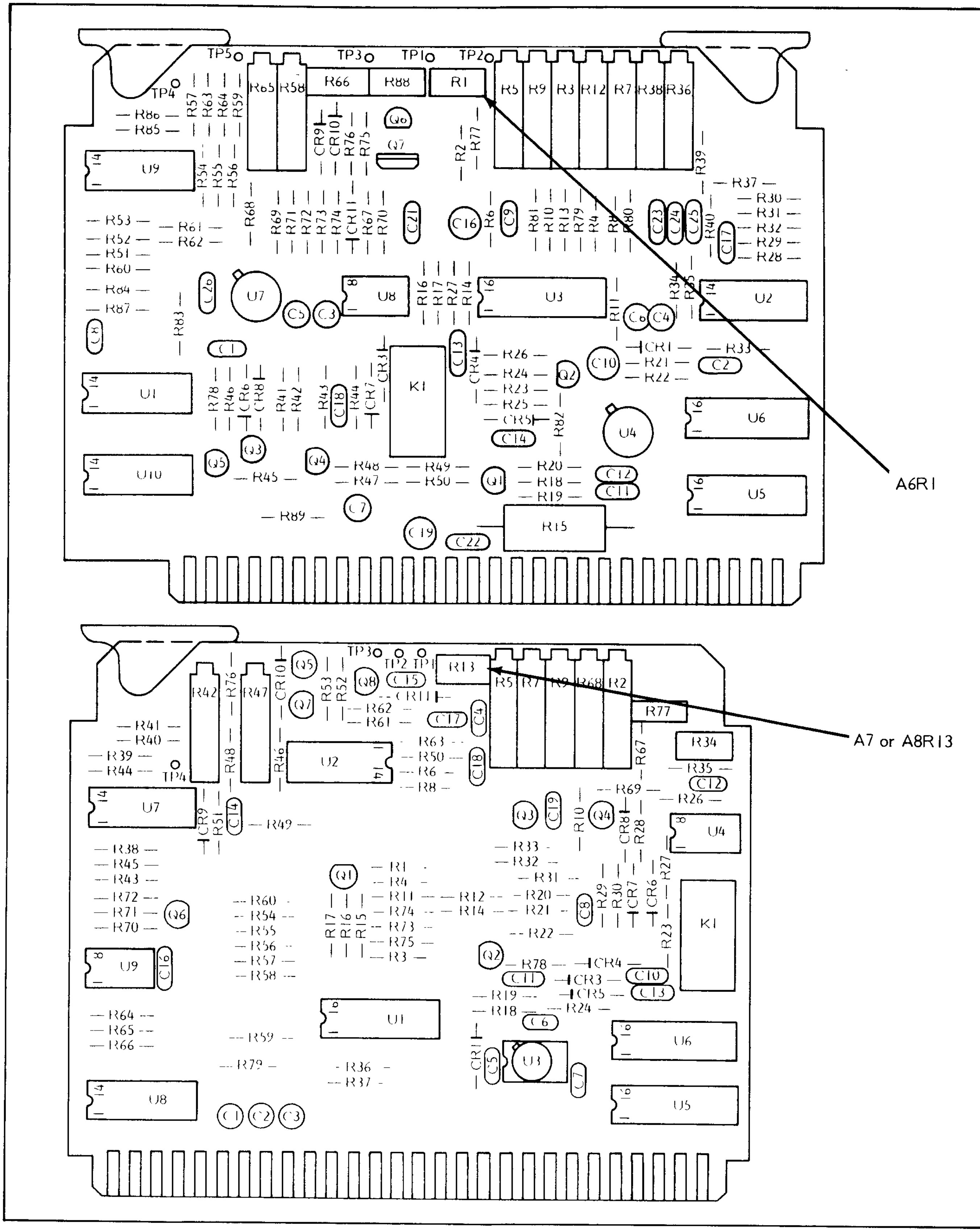


Figure 5-36. Sweep Rate Compensation Adjustments

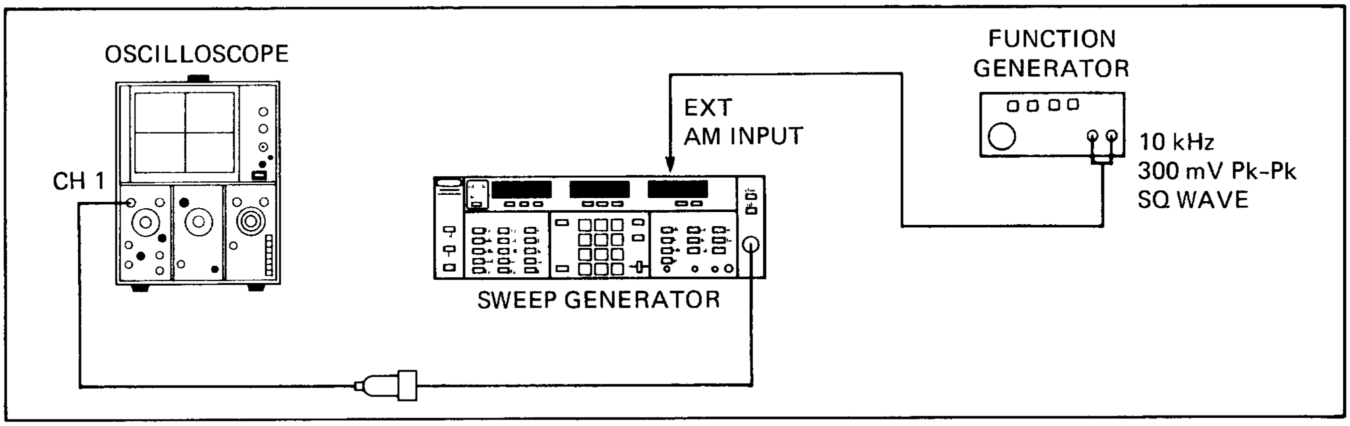


Figure 5-37. Test Equipment Setup for Making ALC Loop Bandwidth Adjustments

a. ALC Loop Bandwidth Adjustments

1. Set up the test equipment as shown in Figure 5-37, and turn the equipment on.
2. Remove the top cover from the sweep generator (sweeper). Refer to paragraph 7-3.1 for instructions.
3. Adjust the function generator to supply the sweeper with a 10 kHz, 300 mV peak-to-peak square wave.
4. Press RESET on sweeper.
5. Press CW F1.
6. Press F1 and set for 5 GHz.
7. Press LEVEL and set for 5 dBm.
8. Adjust the oscilloscope vertical and horizontal controls to display a square wave similar to that shown in Figure 5-38.

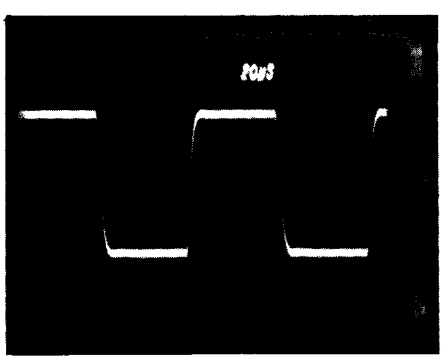


Figure 5-38. ALC Loop Square Wave

9. Alternately adjust A4R123 and A6R66 (Figure 5-39) for the best square-wave response. The square wave should resemble Figure 5-38.
10. For Models 6647/6648,
    (a) press F1 and set for 1 GHz;
    (b) adjust A4R124 and, if necessary, A6R66 for best square-wave response.
11. Set F1 to 10 GHz, and adjust A7R34 for best square-wave response.
12. Set F1 to 15 GHz, and adjust A8R34 for best square-wave response.
13. Reset F1 to 1 GHz (6647/6648).
14. With oscilloscope, verify the following signal parameters at +5, +10, and 0 dBm power-level settings:
    - Overshoot: <20%
    - Rise Time: <7μs.
15. Reset F1 to 5 GHz.
16. Repeat step 14.
17. Reset F1 to 10 GHz.
18. Repeat step 14.
19. Reset F1 to 15 GHz.
20. Repeat step 14.
21. Press POWER to OFF, and disconnect the test equipment.

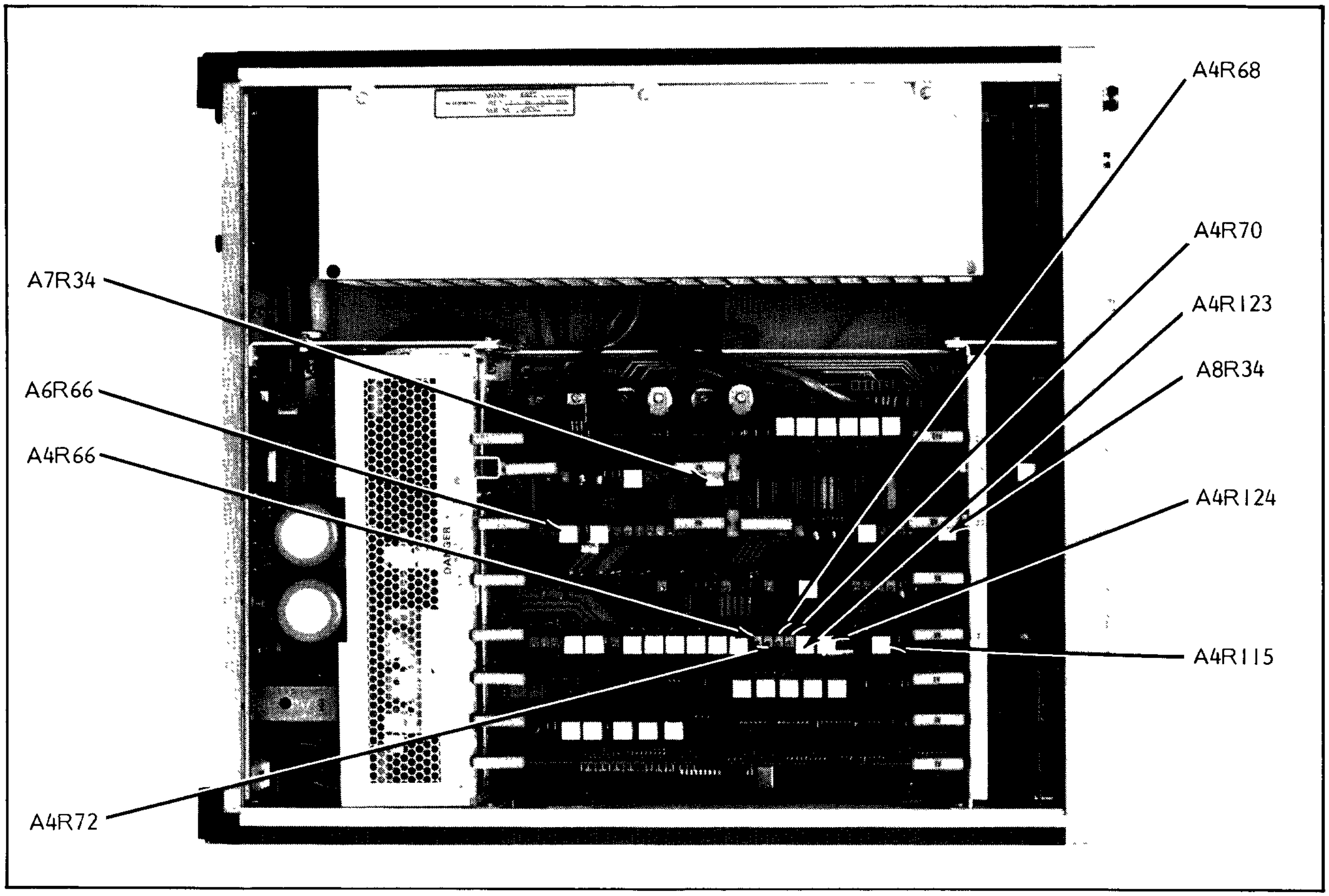


Figure 5-39. ALC Loop Adjustments

b. RF SLOPE Adjustment

1. Set up the test equipment as shown in Figure 5-40, and turn the equipment on.

   (a) Ensure that RF SLOPE is OFF.

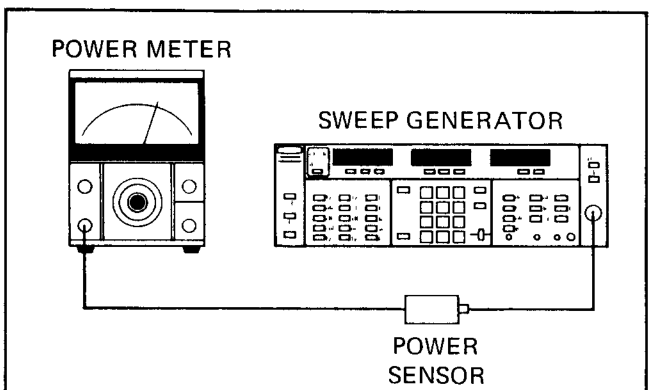


Figure 5-40. Test Equipment Setup for RF SLOPE and Power Level Adjustments

2. Press LEVEL and set for 5 dBm.

NOTE

Ensure the CAL FACTOR control on the power meter is set to the correct value for the F1 frequency.

3. Reset F1 for 2.050 GHz, and record power meter reading.

4. Reset F1 for the high-end frequency (18.6 or 20 GHz), and record the power meter reading.

5. Adjust A4R115 (Figure 5-39) for equal power at both 2.050 GHz and the high-end frequency.

c. Power Level Adjustments

1. Reset F1 for 2.050 GHz.

2. Press LEVEL and set for 10 dBm.

3. Adjust A4R66 (Figure 5-39) for 10 dBm, as indicated on the power meter.

4. Set LEVEL for 0 dBm.

5. Adjust A4R72 for a power meter reading of 0 dBm.

6. Repeat steps 2 thru 5 as necessary until the power levels are 10 dBm and 0 dBm, ±0.1 dBm.

7. Press POWER to OFF, and disconnect the test equipment.

d. Coupler- and 720-Detector-Tracking Adjustment (6647/6648)

1. Set up the test equipment as shown in Figure 5-41, and turn the equipment on.

2. On sweeper,

   (a) press FREQUENCY RANGE ΔF F0;

   (b) press F0 and set for 1 GHz;

   (c) press ΔF and set for 1 GHz.

3. On 560, press REF POS LOCATE, and adjust the SET screwdriver potentiometer to position the reference line to center-screen.

4. On sweeper,

   (a) press LEVEL and set for 10 dBm;

   (b) Adjust A4R142 for a level trace on the 560;

   (c) press F0 and set for 2 GHz.

   (d) adjust A4R68 until the power levels on both sides of the 2 GHz center frequency are approximately equal, as observed on the 560.

5. On 560, readjust the OFFSET control for a 0 dBm reading on the OFFSET dB display.

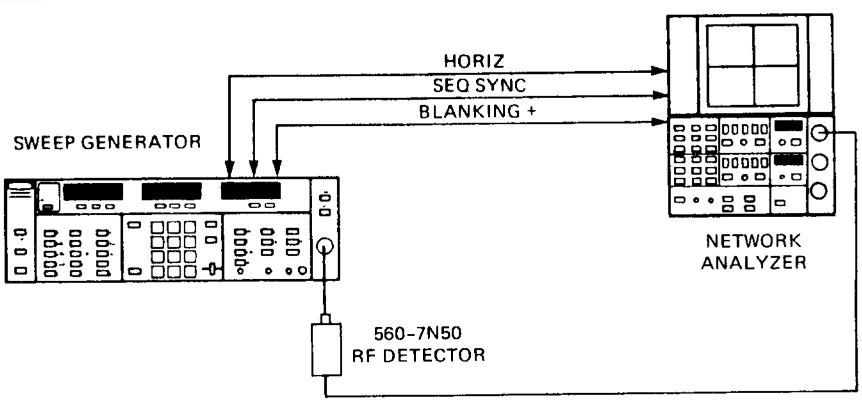
6. On sweeper,

   (a) press LEVEL and set for 0 dBm.

   (b) adjust A4R70 until the power levels on both sides of the 2 GHz center frequency are approximately equal, as observed on the 560.

7. While observing the 560 display and using the 560 OFFSET control to keep the trace on the screen, use the INCREASE-DECREASE lever on the sweeper to vary the power level back and forth between 0 and 10 dBm.

8. Verify that the power levels on both sides of the 2 GHz center frequency are equal, ±0.5 dB. If they are unequal between 0 and 5 dBm, readjust A4R68. Conversely, if they are unequal between 5 and 10 dBm, readjust A4R68.



560 Control Settings

CHANNEL A ON: On
MEMORY: OFF
dB PER DIVISION: .5
REFERENCE dB/dBm: dBm
OFFSET 10 dBm

CHANNEL B ON: Off
REAL TIME: On
SMOOTHING: Off
MARKERS: Off

Figure 5-41. Test Equipment Setup for Detector-Tracking Adjustment

SECTION VI
PARTS LIST

6-1 INTRODUCTION

This section provides parts lists for the Model 6637, 6638, 6647, and 6648 Programmable Sweep Generators. The parts lists are arranged in order of hierarchy, by major assembly. Such assemblies are illustrated in Figures 6-1 through 6-8. The replaceable parts for each printed circuit board (PCB) are tabulated and organized under their next-higher major assembly.

6-2 PARTS ORDERING INFORMATION

Replaceable parts may be ordered either from the local WILTRON representative or directly from the factory.

WILTRON Company
825 East Middlefield Road
Mountain View, California 94043

Telephone: (415) 969-6500
TWX: 910-379-6578

When ordering, give complete information including the model and serial number of the instrument, the full part description, the WILTRON part number, and the quantity required.

6-3 ABBREVIATIONS

The following abbreviations appear in the "DESCRIPTION" column of the WILTRON parts lists:

CC – Carbon Composition
MF – Metal Film
WJ – Watkins-Johnson Company
Dwg – WILTRON Engineering Drawing

6-4 REPLACEABLE PARTS

Illustrated Major Assembly Parts

PCB Parts Lists

PCB Parts List (Cont'd)

INDEX NO.	NAME	PART OR DWG. NO.
1	RF Deck Assembly (See Fig. 6-2)	
	a. Model 6637	660-D-8053-1
	b. Model 6638	660-D-8058-1
	c. Model 6647	660-D-8054-1
	d. Model 6648	660-D-8055-1
2	Basic Frame Assembly (See Fig. 6-4)	660-D-8000
3	Connector Jumper Assembly	660-A-8144
4	Cover, Top and Bottom	660-D-8044
5	Cover, Right Side	660-D-8045
6	Cover, Left Side	660-D-8046
7	Trim Strip, Bottom	560-B-7036
8	Trim Strip, Top	560-B-7037
9	Model Number Nameplate	
	a. 6637	660-B-8093-2
	b. 6638	660-B-8093-8
	c. 6647	660-B-8093-1
	d. 6648	660-B-8093-9
10	Adapter, PCB	660-A-8118
11	Handle Assembly	
	Strap	783-100
	Cap	783-11
	Bracket	783-12
–	Tilt Bail	2000-61F
–	Foot, Bottom	2000-61G
–	Foot, Rear	2000-61H
–	Fuse, Line (2A SB, 3AG)	631-16
–	Cord, Line	800-119
–	Coupler Assembly	660-B-8125
–	Rubber Pad	2000-61K

Figure 6-1. Top Assembly, Dwg. 660-D-8152, -8158, -8151, and -8159 (Sheet 1 of 2)

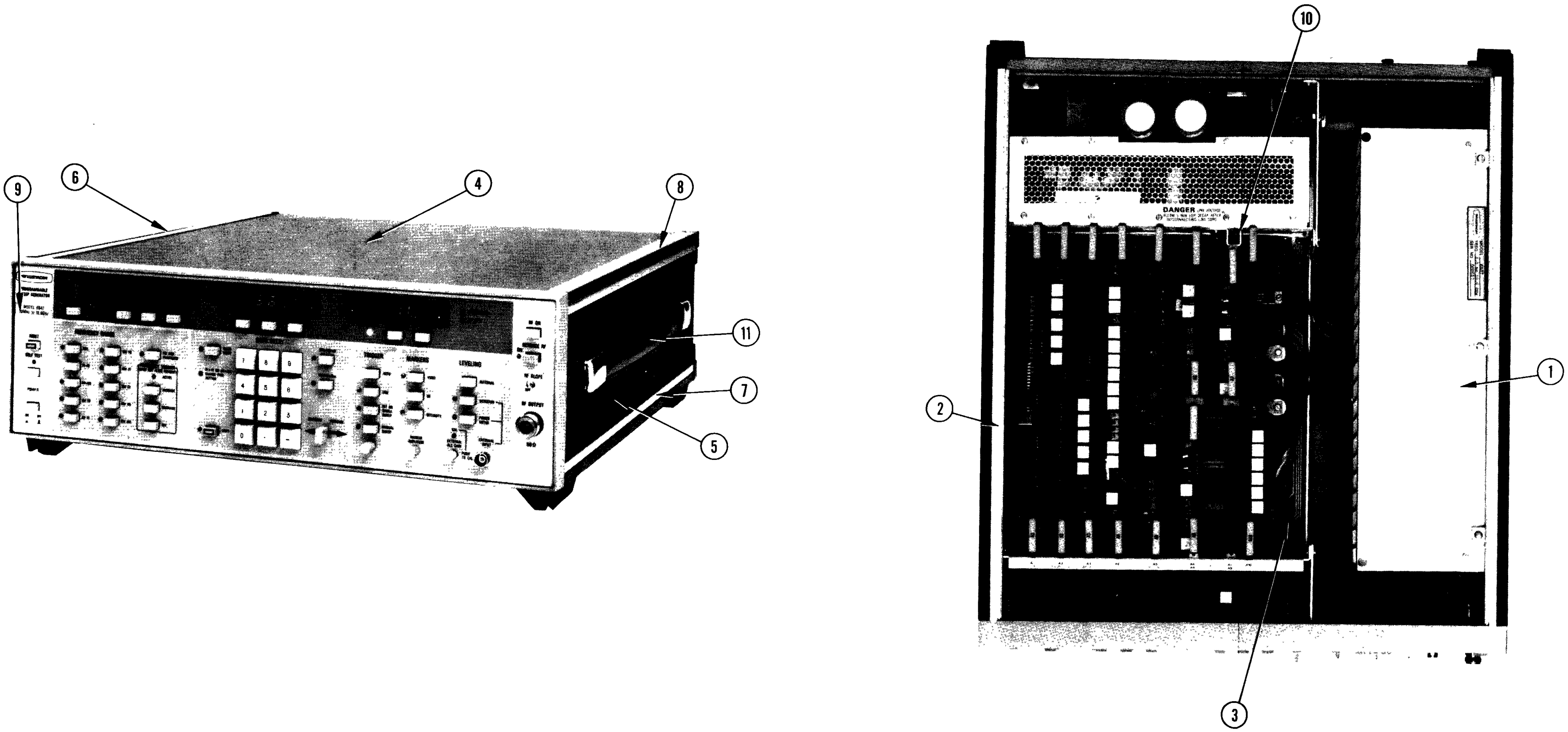
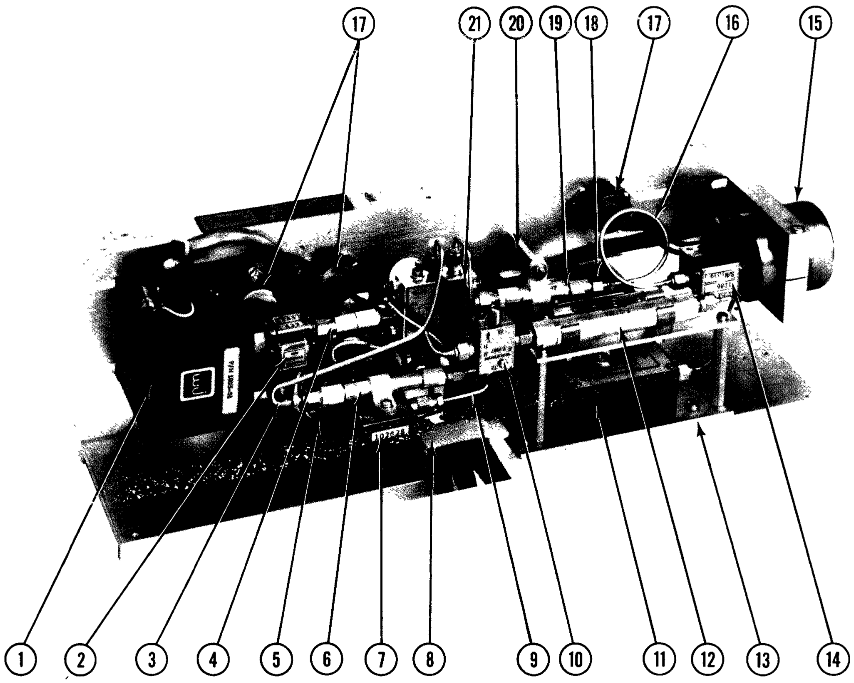


Figure 6-1. Top Assembly, Dwg. 660-D-8152, -8158, -8151, and -8159 (Sheet 2 of 2)



INDEX NO.	NAME	PART OR DWG. NO.
1	Oscillator Assembly, 12.4-18.6 (or 20) GHz (See Figure 6-3)	
	a. 6637/6647	660-C-8085-1
	b. 6638/6648	660-C-8176-1
2	Isolator (p/o Index 1 Oscillator Assembly)	Figure 6-3
3	Cable Coax, RF086 Male-Female (Filter to PIN Switch)	660-A-8102-6
4	Filter (p/o Index 1 Oscillator Assembly)	Figure 6-3
5	Oscillator Assembly, 2-8 GHz (See Fig. 6-3)	660-D-8087-1
6	Filter (p/o Index 5 Oscillator Assembly)	Figure 6-3
7	Matched Modulator (p/o Index 5 Oscillator Assembly)	Figure 6-3
8	Cable Clip	721-17
9	Cable Assembly, RG086 Male-Male (Filter to Modulator)	660-A-8102-2
10	Model 720 Detector (p/o Heterodyne Down Converter)	--
11	Fixed Frequency Oscillator (p/o Heterodyne Down Converter)	--
12	2 GHz Filter (p/o Heterodyne Down Converter)	
13	Heterodyne Down Converter Assembly	660-C-8090-1
14	Isolator (p/o Index 15 Oscillator Assembly)	Figure 6-3
15	Oscillator Assembly, 8-12.4 GHz (See Fig. 6-3)	
	a. WJ YIG	660-C-8086-1
	b. Avantek YIG	660-C-8086-2
16	Cable Assembly, Isolator to Filter	660-A-8102-6
17	Transformer, Compensation	
	a. YIG Osc. P/N 1005-47 (SPEC-A-11016)	320-66
	b. YIG Osc. P/N 1005-29 (SPEC-A-11017)	320-65
	c. YIG Osc. P/N 1005-53 (SPEC-A-11018)	320-63
	d. YIG Osc. P/N 1005-13 (SPEC-A-11019)	320-64
18	Mixer (p/o Heterodyne Down Converter)	--
19	Filter (p/o Index 18 Oscillator Assembly)	Figure 6-3
20	Standoff, 4-40 x 1" long	785-418
21	PIN Switch Assembly	660-D-8821
–	Voltage Regulator, -5V	54-184

Figure 6-2. RF Deck Assembly, Dwg. 660-D-8053-1, -8058-1, -8054-1, and -8055-1 (See Figure 6-1 for next higher assembly)

Reference Photo

INDEX NO.	NAME	PART OR DWG. NO.
1	PCB, YIG Driver	
	a. 2-8 GHz (See Table 6-1)	660-D-8007-3
	b. 8-12.4 GHz	
	1. WJ YIG (See Table 6-2)	660-D-8008-5
	2. Avantek YIG (See Table 6-3)	660-D-8009-4
	c. 12.4-18.6 GHz	
	1. WJ YIG (See Table 6-2)	660-D-8008-4
	2. Avantek YIG (See Table 6-3)	660-D-8009-5
2	Cable, Transistor (3 ea)	660-A-8100
3	Transistors Q1, Q2, Q3;	20-2N6044
	Q1 on Assy. 660-D-8086-2	20-2N6041
4	Cable, SMA Male-Male, RG085	660-A-8101-5
5	YIG Oscillator, 2-8 GHz	1005-46 or -47
6	YIG Oscillator, WJ	
	a. 8-12.4 GHz	1005-54
	b. 12.4-18.6 GHz	1005-51
	c. 12.4-20 GHz	1005 52
7	YIG Oscillator, Avantek	
	a. 8-12.4 GHz	1005-53
	b. 12.4-18.6 GHz	
	c. 12.4-20 GHz	
	Matched Modulator	660-B-9342
8	Isolator	
	a. 7-12.4 GHz	1000-21
	b. 12.4-18.6 GHz	1005-13
	c. 12.4-20 GHz	1000-35
9	Filter	
	a. 2-8 GHz	1030-26
	b. 8-12.4 GHz	1030-29
	c. LP to 20 GHz	1030-32
10	Capacitor, Tantalum, 10 uF	250-42
11	Capacitor, Tantalum, 100 µF	250-50
	On Oscillator 1005-54, capacitor is 10µF	250-42A
12	Capacitor, Tantalum, 10µF	250-42
13	Core, Torroid	640-5
14	Connector Housing, 16-pin	551-247
	Female Pin	551-35
–	Resistor (R1), MF, 1/4W, 1%, 105Ω	110-105-1
–	Cover (for Item 6 oscillator)	660-B-8160

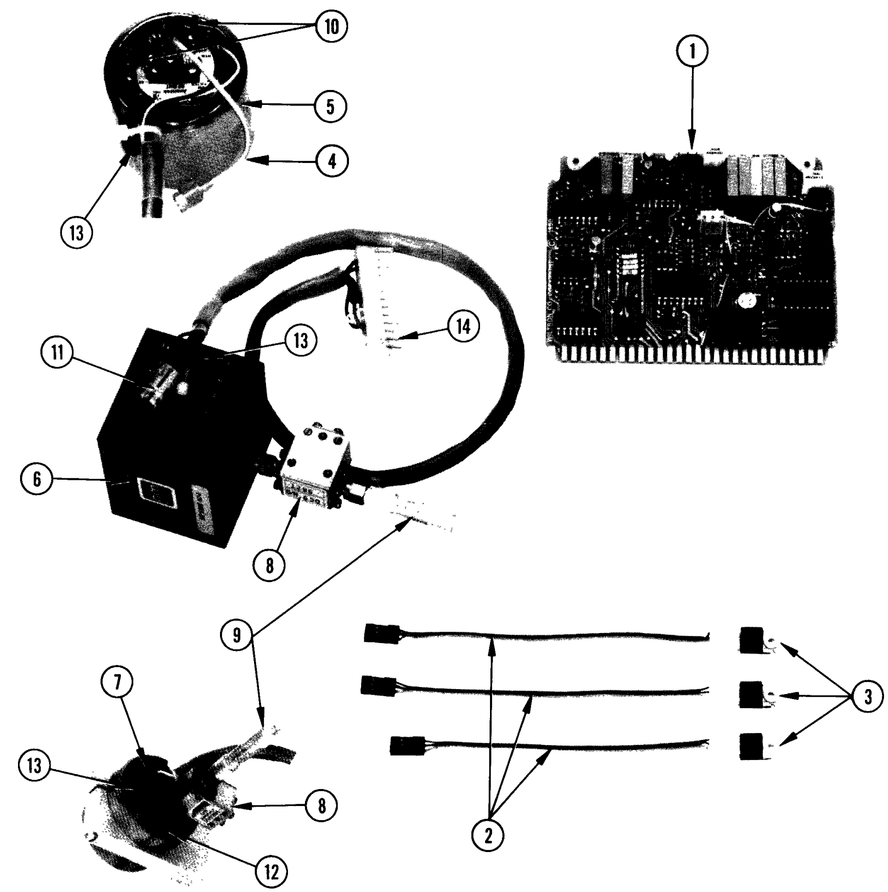


Figure 6-3. Oscillator Assembly, Dwg. 660-D-8087-1, -8086-1 & 2, -8085-1, and -8176-1 (See Figure 6-2 for next higher assembly)

Table 6-1. A6 Het/YIG Driver PCB, Dwg. 660-D-8007-3
(See Figure 6-3 for next higher assembly)

CAPACITORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
C1	Monolithic, .1μF	230-37
C2	Monolithic, .1μF	230-37
C3	Tantalum, 35V, 6.8μF	250-41A
C4	Monolithic, .1μF	230-37
C5	Tantalum, 35V, 6.8μF	250-41A
C6	Monolithic, .1μF	230-37
C7	Tantalum, 35V, 6.8μF	250-41A
C8	Monolithic, .1μF	230-37
C9	Ceramic, .01μF	230-11
C10	Ceramic, .001μF	230-30
C11	Monolithic, .1μF	230-37
C12	Monolithic, .1μF	230-37
C13	Monolithic, 1μF	230-41
C14	Monolithic, .1μF	230-37
C15	Not Used	
C16	Tantalum, 35V, 6.8μF	250-41A
C17	Ceramic, .001μF	230-30
C18	Ceramic, .01μF	230-11
C19	Tantalum, 35V, 6.8μF	250-41A
C20	Mica, 150pF	220-150
C21	Capacitor 8.2pF	221-8.2
C22	Mica, 470pF	220-470
C23	Ceramic, .01μF	230-11
C24	Ceramic, .01μF	230-11
C25	Ceramic, .01μF	230-11
C26	Monolithic, .1μF	230-37

DIODES

REF. DES.	DESCRIPTION	WILTRON PART NO.
CR1	Silicon, 1N4446	10-1N4446
CR2	Not Used	
CR3	Silicon, 1N4446	10-1N4446
CR4	Silicon, SI2	10-SI2
CR5	Zener, 24V, 1W, 1N4749A	10-1N4749A
CR6	Silicon, 1N4446	10-1N4446
CR7	Silicon, 1N4446	10-1N4446
CR8	Zener, 6.8V, 1W, 1N4736A	10-1N4745A
CR9	Silicon, 1N4446	10-1N4446
CR10	Silicon, 1N4446	10-1N4446
CR11	Silicon, 1N4446	10-1N4446

TRANSISTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
Q1	PNP, MPSA92	20-MPSA92
Q2	PNP, MPSA92	20-MPSA92
Q3	PNP, 2N2907	20-2N2907A
Q4	NPN, 2N2222A	20-2N2222A
Q5	PNP, 2N2907	20-2N2907A
Q6	NPN, 2N3694	20-2N3694
Q7	NPN, MPSU04	20-MPSU04

RESISTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
R1	Variable, 1 Turn, 20kΩ	156-20K
R2	MF, 1/4W, 1%, 61.9kΩ	110-61.9k-1
R3	Variable, 10 Turn 1kΩ	157-1k
R4	MF, 1/4W, 1%, 11kΩ	110-11k-1
R5	Variable, 10 Turn, 50kΩ	157-50k
R6	CC, 1/4W, 5%, 3.6MΩ	101-3.6M-5
R7	Variable, 10 Turn, 1kΩ	157-1k
R8	MF, 1/4W, 1%, 11kΩ	110-11k-1
R9	Variable, 10 Turn, 200kΩ	157-200k
R10	MF, 1/4W, 1%, 205kΩ	110-205k-1
R11	MF, 1/4W, 1%, 100kΩ	110-100k-1
R12	Variable, 10 Turn, 20kΩ	157-20k
R13	MF, 1/4W, 1%, 75kΩ	110-75k-1
R14	MF, 1/4W, 1%, 9.76kΩ	110-9.76k-1
R15	Power, 5W, 5Ω	131-3
R16	MF, 1/4W, 1%, 100kΩ	110-100k-1
R17	MF, 1/4W, 1%, 3.24kΩ	110-3.24k-1
R18	MF, 1/4W, 1%, 10kΩ	110-10k-1
R19	MF, 1/4W, 1%, 10kΩ	110-10k-1
R20	MF, 1/4W, 1%, 10kΩ	110-10k-1
R21	MF, 1/4W, 1%, 23.7kΩ	110-23.7k-1
R22	MF, 1/4W, 1%, 1kΩ	110-1k-1
R23	MF, 1/4W, 1%, 121Ω	110-121-1
R24	MF, 1/4W, 1%, 1kΩ	110-1k-1
R25	MF, 1/4W, 1%, 7.5kΩ	110-7.5k-1
R26	MF, 1/4W, 1%, 5.11Ω	110-5.11-1
R27	MF, 1/4W, 1%, 5.11kΩ	110-5.11k-1
R28	MF, 1/4W, 1%, 18.7kΩ	110-18.7k-1
R29	MF, 1/4W, 1%, 536kΩ	110-536k-1
R30	MF, 1/4W, 1%, 18.7kΩ	110-18.7k-1
R31	MF, 1/4W, 1%, 18.7kΩ	110-18.7k-1
R32	MF, 1/4W, 1%, 18.7kΩ	110-18.7k-1
R33	MF, 1/4W, 1%, 18.7kΩ	110-18.7k-1
R34	MF, 1/4W, 1%, 18.7kΩ	110-18.7k-1
R35	MF, 1/4W, 1%, 536kΩ	110-536k-1
R36	Variable, 10 Turn, 2kΩ	157-2k
R37	MF, 1/4W, 1%, 20kΩ	110-20k-1
R38	Variable, 10 Turn, 50kΩ	157-50k
R39	MF, 1/4W, 1%, 205kΩ	110-205k-1
R40	MF, 1/4W, 1%, 75kΩ	110-75k-1
R41	MF, 1/4W, 1%, 10kΩ	110-10k-1
R42	MF, 1/4W, 1%, 30.1kΩ	110-30.1k-1
R43	MF, 1/4W, 1%, 11kΩ	110-11k-1
R44	MF, 1/4W, 1%, 3.24kΩ	110-3.24k-1
R45	MF, 1/4W, 1%, 3.24kΩ	110-3.24k-1
R46	MF, 1/4W, 1%, 1kΩ	110-1k-1
R47	MF, 1/4W, 1%, 511Ω	110-511-1
R48	MF, 1/4W, 1%, 5.11Ω	110-5.11-1
R49	MF, 1/4W, 1%, 5.11Ω	110-5.11-1
R50	MF, 1/4W, 1%, 2.74kΩ	110-2.74k-1
R51	MF, 1/4W, 1%, 10kΩ	110-10k-1
R52	MF, 1/4W, 1%, 750kΩ	110-750k-1
R53	MF, 1/4W, 1%, 14.7kΩ	110-14.7k-1
R54	MF, 1/4W, 1%, 10kΩ	110-10k-1
R55	MF, 1/4W, 1%, 750kΩ	110-750k-1
R56	MF, 1/4W, 1%, 14.7kΩ	110-14.7k-1
R57	MF, 1/4W, 1%, 2.74kΩ	110-2.74k-1
R58	Variable, 10 Turn, 500Ω	157-500
R59	MF, 1/4W, 1%, 2kΩ	110-2k-1

R60	MF, 1/4W, 1%, 10kΩ	110-10k-1
R61	MF, 1/4W, 1%, 750kΩ	110-750k-1
R62	MF, 1/4W, 1%, 14.7kΩ	110-14.7k-1
R63	MF, 1/4W, 1%, 18.2kΩ	110-18.2k-1
R64	MF, 1/4W, 1%, 2kΩ	110-2k-1
R65	Variable, 10 Turn, 500Ω	157-500
R66	Variable, 1 Turn, 500kΩ	156-500k
R67	MF, 1/4W, 1%, 20kΩ	110-20k-1
R68	MF, 1/4W, 1%, 10kΩ	110-10k-1
R69	MF, 1/4W, 1%, 10kΩ	110-10k-1
R70	MF, 1/4W, 1%, 15kΩ	110-15k-1
R71	MF, 1/4W, 1%, 1.24kΩ	110-1.24k-1
R72	MF, 1/4W, 1%, 19.1kΩ	110-19.1k-1
R73	MF, 1/4W, 1%, 1.1kΩ	110-1.1k-1
R74	MF, 1/4W, 1%, 5.11kΩ	110-5.11k-1
R75	MF, 1/4W, 1%, 301Ω	110-301-1
R76	MF, 1/4W, 1%, 1.21kΩ	110-1.21k-1
R77	MF, 1/4W, 1%, 17.8kΩ	110-17.8k-1
R78	MF, 1/4W, 1%, 511Ω	110-511-1
R79	MF, 1/4W, 1%, 10kΩ	110-10k-1
R80	MF, 1/4W, 1%, 10kΩ	110-10k-1
R81	MF, 1/4W, 1%, 205kΩ	110-205k-1
R82	MF, 1/4W, 1%, 2kΩ	110-2k-1
R83	MF, 1/4W, 1%, 18.7kΩ	110-18.7k-1
R84	MF, 1/4W, 1%, 205kΩ	110-205k-1
R85	MF, 1/4W, 1%, 10kΩ	110-10k-1
R86	MF, 1/4W, 1%, 5.11kΩ	110-5.11k-1
R87	MF, 1/4W, 1%, 14.7kΩ	110-14.7k-1

INTEGRATED CIRCUITS

REF. DES.	DESCRIPTION	WILTRON PART NO.
U1	Quad EX-OR Gate, 74LS86	54-125
U2	Quad Op Amp, TL074	54-132
U3	Quad Analog Switch, LF13201	54-20
U4	Op-Amp, OP05	54-87
U5	256 x 4 PROM, 74LS86	56-4
U6	256 x 4 PROM, 74LS86	56-4
U7	Dual Analog Switch, DG200	50-DG200BA
U8	Dual Op-Amp, TL072	54-53
U9	Quad Volt Comparitor, MC3302P	54-MC3302P
U10	Input NAND Gate, 74LS10	54-42

MISCELLANEOUS

REF. DES.	DESCRIPTION	WILTRON PART NO.
—	Ejector, P.C. Board	553-96
—	Ejector, P.C. Board	660-B-8116-6
TP1 thru TP5	Pin, Test Point	706-44
K1	Relay, 2 Form C	690-28
—	Socket, I.C., 16-Pin	553-48

Table 6-2. A7/A8 YIG Driver PCB, Dwg. 660-D-8008-3 & -4
(See Figure 6-3 for next higher assembly)

CAPACITORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
C1	Tantalum, 4.7μF	250-39A
C2	Tantalum, 4.7μF	250-39A
C3	Tantalum, 4.7μF	250-39A
C4	Disc Ceramic, .01μF	230-11
C5	Disc Ceramic, .001μF	230-30
C6	Monolithic, .1μF	230-37
C7	Monolithic, .1μF	230-37
C8	Monolithic, 1.0μF	230-41
C9	Not Used	
C10	Monolithic, .1μF	230-37
C11	Tantalum, 6.8μF	250-41A
C12	Mica, 5pF	220-5
C13	Monolithic, .1μF	230-37
C14	Disc Ceramic, .01μF	230-11
C15	Mica, 300pF	220-300
C16	Monolithic, .1μF	230-37
C17	Disc Ceramic, .01μF	230-11
C18	Disc Ceramic, .01μF	230-11
C19	Disc Ceramic, .01μF	230-11

DIODES

REF. DES.	DESCRIPTION	WILTRON PART NO.
CR1	Silicon, 1N4446	10-1N4446
CR2	Not Used	
CR3	Silicon, SI2	10-SI2
CR4	Zener, 24V, 1W, 1N4749A	10-1N4749A
CR5	Silicon, SI2	10-SI2
CR6	Silicon, 1N4446	10-1N4446
CR7	Silicon, 1N4446	10-1N4446
CR8	Silicon, 1N4446	10-1N4446
CR9	Zener, 10V, 0.4W, 1N758A	10-1N758A
CR10	Silicon, 1N4446	10-1N4446
CR11	Silicon, 1N4446	10-1N4446

TRANSISTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
*Q1	PNP, MPSA92	20-MPSA92
*Q2	PNP, MPSA92	20-MPSA92
*Q3	NPN, 2N3694	20-2N3694
Q4	NPN, 2N2222A	20-2N2222A
Q5	PNP, 2N2907A	20-2N2907A
Q6	NPN, 2N2222A	20-2N2222A
Q7	PNP, 2N2907A	20-2N2907A
Q8	PNP, 2N2907A	20-2N2907A

*A6Q1 - Q3 are shown in Figure 6-3

RESISTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
R1	CC, 1/4W, 5%, 3.3MΩ	101-3.3M-5
R2	Variable, 15 Turn, 50kΩ	157-50k
R3	CC, 1/4W, 5%, 3.6MΩ	101-3.6M-5
R4	MF, 1/4W, 1%, 61.9kΩ	110-61.9k-1
R5	Variable, 15 Turn, 1kΩ	157-1k
R6	MF, 1/4W, 1%, 11kΩ	110-11-1
R7	Variable, 15 Turn, 1kΩ	157-1k
R8	MF, 1/4W, 1%, 11kΩ	110-11-1
R9	Variable, 15 Turn, 200kΩ	157-200k
R10	MF, 1/4W, 1%, 210kΩ	110-210k-1
R11	MF, 1/4W, 1%, 7.87kΩ	110-7.68k-1

R12	MF, 1/4W, 1%, 20kΩ	110-20k-1
R13	Variable, 1 Turn, 20kΩ	156-20k
R14	MF, 1/4W, 1%, 3.16kΩ	110-3.16k-1
R15	MF, 1/4W, 1%, 10kΩ	110-10k-1
R16	MF, 1/4W, 1%, 10kΩ	110-10k-1
R17	MF, 1/4W, 1%, 10kΩ	110-10k-1
R18	MF, 1/4W, 1%, 23.7kΩ	110-23.7k-1
R19	MF, 1/4W, 1%, 1kΩ	110-1k-1
R20	MF, 1/4W, 1%, 121Ω	110-121-1
R21	MF, 1/4W, 1%, 1kΩ	110-1k-1
R22	MF, 1/4W, 1%, 7.5kΩ	110-7.5k-1
R23	MF, 1/4W, 1%, 511Ω	110-511-1
R24	MF, 1/4W, 1%, 5.11kΩ	110-5.11k-1
R25	WW, 5W, 5Ω	131-3
R26	MF, 1/4W, 1%, 10kΩ	110-10k-1
R27	MF, 1/4W, 1%, 750Ω	110-750-1
R28	MF, 1/4W, 1%, 5.49kΩ	110-5.49k-1
R29	MF, 1/4W, 1%, 1.78kΩ	110-1.78k-1
R30	MF, 1/4W, 1%, 2.15kΩ	110-2.15k-1
R31	MF, 1/4W, 1%, 1kΩ	110-1k-1
R32	MF, 1/4W, 1%, Factory-select	Factory-select
R33	MF, 1/4W, 1%, 17.8kΩ	110-17.8k-1
R34	Variable, 1 Turn, 200kΩ	156-200k
R35	MF, 1/4W, 1%, 1kΩ	110-1k-1
R36	MF, 1/4W, 1%, 10kΩ	110-10k-1
R37	MF, 1/4W, 1%, 10kΩ	110-10k-1
R38	MF, 1/4W, 1%, 18.7kΩ	110-18.7k-1
R39	MF, 1/4W, 1%, 18.7kΩ	110-18.7k-1
R40	MF, 1/4W, 1%, 10kΩ	110-10k-1
R41	MF, 1/4W, 1%, 59kΩ	110-59k-1
R42	Variable, 15 Turn, 50kΩ	157-50k
R43	MF, 1/4W, 1%, 18.7kΩ	110-18.7k-1
R44	MF, 1/4W, 1%, 18.7kΩ	110-18.7k-1
R45	MF, 1/4W, 1%, 10kΩ	110-10k-1
R46	MF, 1/4W, 1%, 8.45kΩ	110-8.45k-1
R47	Variable, 15 Turn, 10kΩ	157-10k
R48	MF, 1/4W, 1%, 11kΩ	110-11k-1
R49	MF, 1/4W, 1%, 10kΩ	110-10k-1
R50	MF, 1/4W, 1%, 511Ω	110-511-1
R51	MF, 1/4W, 1%, 4.99kΩ	110-4.99k-1
R52	MF, 1/4W, 1%, 3.83kΩ	110-3.83k-1
R53	MF, 1/4W, 1%, 1kΩ	110-1k-1
R54	MF, 1/4W, 1%, 511Ω	110-511-1
R55	MF, 1/4W, 1%, 8.06Ω	110-8.06-1
R56	MF, 1/4W, 1%, 8.06Ω	110-8.06-1
R57	MF, 1/4W, 1%, 8.06Ω	110-8.06-1
R58	MF, 1/4W, 1%, 8.06Ω	110-8.06-1
R59	Carbon, 1/2W, .5Ω	102-.5-5
R60	MF, 1/4W, 1%, 2.15kΩ	110-2.15k-1
R61	MF, 1/4W, 1%, 10kΩ	110-10k-1
R62	MF, 1/4W, 1%, 8.66Ω	110-8.66k-1
R63	MF, 1/4W, 1%, 10kΩ	110-10k-1
R64	MF, 1/4W, 1%, 10kΩ	110-10k-1
R65	MF, 1/4W, 1%, 750kΩ	110-750k-1
R66	MF, 1/4W, 1%, 14.7kΩ	110-14.7k-1
R67	MF, 1/4W, 1%, 5.11Ω	110-5.11-1
R68	Variable, 15 Turn, 500Ω	157-500
R69	MF, 1/4W, 1%, 2kΩ	110-2k-1
R70	MF, 1/4W, 1%, 10kΩ	110-10k-1
R71	MF, 1/4W, 1%, 750kΩ	110-750k-1
R72	MF, 1/4W, 1%, 14.7kΩ	110-14.7k-1
R73	MF, 1/4W, 1%, 10kΩ	110-10k-1
R74	MF, 1/4W, 1%, 10kΩ	110-10k-1
R75	MF, 1/4W, 1%, 205kΩ	110-205k-1
R76	MF, 1/4W, 1%, 511Ω	110-511-1

INTEGRATED CIRCUITS

REF. DES.	DESCRIPTION	WILTRON PART NO.
U1	Quad Analog Switch, LF13201	54-20
U2	NAND Gate, 74LS10	54-42
U3	Op Amp, OP05	54-87
U4	Quad Op Amp, TL072	54-53
U5	256 x 4 PROM, 74S387	56-4
U6	256 x 4 PROM, 74S387	56-4
U7	Quad Op Amp, TL074	54-132
U8	Quad Ex. OR Gate, 74LS86	54-125
U9	Dual Volt. Comp., LM393	54-158

MISCELLANEOUS

REF. DES.	DESCRIPTION	WILTRON PART NO.
—	Ejector, PC Board	553-96
TP1 thru TP4	Pin, Test Point	706-44
K1	Relay, 2 Form C	690-28
—	Socket, I.C., 16-Pin	553-48

Table 6-3. A7/A8 YIG Driver PCB, Dwg. 660-D-8009-3 & -4
(See Figure 6-3 for next higher assembly)

CAPACITORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
C1	Tantalum, 4.7μF	250-39A
C2	Tantalum, 4.7μF	250-39A
C3	Tantalum, 4.7μF	250-39A
C4	Disc Ceramic, .01μF	230-11
C5	Disc Ceramic, .001μF	230-30
C6	Monolithic, .1μF	230-37
C7	Monolithic, .1μF	230-37
C8	Monolithic, 1.0μF	230-41
C9	Not Used	
C10	Monolithic, .1μF	230-37
C11	Tantalum, 6.8μF	250-41A
C12	Mica, 5pF	220-5
C13	Monolithic, .1μF	230-37
C14	Disc Ceramic, .01μF	230-11
C15	Not used	
C16	Monolithic, .1μF	230-37
C17	Disc Ceramic, .01μF	230-11
C18	Disc Ceramic, .01μF	230-11
C19	Disc Ceramic, .01μF	230-11
C20	Mica, 300pF	220-300

DIODES

REF. DES.	DESCRIPTION	WILTRON PART NO.
CR1	Silicon, 1N4446	10-1N4446
CR2	Not Used	
CR3	Silicon, SI2	10-SI2

CR4	Zener, 24V, 1W, 1N4749A	10-1N4749A
CR5	Silicon, SI2	10-SI2
CR6	Silicon, 1N4446	10-1N4446
CR7	Silicon, 1N4446	10-1N4446
CR8	Silicon, 1N4446	10-1N4446
CR9	Zener, 10V, 0.4W, 1N758A	10-1N758A
CR10	Silicon, 1N4446	10-1N4446
CR11	Silicon, 1N4446	10-1N4446

TRANSISTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
*Q1	PNP, MPSA92	20-MPSA92
*Q2	PNP, MPSA92	20-MPSA92
*Q3	NPN, 2N3694	20-2N3694
Q4	NPN, 2N2222A	20-2N2222A
Q5	NPN, 2N2222A	20-2N2222A
Q6	PNP, 2N2907A	20-2N2907A
Q7	NPN, 2N2222A	20-2N2222A
Q8	NPN, 2N2222A	20-2N2222A

*A7 and A8Q1 - Q3 are shown in Figure 6-3.

RESISTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
R1	CC, 1/4W, 5%, 3.3MΩ	101-3.3M-5
R2	Variable, 15 Turn, 50kΩ	157-50k
R3	CC, 1/4W, 5%, 3.6MΩ	101-3.6M-5
R4	MF, 1/4W, 1%, 61.9kΩ	110-61.9k-1
R5	Variable, 15 Turn, 1kΩ	157-1k
R6	MF, 1/4W, 1%, 11kΩ	110-11k-1
R7	Variable, 15 Turn, 1kΩ	157-1k
R8	MF, 1/4W, 1%, 11kΩ	110-11k-1
R9	Variable, 15 Turn, 200kΩ	157-200k
R10	MF, 1/4W, 1%, 205kΩ	110-205k-1
R11[1]	MF, 1/4W, 1%, 10.5kΩ	110-10.5k-1
R11[2]	MF, 1/4W, 1%, 10kΩ	110-10k-1
R12	MF, 1/4W, 1%, 20kΩ	110-20k-1
R13	Variable, 1 Turn, 20kΩ	156-20k
R14	MF, 1/4W, 1%, 2.74kΩ	110-2.74k-1
R15	MF, 1/4W, 1%, 10kΩ	110-10k-1
R16	MF, 1/4W, 1%, 10kΩ	110-10k-1
R17	MF, 1/4W, 1%, 10kΩ	110-10k-1
R18	MF, 1/4W, 1%, 23.7kΩ	110-23.7k-1
R19	MF, 1/4W, 1%, 1kΩ	110-1k-1
R20	MF, 1/4W, 1%, 121Ω	110-121-1
R21	MF, 1/4W, 1%, 1kΩ	110-1k-1
R22	MF, 1/4W, 1%, 7.5kΩ	110-7.5k-1
R23	MF, 1/4W, 1%, 511Ω	110-511-1
R24	MF, 1/4W, 1%, 5.11kΩ	110-5.11k-1
R25	WW, 5W, 5Ω	131-3
R26	MF, 1/4W, 1%, 10kΩ	110-10k-1
R27	MF, 1/4W, 1%, 750Ω	110-750-1
R28	MF, 1/4W, 1%, 5.49kΩ	110-5.49k-1
R29	MF, 1/4W, 1%, 1.78kΩ	110-1.78k-1
R30	MF, 1/4W, 1%, 2.15kΩ	110-2.15k-1
R31	MF, 1/4W, 1%, 1kΩ	110-1k-1
R32	MF, 1/4W, 1%, 1.21kΩ	110-1.21k-1
R33	MF, 1/4W, 1%, 17.8kΩ	110-17.8k-1
R34	Variable, 1 Turn, 200kΩ	156-200k
R35	MF, 1/4W, 1%, 1kΩ	110-1k-1
R36	MF, 1/4W, 1%, 10kΩ	110-10k-1
R37	MF, 1/4W, 1%, 10kΩ	110-10k-1
R38	MF, 1/4W, 1%, 18.7kΩ	110-18.7k-1
R39	MF, 1/4W, 1%, 18.7kΩ	110-18.7k-1
R40	MF, 1/4W, 1%, 10kΩ	110-10k-1
R41	MF, 1/4W, 1%, 59kΩ	110-59k-1
R42	Variable, 15 Turn, 50kΩ	157-50k
R43	MF, 1/4W, 1%, 18.7kΩ	110-18.7k-1
R44	MF, 1/4W, 1%, 18.7kΩ	110-18.7k-1
R45	MF, 1/4W, 1%, 10kΩ	110-10k-1
R46	MF, 1/4W, 1%, 9.53kΩ	110-9.53k-1
R47	Variable, 15 Turn, 1kΩ	157-1k
R48	MF, 1/4W, 1%, 11kΩ	110-11k-1
R49	MF, 1/4W, 1%, 10kΩ	110-10k-1
R50	MF, 1/4W, 1%, 511Ω	110-511-1
R51	MF, 1/4W, 1%, 4.99kΩ	110-4.99k-1
R52	MF, 1/4W, 1%, 3.83kΩ	110-3.83k-1
R53	MF, 1/4W, 1%, 1kΩ	110-1k-1
R54	MF, 1/4W, 1%, 511Ω	110-511-1
R55[1]	MF, 1/4W, 1%, 6.49Ω	110-6.49-1
R55[2]	MF, 1/4W, 1%, 6.19Ω	110-6.19-1
R56[1]	MF, 1/4W, 1%, 6.49Ω	110-6.49-1
R56[2]	MF, 1/4W, 1%, 6.19Ω	110-6.19-1
R57[1]	MF, 1/4W, 1%, 6.49Ω	110-6.49-1
R57[2]	MF, 1/4W, 1%, 6.19Ω	110-6.19-1
R58[1]	MF, 1/4W, 1%, 6.49Ω	110-6.49-1
R58[2]	MF, 1/4W, 1%, 6.19Ω	110-6.19-1
R59[1]	MF, 1/4W, 1%, 6.49Ω	110-6.49-1
R59[2]	MF, 1/4W, 1%, 6.19Ω	110-6.19-1
R60	MF, 1/4W, 1%, 2.15kΩ	110-2.15k-1
R61	MF, 1/4W, 1%, 10kΩ	110-10k-1
R62	MF, 1/4W, 1%, 10.7kΩ	110-10.7k-1
R63	MF, 1/4W, 1%, 10kΩ	110-10k-1
R64	MF, 1/4W, 1%, 10kΩ	110-10k-1
R65	MF, 1/4W, 1%, 750kΩ	110-750k-1
R66	MF, 1/4W, 1%, 14.7kΩ	110-14.7k-1
R67	MF, 1/4W, 1%, 866Ω	110-866-1
R68	Variable, 15 Turn, 500Ω	157-500
R69	MF, 1/4W, 1%, 2kΩ	110-2k-1
R70	MF, 1/4W, 1%, 10kΩ	110-10k-1
R71	MF, 1/4W, 1%, 750kΩ	110-750k-1
R72	MF, 1/4W, 1%, 14.7kΩ	110-14.7k-1
R73	MF, 1/4W, 1%, 10kΩ	110-10k-1
R74	MF, 1/4W, 1%, 10kΩ	110-10k-1
R75	MF, 1/4W, 1%, 205kΩ	110-205k-1
R76	MF, 1/4W, 1%, 511Ω	110-511-1

INTEGRATED CIRCUITS

REF. DES.	DESCRIPTION	WILTRON PART NO.
U1	Quad Analog Switch, LF13201	54-20
U2	NAND Gate, 74LS10	54-42
U3	Op Amp, OP05	54-87
U4	Dual Op Amp, TL072	54-53
U5	256 x 4 PROM, 74S387	56-4
U6	256 x 4 PROM, 74S387	56-4
U7	Quad Op Amp, TL074	54-132
U8	Quad Ex. OR Gate 74LS86	54-125
U9	Dual Volt. Comp., LM393	54-158

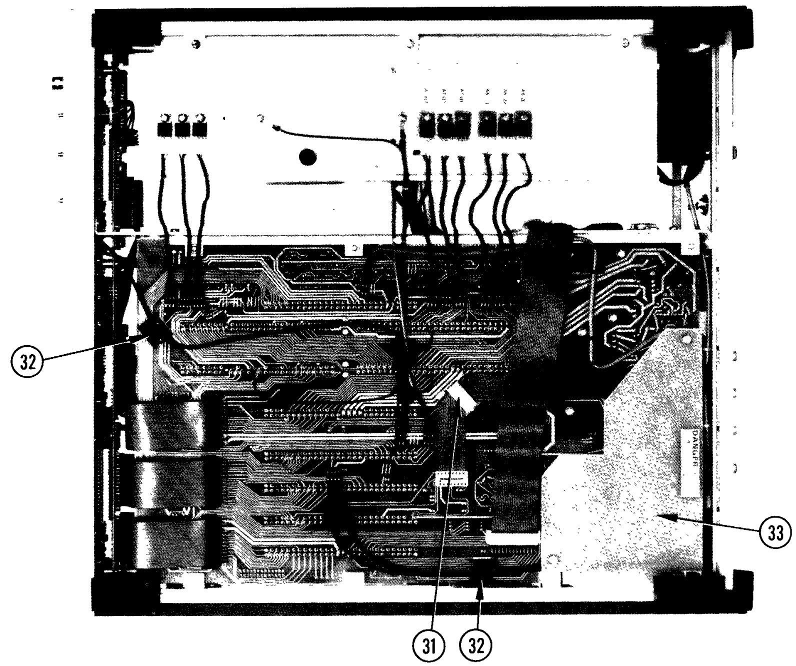
MISCELLANEOUS

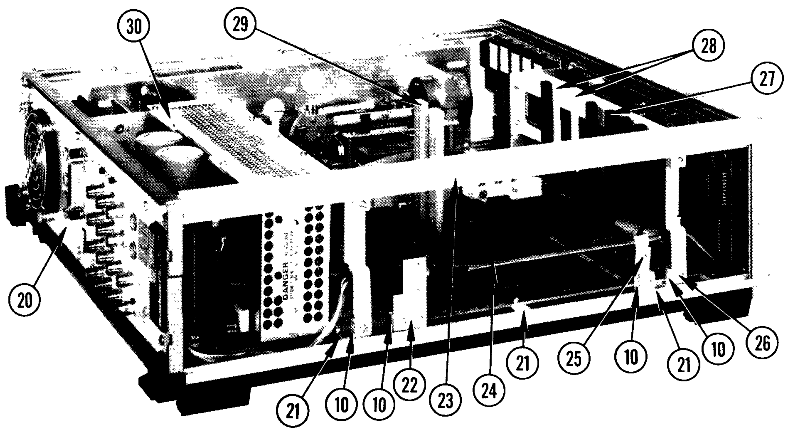
—	Ejector, P.C. Board	553-96
TP1 thru TP4	Pin, Test Point	706-44
K1	Relay, 2 Form C	690-28
—	Socket, I.C., 16-Pin	553-48

[1]Used with 660-D-8009-4 assembly.
[2]Used with 660-D-8009-7 assembly.

INDEX NO.	NAME	PART OR DWG. NO.
1	A2 Ramp Generator PCB (See Table 6-4)	660-D-8002-3
2	A3 Marker Generator PCB (See Table 6-5)	660-D-8003-3
3	A4 Automatic Level Control (ALC) PCB (See Table 6-6)	660-D-8004-3
4	A5 Frequency Instruction PCB (See Table 6-7)	660-D-8005-3
5	A10 FM/Attenuator PCB (See Table 6-8)	660-D-8010-3
6	A14 Motherboard PCB (See Table 6-10)	660-D-8014-3
7	A15 Front Panel Assembly (See Fig. 6-5)	660-D-8015
8	Casting, Finished Front	660-D-8084
9	Bracket, Support, Front	660-B-8030
10	Clip, Mounting (Heat sink & bracket for PCB and POWER switch support)	660-B-8031
11	Card Cage, Front	660-D-8069
12	Bracket, Support, Rear	660-B-8034
13	Transistor, TIP 117	20-5
14	Casting, Finished Rear	660-D-8083
15	Cable Assembly (Regulator to Motherboard)	660-A-8033
16	Card Cage, Rear	660-D-8070
17	A13 Switching Power Supply PCB (See Table 6-9)	660-D-8013-3
18	Bracket, PCB, Rear	660-B-8028
19	Bracket, PCB, Front	660-B-8027
20	A16 Rear Panel Assembly (See Fig. 6-6)	660-D-8016
21	Clip, Mounting (PCB)	660-B-8032
22	Plate, POWER Switch Mounting	560-A-7053
23	Extrusion, Corner Frame	660-B-8082
24	POWER Switch Extender Assembly	660-D-8025
25	Clip, Mounting, POWER Switch	560-B-7044
26	Plate, POWER Switch Support	660-A-8099
27	Guide, PCB	553-97
28	Guide, PCB	553-41
–	Heat Sink	553-65
29	Guide, PCB	660-A-8035
30	Card Cage, Top	660-B-8068
31	Clip, Flat Cable	721-16
32	Clip, Coax Cable	721-15
33	Shield, Voltage Protection	660-B-8072
–	Angle Support, PCB	660-B-8029
–	Regulator, +15V, 7815	54-MC7815CP
–	Regulator, -15V, 7915	54-MC7915CP
–	Regulator, -15V, µA79HGKC	54-145
–	Insulator, Mica	790-70
–	Clamp, Cable	720-3/16
–	Washer, Shoulder	790-52

Figure 6-4. Basic Frame Assembly, Dwg. 660-D-8000
(See Figure 6-1 for next higher assembly) (Sheet 1 of 2)





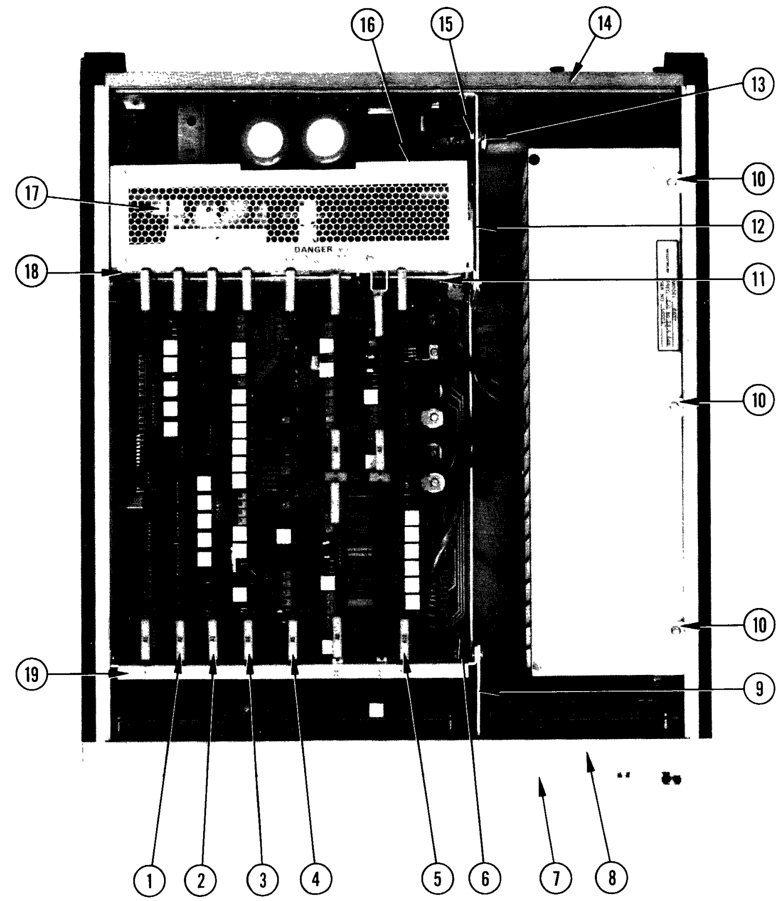


Figure 6-4. Basic Frame Assembly, Dwg. 660-D-8000 (See Figure 6-1 for next higher assembly) (Sheet 2 of 2)

Table 6-4. A2 Ramp Generator PCB, Dwg. 660-D-8002-3
(See Figure 6-4 for next higher assembly)

CAPACITORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
C1	Tantalum, 6V, 68µF	250-58
C2	Monolithic, 50V, .1µF	230-37
C3	Monolithic, 50V, .1µF	230-37
C4	Monolithic, 50V, .1µF	230-37
C5	Monolithic, 50V, .1µF	230-37
C6	Monolithic, 50V, .1µF	230-37
C7	Monolithic, 50V, .1µF	230-37
C8	Monolithic, 50V, .1µF	230-37
C9	Monolithic, 50V, .1µF	230-37
C10	Mica, 250V, 270pF	223-270
C11	Monolithic, 50V, .01µF	250-77
C12	Monolithic, 50V, .01µF	250-77
C13	Monolithic, 50V, .1µF	230-37
C14	Monolithic, 50V, .1µF	230-37
C15	Monolithic, 50V, .1µF	230-37
C16	Monolithic, 50V, .1µF	230-37
C17	Monolithic, 50V, .1µF	230-37
C18	Monolithic, 50V, .1µF	230-37
C19	Monolithic, 50V, .1µF	230-37
C20	Monolithic, 50V, .1µF	230-37
C21	Monolithic, 50V, .1µF	230-37
C22	Monolithic, 50V, .1µF	230-37
C23	Mylar, 250V, 1µF	210-36
C24	Tantalum, 25V, 10µF	250-42
C25	Tantalum, 25V, 10µF	250-42
C26	Monolithic, 50V, .1µF	230-37

DIODES

REF. DES.	DESCRIPTION	WILTRON PART NO.
CR1	Silicon, 1N4446	10-1N4446
CR2	Reference, 1N823, 6.2V, 0.4W	10-1N823
CR3	Silicon, 1N4446	10-1N4446
CR4	Zener, 1N751A, 5.1V, 0.4W	10-1N751A
CR5	Silicon, 1N4446	10-1N4446
CR6	Silicon, 1N4446	10-1N4446
CR7	Silicon, 1N4446	10-1N4446
CR8	Silicon, 1N4446	10-1N4446
CR9	Zener, 1N751A, 5.1V, 0.4W	10-1N751A
CR10	Hot-carrier, MBD-501	10-4
CR11	Zener, 1N758A, 10V, 0.4W	10-1N758A
CR12	Silicon, 1N4446	10-1N4446
CR13	Zener, 1N751A, 5.1V, 0.4W	10-1N751A
CR14	Zener, 1N746A, 3.3V, 0.4W	10-1N746A
CR15	Zener, 1N751A, 5.1V, 0.4W	10-1N751A

TRANSISTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
Q1	2N3694, PNP, 0.2W	20-2N3694
Q2	2N4249, NPN, 0.4W	20-2N4249
Q3	2N3694, PNP, 0.2W	20-2N3694
Q4	2N3694, PNP, 0.2W	20-2N3694
Q5	2N3694, PNP, 0.2W	20-2N3694
Q6	2N4249, NPN, 0.4W	20-2N4249
Q7	2N3694, PNP, 0.2W	20-2N3694
Q8	J112, JFET	20-17
Q9	J112, JFET	20-17
Q10	2N3694, PNP, 0.2W	20-2N3694

RESISTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
R1	MF, 1/4W, 1%, 1.15kΩ	110-1.15k-1
R2	MF, 1/4W, 1%, 8.66kΩ	110-8.66k-1
R3	MF, 1/4W, 1%, 10kΩ	110-10k-1
R4	MF, 1/4W, 1%, 9.76kΩ	110-9.76k-1
R5	MF, 1/4W, 1%, 56.2Ω	110-56.2-1
R6	Variable, 1/2W, 10%, 200kΩ	156-200k
R7	MF, 1/4W, 1%, 1MΩ	110-1M-1A
R8	MF, 1/4W, 1%, 4.99kΩ	110-4.99k-1
R9	MF, 1/4W, 1%, 2.74kΩ	110-2.74k-1
R10	Variable, 1/2W, 10%, 10kΩ	156-10k
R11	MF, 1/4W, 1%, 10.2kΩ	110-10.2k-1
R12	MF, 1/4W, 1%, 10kΩ	110-10k-1
R13	MF, 1/4W, 1%, 1.07kΩ	110-1.07k-1
R14	MF, 1/4W, 1%, 19.6kΩ	110-19.6k-1
R15	MF, 1/4W, 1%, 10kΩ	110-10k-1
R16	MF, 1/4W, 1%, 392kΩ	110-392k-1
R17	Variable, 1/2W, 10%, 500kΩ	156-500k
R18	MF, 1/4W, 1%, 3.48kΩ	110-3.48k-1
R19	MF, 1/4W, 1%, 10kΩ	110-10k-1
R20	MF, 1/4W, 1%, 100Ω	110-100-1
R21	MF, 1/4W, 1%, 2.43kΩ	110-2.43k-1
R22	MF, 1/4W, 1%, 10kΩ	110-10k-1
R23	MF, 1/4W, 1%, 10kΩ	110-10k-1
R24	MF, 1/4W, 1%, 10kΩ	110-10k-1
R25	MF, 1/4W, 1%, 10kΩ	110-10k-1
R26	MF, 1/4W, 1%, 20kΩ	110-20k-1
R27	MF, 1/4W, 1%, 10kΩ	110-10k-1
R28	MF, 1/4W, 1%, 10kΩ	110-10k-1
R29	MF, 1/4W, 1%, 10kΩ	110-10k-1
R30	MF, 1/4W, 1%, 1.1kΩ	110-1.1k-1
R31	Variable, 1/2W, 10%, 2kΩ	156-2k
R32	MF, 1/4W, 1%, 9.53kΩ	110-9.53k-1
R33	MF, 1/4W, 1%, 20kΩ	110-20k-1
R34	MF, 1/4W, 1%, 49.9kΩ	110-49.9k-1
R35	MF, 1/4W, 1%, 100Ω	110-100-1
R36	MF, 1/4W, 1%, 14.7kΩ	110-14.7k-1
R37	MF, 1/4W, 1%, 10kΩ	110-10k-1
R38	MF, 1/4W, 1%, 14.7kΩ	110-14.7k-1
R39	Variable, 1/2W, 10%, 1kΩ	156-1k
R40	MF, 1/4W, 1%, 14.7kΩ	110-14.7k-1
R41	CC, 1/4W, 5%, 2.2M	101-2.2M-5
R42	MF, 1/4W, 1%, 49.9kΩ	110-49.9k-1
R43	MF, 1/4W, 1%, 14.7kΩ	110-14.7k-1
R44	MF, 1/4W, 1%, 20kΩ	110-20k-1
R45	MF, 1/4W, 1%, 10kΩ	110-10k-1
R46	MF, 1/4W, 1%, 10kΩ	110-10k-1
R47	MF, 1/4W, 1%, 4.99kΩ	110-4.99k-1
R48	MF, 1/4W, 1%, 20kΩ	110-20k-1
R49	MF, 1/4W, 1%, 20kΩ	110-20k-1
R50	MF, 1/4W, 1%, 140kΩ	110-140k-1
R51	MF, 1/4W, 1%, 10kΩ	110-10k-1
R52	MF, 1/4W, 1%, 4.99kΩ	110-4.99k-1
R53	MF, 1/4W, 1%, 10kΩ	110-10k-1
R54	MF, 1/4W, 1%, 10kΩ	110-10k-1
R55	MF, 1/4W, 1%, 10kΩ	110-10k-1
R56	MF, 1/4W, 1%, 10kΩ	110-10k-1
R57	MF, 1/4W, 1%, 10kΩ	110-10k-1
R58	MF, 1/4W, 1%, 10kΩ	110-10k-1

REF. DES.	DESCRIPTION	WILTRON PART NO.
R59	MF, 1/4W, 1%, 34k	110-34k-1
R60	MF, 1/4W, 1%, 10kΩ	110-10k-1
R61	MF, 1/4W, 1%, 3.48kΩ	110-3.48k-1
R62	MF, 1/4W, 1%, 10kΩ	110-10k-1
R63	MF, 1/4W, 1%, 10kΩ	110-10k-1
R64	MF, 1/4W, 1%, 20kΩ	110-20k-1
R65	MF, 1/4W, 1%, 10kΩ	110-10k-1
R66	MF, 1/4W, 1%, 140kΩ	110-140k-1
R67	MF, 1/4W, 1%, 10kΩ	110-10k-1

INTEGRATED CIRCUITS

REF. DES.	DESCRIPTION	WILTRON PART NO.
U1	Dual D-Flip-Flop, 74LS74	54-44
U2	Quad AND, 74LS08	54-74LS08
U3	Timer, NE-555	54-555
U4	Counter, 74LS161	54-60
U5	Hex Inverter, 74LS04	54-74LS04
U6	Decoder, 74LS138	54-74LS138
U7	Octal Latch, 74LS374	54-41
U8	2-1 Multiplexer, 74LS157	54-59
U9	4-Bit Counter, 74LS191	54-120
U10	Quad Inverter, 74LS05	54-105
U11	Dual D-Flip-Flop, 74LS74	54-44
U12	2-1 Multiplexer, 74LS157	54-59
U13	4-Bit Counter, 74LS191	54-120
U14	Octal Latch, 74LS374	54-41
U15	8-Bit Latch/DAC, AD7524	54-129
U16	Dual D-Flip-Flop, 74LS74	54-44
U17	Quad NAND Gate, 74LS00	54-74LS00
U18	Dual Op-Amp, TL072	54-53
U19	Data Selector, 74LS151	54-119
U20	Dual Op-Amp, TL072	54-53
U21	Quad Switch, DG201	54-24
U22	Dual D-Flip-Flop, 74LS74	54-44
U23	4-Input NAND, 74LS20	54-74LS20
U24	Dual D-Flip-Flop, 74LS74	54-44
U25	QUAD Comparator, LM339	54-45
U26	Quad NAND, 74LS01	54-74LS01

MISCELLANEOUS

REF. DES.	DESCRIPTION	WILTRON PART NO.
S1	Slide Switch	420-14
TP1 thru TP5	Test Points	706-44
---	Ejector, P.C. Board	553-96

Table 6-5. A3 Marker Generator PCB, Dwg. 660-D-8003-3
(See Figure 6-4 for next higher assembly)

CAPACITORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
C1	Tantalum, 68μF, 6V	250-58
C2	Monolithic, .1μF, 50V	230-37
C3	Monolithic, .1μF, 50V	230-37
C4	Monolithic, .1μF, 50V	230-37
C5	Not Used	
C6	Not Used	
C7	Tantalum, 10μF, 25V	250-42
C8	Tantalum, 10μF, 25V	250-42
C9	Monolithic, .1μF, 50V	230-37
C10	Monolithic, .1μF, 50V	230-37
C11	Tantalum, 10μF, 25V	250-42
C12	Monolithic, .1μF, 50V	230-37
C13	Monolithic, .1μF, 50V	230-37
C14	Mica, 20pF	220-20
C15	Mica, 20pF	220-20
C16	Mica, 20pF	220-20
C17	Monolithic, .1μF, 50V	230-37
C18	Monolithic, .1μF, 50V	230-37
C19	Monolithic, .1μF, 50V	230-37
C20	Monolithic, .1μF, 50V	230-37
C21	Mica, 3pF	223-3
C22	Mica, 3pF	223-3
C23	Monolithic, .1μF, 50V	230-37
C24	Monolithic, .1μF, 50V	230-37
C25	Monolithic, .1μF, 50V	230-37
C26	Monolithic, .1μF, 50V	230-37
C27	Monolithic, .01μF, 100V	250-77
C28	Monolithic, .01μF, 100V	250-77
C29	Mica, 150pF	220-150
C30	Tantalum, 10μF, 25V	250-42
C31	Monolithic, .1μF, 50V	230-37
C32	Tantalum, 10μF, 25V	250-42
C33	Monolithic, .01μF, 100V	250-77
C34	Monolithic, .1μF, 50V	230-37
C35	Monolithic, .1μF, 50V	230-37

DIODES

REF. DES.	DESCRIPTION	WILTRON PART NO.
CR1	Reference, 1N823, 6V	10-1N823
CR2	Shottky, MBD-501	10-4
CR3	Not Used	
CR4	Shottky, MBD-501	10-4
CR5	Not Used	
CR6	Shottky, MBD-501	10-4
CR7	Not Used	
CR8	Zener, 30V, 5%, 1W	10-1N4751A
CR9	Signal, 1N4446	10-1N4446
CR10	Signal, 1N4446	10-1N4446
CR11	Signal, 1N4446	10-1N4446
CR12	Signal, 1N4446	10-1N4446
CR13	Signal, 1N4446	10-1N4446
CR14	Signal, 1N4446	10-1N4446
CR15	Signal, 1N4446	10-1N4446
CR16	Signal, 1N4446	10-1N4446
CR17	Zener, 30V, 5%, 1W	10-1N4751A
CR18	Signal, 1N4446	10-1N4446
CR19	Signal, 1N4446	10-1N4446
CR20	Signal, 1N4446	10-1N4446
CR21	Signal, 1N4446	10-1N4446
CR22	Signal, 1N4446	10-1N4446
CR23	Zener, 3.3V, 5%, .4W	10-1N746A
CR24	Signal, 1N4446	10-1N4446
CR25	Signal, 1N4446	10-1N4446
CR26	Signal, 1N4446	10-1N4446
CR27	Zener, 4.7V, 5%, .4W	10-11
CR28	Signal, 1N4446	10-1N4446

TRANSISTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
Q1	FET, J112	20-17
Q2	FET, J112	20-17
Q3	FET, J112	20-17
Q4	NPN, 2N3694	20-2N3694
Q5	NPN, 2N3694	20-2N3694
Q6	NPN, 2N3694	20-2N3694

RESISTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
R1	MF, 1/4W, 1%, 10kΩ	110-10k-1
R2	MF, 1/4W, 1%, 10kΩ	110-10k-1
R3	MF, 1/4W, 1%, 10kΩ	110-10k-1
R4	MF, 1/4W, 1%, 10kΩ	110-10k-1
R5	MF, 1/4W, 1%, 10kΩ	110-10k-1
R6	MF, 1/4W, 1%, 10kΩ	110-10k-1
R7	MF, 1/4W, 1%, 1kΩ	110-1k-1
R8	MF, 1/4W, 1%, 10kΩ	110-10k-1
R9	MF, 1/4W, 1%, 16.2kΩ	110-16.2k-1
R10	MF, 1/4W, 1%, 10kΩ	110-10k-1
R11	MF, 1/4W, 1%, 16.2kΩ	110-16.2k-1
R12	MF, 1/4W, 1%, 10kΩ	110-10k-1
R13	Variable, 1/2W, 10%, 2k	156-2k
R14	MF, 1/4W, 1%, 1kΩ	110-1k-1
R15	MF, 1/4W, 1%, 1kΩ	110-1k-1
R16	MF, 1/4W, 1%, 1kΩ	110-1k-1
R17	MF, 1/4W, 1%, 1MΩ	110-1M-1A
R18	MF, 1/4W, 1%, 1MΩ	110-1M-1A
R19	MF, 1/4W, 1%, 10kΩ	110-10k-1
R20	Variable, 1/2W, 10%, 2k	156-2k
R21	MF, 1/4W, 1%, 1kΩ	110-1k-1
R22	MF, 1/4W, 1%, 1kΩ	110-1k-1
R23	MF, 1/4W, 1%, 1kΩ	110-1k-1
R24	MF, 1/4W, 1%, 1MΩ	110-1M-1A
R25	MF, 1/4W, 1%, 1MΩ	110-1M-1A
R26	MF, 1/4W, 1%, 10kΩ	110-10k-1
R27	Variable, 1/2W, 10%, 2k	156-2k
R28	MF, 1/4W, 1%, 1kΩ	110-1k-1
R29	MF, 1/4W, 1%, 1kΩ	110-1k-1
R30	MF, 1/4W, 1%, 1kΩ	110-1k-1
R31	MF, 1/4W, 1%, 1MΩ	110-1M-1A
R32	MF, 1/4W, 1%, 1MΩ	110-1M-1A
R33	MF, 1/4W, 1%, 17.8kΩ	110-17.8k-1
R34	MF, 1/4W, 1%, 10kΩ	110-10k-1
R35	MF, 1/4W, 1%, 10kΩ	110-10k-1
R36	MF, 1/4W, 1%, 10kΩ	110-10k-1
R37	MF, 1/4W, 1%, 24.9kΩ	110-24.9k-1
R38	MF, 1/4W, 1%, 100kΩ	110-100k-1
R39	MF, 1/4W, 1%, 100kΩ	110-100k-1
R40	MF, 1/4W, 1%, 133kΩ	110-133k-1
R41	MF, 1/4W, 1%, 100kΩ	110-100k-1
R42	MF, 1/4W, 1%, 17.8kΩ	110-17.8k-1
R43	MF, 1/4W, 1%, 10kΩ	110-10k-1
R44	MF, 1/4W, 1%, 10kΩ	110-10k-1
R45	MF, 1/4W, 1%, 10kΩ	110-10k-1
R46	MF, 1/4W, 1%, 24.9kΩ	110-24.9k-1
R47	MF, 1/4W, 1%, 100kΩ	110-100k-1
R48	MF, 1/4W, 1%, 100kΩ	110-100k-1
R49	MF, 1/4W, 1%, 133kΩ	110-133k-1
R50	MF, 1/4W, 1%, 100kΩ	110-100k-1
R51	MF, 1/4W, 1%, 1kΩ	110-1k-1
R52	MF, 1/4W, 1%, 17.8kΩ	110-17.8k-1
R53	MF, 1/4W, 1%, 10kΩ	110-10k-1
R54	MF, 1/4W, 1%, 10kΩ	110-10k-1
R55	MF, 1/4W, 1%, 10kΩ	110-10k-1
R56	MF, 1/4W, 1%, 24.9kΩ	110-24.9k-1
R57	MF, 1/4W, 1%, 4.99kΩ	110-4.99k-1
R58	MF, 1/4W, 1%, 200kΩ	110-200k-1
R59	MF, 1/4W, 1%, 12.4kΩ	110-12.4k-1
R60	MF, 1/4W, 1%, 887Ω	110-887-1
R61	MF, 1/4W, 1%, 20kΩ	110-20k-1
R62	Variable, 1/2W, 10%, 200k	156-200k
R63	MF, 1/4W, 1%, 19.6kΩ	110-19.6k-1
R64	MF, 1/4W, 1%, 49.9k	110-49.9k-1
R65	MF, 1/4W, 1%, 10kΩ	110-10k-1
R66	MF, 1/4W, 1%, 1.47kΩ	110-1.47k-1
R67	MF, 1/4W, 1%, 10kΩ	110-10k-1
R68	MF, 1/4W, 1%, 1kΩ	110-1k-1
R69	MF, 1/4W, 1%, 20kΩ	110-20k-1
R70	MF, 1/4W, 1%, 301kΩ	110-301k
R71	MF, 1/4W, 1%, 10kΩ	110-10k-1
R72	MF, 1/4W, 1%, 100kΩ	110-100k-1
R73	MF, 1/4W, 1%, 10kΩ	110-10k-1
R74	MF, 1/4W, 1%, 100kΩ	110-100k-1
R75	MF, 1/4W, 1%, 1MΩ	110-1M-1A
R76	MF, 1/4W, 1%, 10kΩ	110-10k-1
R77	MF, 1/4W, 1%, 20kΩ	110-20k-1
R78	MF, 1/4W, 1%, 100kΩ	110-100k-1
R79	MF, 1/4W, 1%, 30.1kΩ	110-30.1k-1
R80	MF, 1/4W, 1%, 10kΩ	110-10k-1
R81	MF, 1/4W, 1%, 100kΩ	110-100k-1
R82	MF, 1/4W, 1%, 100kΩ	110-100k-1
R83	MF, 1/4W, 1%, 100kΩ	110-100k-1
R84	MF, 1/4W, 1%, 178kΩ	110-178k-1
R85	MF, 1/4W, 1%, 27.4kΩ	110-27.4k-1
R86	MF, 1/4W, 1%, 5.11Ω	110-5.11-1
R87	MF, 1/4W, 1%, 10kΩ	110-10k-1
R88	MF, 1/4W, 1%, 20kΩ	110-20k-1
R89	MF, 1/4W, 1%, 10kΩ	110-10k-1
R90	Variable, 1/2W, 10%, 200k	156-200k
R91	MF, 1/4W, 1%, 10kΩ	110-10k-1
R92	MF, 1/4W, 1%, 20kΩ	110-20k-1
R93	MF, 1/4W, 1%, 1kΩ	110-1k-1
R94	MF, 1/4W, 1%, 1kΩ	110-1k-1
R95	MF, 1/4W, 1%, 1kΩ	110-1k-1

INTEGRATED CIRCUITS

REF. DES.	DESCRIPTION	WILTRON PART NO.
U1	Octal Latch, 74LS374	54-41
U2	Quad NAND Gate, 74LS01	54-74LS01
U3	Op Amp, TL072CP	54-53
U4	Not Used	
U5	8 Bit DAC, AD7524	54-129
U6	8 Bit DAC, AD7524	54-129
U7	8 Bit DAC, AD7524	54-129
U8	Quad Op Amp, RC4136	54-RC4136
U9	Quad Op Amp, RC4136	54-RC4136
U10	Quad Op Amp, RC4136	54-RC4136
U11	Quad AND Gate, 74LS09	54-96
U12	Voltage Comparator, LM311	54-30
U13	Op Amp, TL072CP	54-53
U14	Op Amp, LM339	54-45
U15	Dual Flip-Flop, 74LS74	54-44
U16	Dual One-Shot, 96L02	54-96L02
U17	2-input NAND, 74LS10	54-42
U18	8 Bit ADC, ADC0804LCN	54-161
U19	Octal Latch, 74LS374	54-41

MISCELLANEOUS

REF. DES.	DESCRIPTION	WILTRON PART NO.
TP1 thru TP19	Test Points	706-44
—	Ejector, PCB	553-96

Table 6-6. A4 Automatic Level Control PCB, Dwg. 660-D-8004-3
(See Figure 6-4 for next higher assembly)

CAPACITORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
C1	Ceramic Disc, .1µF	230-37
C2	Ceramic Disc, .1µF	230-37
C3	Tantalum, 25V, 10µF	250-42
C4	Tantalum, 25V, 10µF	250-42
C5	Tantalum, 6V, 68µF	250-58
C6	Ceramic Disc, .1µF	230-37
C7	Ceramic Disc, .1µF	230-37
C8	Ceramic Disc, .1µF	230-37
C9	Ceramic Disc, .1µF	230-37
C10	Mica, 27pF	220-27
C11	Ceramic Disc, .1µF	230-37
C12	Ceramic Disc, .1µF	230-37
C13	Ceramic Disc, .1µF	230-37
C14	Ceramic Disc, .1µF	230-37
C15	Polycarbonate, .0047µF	210-50
C16	Polycarbonate, .0047µF	210-50
C17	Ceramic Disc, .1µF	230-37
C18	Ceramic Disc, .01µF	230-11
C19	Ceramic Disc, .0047µF	230-36
C20	Ceramic Disc, .02µF	230-27
C21	Ceramic Disc, .1µF	230-37
C22	Ceramic Disc, .1µF	230-37
C23	Aluminum, 63V, 47µF	250-51
C24	Not Used	
C25	Ceramic Disc, .01µF	230-11

DIODES

REF. DES.	DESCRIPTION	WILTRON PART NO.
CR1	Silicon, 1N4446	10-1N4446
CR2	Silicon, 1N4446	10-1N4446
CR3	Silicon, 1N4446	10-1N4446
CR4	Silicon, 1N4446	10-1N4446
CR5	Silicon, 1N4446	10-1N4446
CR6	Silicon, 1N4446	10-1N4446
CR7	Reference, 6.2V, 1N823	10-1N823
CR8	Zener, 5.1V, 0.4W, 1N751A	10-1N751A
CR9	Silicon, 1N4446	10-1N4446
CR10	Silicon, 1N4446	10-1N4446
CR11	Silicon, 1N4446	10-1N4446
CR12	Silicon, 1N4446	10-1N4446
CR13	Silicon, 1N4446	10-1N4446
CR14	Silicon, 1N4446	10-1N4446
CR15	MBD-501	10-4
CR16	Silicon, 1N4446	10-1N4446
CR17	Silicon, 1N4446	10-1N4446

TRANSISTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
Q1	NPN, .5W, 2N2222A	20-2N2222A
Q2	PNP, .4W, 2N4249	20-2N4249
Q3	PNP, .4W, 2N4249	

RESISTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
R1	MF, 1/4W, 1%, 10kΩ	110-10k-1
R2	MF, 1/4W, 1%, 8.25kΩ	110-8.25k-1
R3	Variable, Single Turn, 10kΩ	156-10k
R4	MF, 1/4W, 1%, 3.01kΩ	110-3.01k-1
R5	Variable, Multi-turn, 20kΩ	157-20k
R6	MF, 1/4W, 1%, 3.01kΩ	110-3.01k-1
R7	MF, 1/4W, 1%, 13.3kΩ	110-13.3k-1
R8	MF, 1/4W, 1%, 54.9kΩ	110-54.9k-1
R9	Variable, Single Turn, 20kΩ	156-20k
R10	MF, 1/4W, 1%, 5.49kΩ	110-5.49k-1
R11	Variable, Multi-turn, 20kΩ	157-20k
R12	MF, 1/4W, 1%, 8.25kΩ	110-8.25k-1
R13	MF, 1/4W, 1%, 64.9kΩ	110-64.9k-1
R14	MF, 1/4W, 1%, 316kΩ	110-316k-1
R15	MF, 1/4W, 1%, 20kΩ	110-20k-1
R16	MF, 1/4W, 1%, 64.9kΩ	110-64.9k-1
R17	MF, 1/4W, 1%, 5.49kΩ	110-5.49k-1
R18	MF, 1/4W, 1%, 5.49kΩ	110-5.49k-1
R19	Variable, Multi-turn, 20kΩ	157-20k
R20	MF, 1/4W, 1%, 64.9kΩ	110-64.9k-1
R21	MF, 1/4W, 1%, 10kΩ	110-10k-1
R22	MF, 1/4W, 1%, 20kΩ	110-20k-1
R23	MF, 1/4W, 1%, 10kΩ	110-10k-1
R24	MF, 1/4W, 1%, 10kΩ	110-10k-1
R25	MF, 1/4W, 1%, 1.07kΩ	110-1.07k-1
R26	MF, 1/4W, 1%, 19.6kΩ	110-19.6k-1
R27	MF, 1/4W, 1%, 12.1kΩ	110-12.1k-1
R28	MF, 1/4W, 1%, 10.2kΩ	110-10.2k-1
R29	MF, 1/4W, 1%, 16.5kΩ	110-16.5k-1
R30	MF, 1/4W, 1%, 10kΩ	110-10k-1
R31	MF, 1/4W, 1%, 51.1Ω	110-51.1-1
R32	MF, 1/4W, 1%, 51.1Ω	110-51.1-1
R33	MF, 1/4W, 1%, 10kΩ	110-10k-1
R34	MF, 1/4W, 1%, 511Ω	110-511-1
R35	MF, 1/4W, 1%, 100kΩ	110-100k-1
R36	MF, 1/4W, 1%, 10kΩ	110-10k-1
R37	MF, 1/4W, 1%, 511Ω	110-511-1
R38	MF, 1/4W, 1%, 100kΩ	110-100k-1
R39	MF, 1/4W, 1%, 10kΩ	110-10k-1
R40	MF, 1/4W, 0.1%, 900Ω	113-900-0.1
R41	MF, 1/4W, 0.1%, 900Ω	113-900-0.1
R42	MF, 1/4W, 1%, 12.4kΩ	110-12.4k-1
R43	MF, 1/4W, 1%, 261Ω	110-261-1
R44	MF, 1/4W, 1%, 261Ω	110-261-1
R45	MF, 1/4W, 1%, 12.4kΩ	110-12.4k-1
R46	MF, 1/4W, 1%, 604Ω	110-604-1
R47	MF, 1/4W, 1%, 576Ω	110-576-1
R48	MF, 1/4W, 1%, 12.4kΩ	110-12.4k-1
R49	MF, 1/4W, 1%, 1.82kΩ	110-1.82k-1
R50	MF, 1/4W, 1%, 953Ω	110-953-1
R51	MF, 1/4W, 1%, 4.99kΩ	110-4.99k-1
R52	MF, 1/4W, 1%, 54.9kΩ	110-54.9k-1

R53	MF, 1/4W, 1%, 15kΩ	110-15k-1
R54	MF, 1/4W, 1%, 12.4kΩ	110-12.4k-1
R55	MF, 1/4W, 1%, 487Ω	110-487-1
R56	MF, 1/4W, 1%, 464Ω	110-464-1
R57	MF, 1/4W, 1%, 12.4kΩ	110-12.4k-1
R58	MF, 1/4W, 1%, 2.43kΩ	110-2.43k-1
R59	MF, 1/4W, 1%, 2.05kΩ	110-2.05k-1
R60	MF, 1/4W, 1%, 12.4kΩ	110-12.4k-1
R61	MF, 1/4W, 1%, 12.4kΩ	110-12.4k-1
R62	MF, 1/4W, 0.1%, 20kΩ	113-20k-0.1
R63	MF, 1/4W, 0.1%, 20kΩ	113-20k-0.1
R64	MF, 1/4W, 0.1%, 20kΩ	113-20k-0.1
R65	MF, 1/4W, 0.1%, 20kΩ	113-20k-0.1
R66	Variable, Multi-turn, 2kΩ	157-2k
R67	MF, 1/4W, 1%, 2.37kΩ	110-2.37k-1
R68	Variable, Multi-turn, 2kΩ	157-2k
R69	MF, 1/4W, 1%, 1.47kΩ	110-1.47k-1
R70	Variable, Multi-turn, 2kΩ	157-2k
R71	MF, 1/4W, 1%, 6.19kΩ	110-6.19k-1
R72	Variable, Multi-turn, 2kΩ	157-2k
R73	MF, 1/4W, 1%, 7.87kΩ	110-7.87k-1
R74	MF, 1/4W, 1%, 10kΩ	110-10k-1
R75	MF, 1/4W, 1%, 10kΩ	110-10k-1
R76	CC, 1/4W, 5%, 10MΩ	101-10M-5
R77	MF, 1/4W, 1%, 133kΩ	110-133k-1
R78	MF, 1/4W, 1%, 2.49kΩ	110-2.49k-1
R79	MF, 1/4W, 1%, 8.66kΩ	110-8.66k-1
R80	Variable, Single Turn, 2kΩ	156-2k
R81	MF, 1/4W, 1%, 6.49kΩ	110-6.49k-1
R82	Variable, Single Turn, 2kΩ	156-2k
R83	MF, 1/4W, 1%, 11.3kΩ	110-11.3k-1
R84	Variable, Single Turn, 2kΩ	156-2k
R85	MF, 1/4W, 1%, 8.25kΩ	110-8.25k-1
R86	Variable, Single Turn, 2kΩ	156-2k
R87	MF, 1/4W, 1%, 8.66kΩ	110-8.66k-1
R88	Variable, Single Turn, 2kΩ	156-2k
R89	MF, 1/4W, 1%, 11kΩ	110-11k-1
R90	Variable, Single Turn, 5kΩ	156-5k
R91	MF, 1/4W, 1%, 1MΩ	110-1M-1A
R92	MF, 1/4W, 1%, 1MΩ	110-1M-1A
R93	MF, 1/4W, 1%, 10kΩ	110-10k-1
R94	MF, 1/4W, 1%, 1MΩ	110-1M-1A
R95	MF, 1/4W, 1%, 1MΩ	110-1M-1A
R96	MF, 1/4W, 1%, 1MΩ	110-1M-1A
R97	MF, 1/4W, 1%, 10kΩ	110-10k-1
R98	MF, 1/4W, 1%, 1MΩ	110-1M-1A
R99	MF, 1/4W, 1%, 26.7kΩ	110-26.7k-1
R100	MF, 1/4W, 1%, 42.2kΩ	110-42.2k-1
R101	MF, 1/4W, 1%, 30.1kΩ	110-30.1k-1
R102	MF, 1/4W, 1%, 30.1kΩ	110-30.1k-1
R103	Variable, Multi-turn, 5kΩ	157-5k
R104	MF, 1/4W, 1%, 301kΩ	110-301k-1
R105	MF, 1/4W, 1%, 10kΩ	110-10k-1
R106	MF, 1/4W, 1%, 9.76kΩ	110-9.76k-1
R107	MF, 1/4W, 1%, 10kΩ	110-10k-1
R108	MF, 1/4W, 1%, 511kΩ	110-511k-1
R109	MF, 1/4W, 1%, 10kΩ	110-10k-1
R110	MF, 1/4W, 1%, 10kΩ	110-10k-1
R111	MF, 1/4W, 1%, 10kΩ	110-10k-1
R112	MF, 1/4W, 1%, 10kΩ	110-10k-1
R113	MF, 1/4W, 1%, 20kΩ	110-20k-1
R114	MF, 1/4W, 1%, 20kΩ	110-20k-1
R115	Variable, Single Turn, 20kΩ	156-20k
R116	MF, 1/4W, 1%, 16.5kΩ	110-16.5k-1
R117	MF, 1/4W, 1%, 7.5kΩ	110-7.5k-1
R118	MF, 1/4W, 1%, 5.11kΩ	110-5.11k-1
R119	MF, 1/4W, 1%, 2kΩ	110-2k-1
R120	MF, 1/4W, 1%, 15kΩ	110-15k-1
R121	MF, 1/4W, 1%, 2kΩ	110-2k-1
R122	MF, 1/4W, 1%, 511Ω	110-511-1
R123	Variable, Single Turn, 2kΩ	156-2k
R124	Variable, Single Turn, 2kΩ	156-2k
R125	MF, 1/4W, 1%, 1kΩ	110-1k-1
R126	MF, 1/4W, 1%, 1kΩ	110-1k-1
R127	MF, 1/4W, 1%, 100kΩ	110-100k-1
R128	MF, 1/4W, 1%, 10kΩ	110-10k-1
R129	MF, 1/4W, 1%, 10kΩ	110-10k-1
R130	MF, 1/4W, 1%, 4.02kΩ	110-4.02k-1
R131	MF, 1/4W, 1%, 1kΩ	110-1k-1
R132	MF, 1/4W, 1%, 4.02kΩ	110-4.02k-1
R133	MF, 1/4W, 1%, 4.02kΩ	110-4.02k-1
R134	MF, 1/4W, 1%, 20kΩ	110-20k-1
R135	MF, 1/4W, 1%, 4.02kΩ	110-4.02k-1
R136	MF, 1/4W, 1%, 1kΩ	110-1k-1
R137	MF, 1/4W, 1%, 1kΩ	110-1k-1
R138	MF, 1/4W, 1%, 4.99kΩ	110-4.99k-1
R139	MF, 1/4W, 1%, 649Ω	110-649-1
R140	MF, 1/4W, 1%, 4.99kΩ	110-4.99k-1
R141	MF, 1/4W, 1%, 887Ω	110-887-1
R142	Variable, Single Turn, 20kΩ	156-20k
R143	MF, 1/4W, 1%, 4.99kΩ	110-20k-1
R144	MF, 1/4W, 1%, 15kΩ	110-15k-1
RP1	Package, 1kΩ	123-1

INTEGRATED CIRCUITS

REF. DES.	DESCRIPTION	WILTRON PART NO.
U1	Quad NAND, 74LS00	54-74LS00
U2	Hex Inverter, 74LS04	54-74LS04
U3	Triple NAND, 74LS10	54-42
U4	Op Amp, LF356N	50-9
U5	Switch, DG201	54-24
U6	Op Amp, LF356N	50-9
U7	Op Amp, LF356N	50-9
U8	Op Amp, TL072	54-53
U9	Op Amp, TL072	54-53
U10	Op Amp, TL072	54-53
U11	Quad Comparator, MC3302P	54-MC3302P
U12	Transistor Array, CA3054	54-6
U13	Transistor Array, CA3054	54-6
U14	Op Amp, LF356N	50-9
U15	Transistor Array, CA3054	54-6
U16	Op Amp, TL072	54-53
U17	Switch, DG201	54-24
U18	Op Amp, TL074	54-132
U19	Op Amp, TL074	54-132
U20	Switch, DG201	54-24
U21	Op Amp, LF356N	50-9
U22	8 Bit DAC, AD 7524	54-129
U23	Quad Schmitt NAND, 74LS132	54-74LS132
U24	Octal Latch, 74LS374	54-41

MISCELLANEOUS

REF. DES.	DESCRIPTION	WILTRON PART NO.
TP1 thru TP7	Pin, Test Point	706-44
——	Ejector, PC Board	553-96

Table 6-7. A5 Frequency Instruction PCB, Dwg. 660-D-8005-3
(See Figure 6-4 for next higher assembly)

CAPACITORS

REF DES.	DESCRIPTION	WILTRON PART NO.
C1	Mica, 100pF	220-100
C2	Mica, 100pF	220-100
C3	Disc Ceramic, 0.001μF	230-30
C4	Monolithic, 0.1μF	230-37
C5	Tantalum, 4.7μF, 35V	250-39
C6	Monolithic, 0.1μF	230-37
C7	Tantalum, 4.7μF, 35V	250-39
C8	Monolithic, 0.1μF	230-37
C9	Monolithic, 0.1μF	230-37
C10	Monolithic, 0.1μF	230-37
C11	Monolithic, 0.1μF	230-37
C12	Tantalum, 4.7μF, 35V	250-39
C13	Tantalum, 4.7μF, 35V	250-39
C14	Monolithic, 0.1μF	230-37
C15	Monolithic, 0.1μF	230-37
C16	Tantalum, 4.7μF, 35V	250-39
C17	Tantalum, 4.7μF, 35V	250-39
C18	Monolithic, 0.1μF	230-37
C19	Monolithic, 0.1μF	230-37
C20	Tantalum, 4.7μF, 35V	250-39
C21	Tantalum, 4.7μF, 35V	250-39
C22	Monolithic, 0.1μF	230-37
C23	Monolithic, 0.1μF	230-37
C24	Monolithic, 0.1μF	230-37
C25	Disc Ceramic, 0.001μF	230-30
C26	Mica, 100pF	220-100
C27	Disc Ceramic, 0.001μF	230-30

DIODES

REF DES.	DESCRIPTION	WILTRON PART NO.
CR1	Schottky, MBD-501	10-4
CR2	Schottky, MBD-501	10-4
CR3	Silicon, 1N4446	10-1N4446
CR4	Silicon, 1N4446	10-1N4446
CR5	Zener, 12V, 0.4W, 1N759A	10-1N759A
CR6	Reference, 6.2V, 1N823	10-1N823
CR7	Silicon, 1N4446	10-1N4446
CR8	Silicon, 1N4446	10-1N4446
CR9	Zener, 11V, 1N962B	10-1N962B
CR10	Zener, 11V, 1N962B	10-1N962B

TRANSISTORS

REF DES.	DESCRIPTION	WILTRON PART NO.
Q1	PNP, 2N6041	20-2N6041
Q2	PNP, 2N2907A	20-2N2907A
Q3	NPN, 2N2222A	20-2N2222A

RESISTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
R1	MF, 1/4W, 1%, 10kΩ	110-10k-1
R2	MF, 1/4W, 1%, 2.37kΩ	110-2.37k-1
R3	MF, 1/4W, 1%, 2.37kΩ	110-2.37k-1
R4	MF, 1/4W, 1%, 3.92kΩ	110-3.92k-1
R5	MF, 1/4W, 1%, 392Ω	110-392-1
R6	MF, 1/4W, 1%, 11.8kΩ	110-11.8k-1
R7	MF, 1/4W, 1%, 11.8kΩ	110-11.8k-1
R8	Variable, Multi Turn	157-50k
R9	MF, 1/4W, 1%, 348kΩ	110-348k-1
R10	Variable, Multi Turn 20k	157-20k
R11	MF, 1/4W, 0.1%, 30kΩ	113-30k-0.1
R12	MF, 1/4W, 1%, 511Ω	110-511-1
R13	Variable, Single Turn	156-500
R14	MF, 1/4W, 1%, 10kΩ	110-10k-1
R15	MF, 1/4W, 0.1%, 30kΩ	113-30k-0.1
R16	MF, 1/4W, 1%, 10kΩ	110-10k-1
R17	MF, 1/4W, 1%, 10kΩ	110-10k-1
R18	Part of RP2	
R19	Part of RP2	
R20	Part of RP2	
R21	Part of RP2	
R22	Part of RP2	
R23	MF, 1/4W, 0.1%, 30kΩ	113-30k-0.1
R24	MF, 1/4W, 1%, 511Ω	110-511-1
R25	MF, 1/4W, 1%, 1kΩ	110-1k-1
R26	MF, 1/4W, 0.1%, 10kΩ	113-10k-0.1
R27	MF, 1/4W, 0.1%, 10kΩ	113-10k-0.1
R28	MF, 1/4W, 0.1%, 10kΩ	113-10k-0.1
R29	Variable, Multi Turn 500Ω	157-500
R30	MF, 1/4W, 0.1%, 30kΩ	113-30k-0.1
R31	MF, 1/4W, 0.1%, 10kΩ	113-10k-0.1
R32	MF, 1/4W, 0.1%, 10kΩ	113-10k-0.1
R33	MF, 1/4W, 0.1%, 10kΩ	113-10k-0.1
R34	MF, 1/4W, 0.1%, 10kΩ	113-10k-0.1
R35	MF, 1/4W, 1%, 27.4kΩ	110-27.4k-1
R36	MF, 1/4W, 0.1%, 10kΩ	113-10k-0.1
R37	Part of RP2	
R38	Part of RP2	
R39	MF, 1/4W, 1%, 511Ω	110-511-1
R40	Variable, Multi Turn 20k	157-20k
R41	MF, 1/4W, 0.1%, 10kΩ	113-10k-0.1
R42	MF, 1/4W, 1%, 10kΩ	110-10k-1
R43	MF, 1/4W, 0.1%, 10kΩ	113-10k-0.1
R44	MF, 1/4W, 0.1%, 10kΩ	113-10k-0.1
R45	MF, 1/4W, 0.1%, 10kΩ	113-10k-0.1
R46	Variable, Multi Turn 20k	157-20k
R47	MF, 1/4W, 1%, 10Ω	110-10-1
R48	MF, 1/4W, 1%, 1kΩ	110-1k-1
R49	Variable, Multi Turn 500Ω	157-500
R50	MF, 1/4W, 1%, 9.76kΩ	110-9.76k-1
R51	MF, 1/4W, 1%, 6.19kΩ	110-6.19k-1
R52	MF, 1/4W, 1%, 511Ω	110-511-1
R53	MF, 1/4W, 1%, 10kΩ	110-10k-1
R54	MF, 1/4W, 1%, 1kΩ	110-1k-1
R55	Variable, Multi Turn 500Ω	157-500
R56	MF, 1/4W, 1%, 10kΩ	110-10k-1
R57	MF, 1/4W, 1%, 5.76kΩ	110-5.76k-1
R58	MF, 1/4W, 1%, 10Ω	110-10-1
R59	MF, 1/4W, 0.1%, 10kΩ	113-10k-0.1
R60	MF, 1/4W, 1%, 3.92kΩ	110-3.92k-1
R61	MF, 1/4W, 1%, 10kΩ	110-10k-1
R62	Variable, Single Turn 5k	156-5k
RP1	Resistor Pack, 7 Resistor Network 10kΩ	123-6
RP2	Resistor Pack	
	a. 6637/6647	660-A-8145-3
	b. 6638/6648	660-A-8145-4

INTEGRATED CIRCUITS

REF. DES.	DESCRIPTION	WILTRON PART NO.
U1	Hex Inverter, 74LS00	54-74LS00
U2	8 Bit Multiplying DAC, MC1408L8	54-148
U3	Op Amp, 356	50-9
U4	8 Bit Multiplying DAC, MC1408L8	54-148
U5	Octal Latch, 74LS374	54-41
U6	Op Amp, 356	50-9
U7	16 Bit DAC	54-150
U8	Octal Latch, 74LS374	54-41
U9	Octal Latch, 74LS374	54-41
U10	Dual FET-Input Op Amp, TL072	54-53
U11	Dual Analog Switch, DG200BA	50-DG200BA
U12	Op Amp, 301A	50-8
U13	Op Amp, 356	50-9
U14	Op Amp, 356	50-9
U15	Octal Latch, 74LS374	54-41
U16	Octal Latch, 74LS374	54-41
U17	Octal Latch, 74LS374	54-41
U18	Octal Latch, 74LS374	54-41
U19	12 Bit Multiplying DAC	54-149
U20	Op Amp, 356	50-9
U21	Dual FET-Input Op Amp, TL072	54-53
U22	Quad Analog Switch, LF13201N	54-20
U23	Op Amp, 356	50-9
U24	12 Bit Multiplying DAC	54-149
U25	Op Amp, 356	50-9
U26	Op Amp, 356	50-9
U27	Dual FET-Input Op Amp, TL072	54-53
U28	Quad Analog Switch, LF13201N	54-20

MISCELLANEOUS

REF. DES.	DESCRIPTION	WILTRON PART NO.
S1	Switch, DPDT	420-14
TP1 thru TP10	Pin, Test Point	706-44
——	Socket, I.C., 14 Pin	553-63
——	Socket, I.C. 24 Pin	553-67
——	Ejector, P.C. Board	553-96

Table 6-8. A10 FM/Attenuator PCB, Dwg. 660-D-8010-3
(See Figure 6-4 for next higher assembly)

CAPACITORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
C1	Mica, 130pF	220-130
C2	Monolithic, .1µF	230-37
C3	Monolithic, .1µF	230-37
C4	Ceramic Disc, .001µF	230-30
C5	Ceramic Disc, .001µF	230-30
C6	Ceramic Disc, .001µF	230-30
C7	Ceramic Disc, .001µF	230-30
C8	Mica, 8pF	220-8
C9	Tantalum, 25V, 10µF	250-42
C10	Tantalum, 25V, 10µF	250-42
C11	Ceramic Disc, .001µF	230-30
C12	Mica, 8pF	220-8
C13	Monolithic, .1µF	230-37
C14	Monolithic, .1µF	230-37
C15	Mica, 8pF	220-8
C16	Mica, 8pF	220-8
C17	Tantalum, 25V, 10µF	250-42
C18	Tantalum, 25V, 10µF	250-42
C19	Tantalum, 25V, 10µF	250-42
C20	Tantalum, 25V, 10µF	250-42
C21	Monolithic, .1µF	230-37
C22	Monolithic, .1µF	230-37
C23	Tantalum, 6V, 68µF	250-58
C24	Ceramic Disc .01µF	230-11
C25	Ceramic Disc .01µF	230-11
C26	Mica, 8pF	220-8
C27	Tantalum, 25V, 10µF	250-42
C28	Tantalum, 25V, 10µF	250-42
C29	Ceramic, .0047µF	230-36
C30	Mica, 8pF	220-8

DIODES

REF. DES.	DESCRIPTION	WILTRON PART NO.
CR1	Silicon, 1N4446	10-1N4446
CR2	Silicon, 1N4446	10-1N4446
CR3	Zener, 3.3V, 0.4W, 1N746A	10-1N746A
CR4	Zener, 3.3V, 0.4W, 1N746A	10-1N746A
CR5	Silicon, 1N4446	10-1N4446
CR6	Silicon, 1N4446	10-1N4446
CR7	Zener, 3.3V, 0.4W, 1N746A	10-1N746A
CR8	Zener, 3.3V, 0.4W, 1N746A	10-1N746A
CR9	Silicon, 1N4446	10-1N4446
CR10	Silicon, 1N4446	10-1N4446
CR11	Silicon, 1N4446	10-1N4446
CR12	Silicon, 1N4446	10-1N4446
CR13	Silicon, 1N4446	10-1N4446
CR14	Zener, 4.7V, 0.4W, 1N750A	10-11
CR15	Zener, 4.7V, 0.4W, 1N750A	10-11
CR16	Silicon, 1N4446	10-1N4446
CR17	Silicon, 1N4446	10-1N4446
CR18	Silicon, 1N4446	10-1N4446
CR19	Silicon, 1N4446	10-1N4446
CR20	Silicon, 1N4446	10-1N4446
CR21	Silicon, 1N4446	10-1N4446
CR22	Silicon, 1N4446	10-1N4446
CR23	Silicon, 1N4446	10-1N4446
CR24	Silicon, 1N4446	10-1N4446
CR25	Silicon, 1N4446	10-1N4446
CR26	Silicon, 1N4446	10-1N4446
CR27	Silicon, 1N4446	10-1N4446
CR28	Silicon, 1N4446	10-1N4446
CR29	Silicon, 1N4446	10-1N4446
CR30	Silicon, 1N4446	10-1N4446
CR31	Silicon, 1N4446	10-1N4446
CR32	Silicon, 1N4446	10-1N4446

TRANSISTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
Q1	PNP, 10W, 2N6552	20-3
Q2	NPN, 10W, 2N6555	20-4
Q3	PNP, 10W, 2N6552	20-3
Q4	NPN, 10W, 2N6555	20-4

Q5	NPN, 50W, TIP110	20-22
Q6	PNP, 50W, TIP115	20-23

RESISTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
R1	MF, 1/4W, 1%, 14.3kΩ	110-14.3k-1
R2	MF, 1/4W, 1%, 14.3kΩ	110-14.3k-1
R3	MF, 1/4W, 1%, 100kΩ	110-100k-1
R4	MF, 1/4W, 1%, 10kΩ	110-10k-1
R5	MF, 1/4W, 1%, 10kΩ	110-10k-1
R6	MF, 1/4W, 1%, 100Ω	110-100-1
R7	MF, 1/4W, 1%, 100Ω	110-100-1
R8	MF, 1/4W, 1%, 100Ω	110-100-1
R9	MF, 1/4W, 1%, 100Ω	110-100-1
R10	Variable, 5k, 1-turn	156-5k
R11	Variable, 5k, 1-turn	156-5k
R12	Variable, 5k, 1-turn	156-5k
R13	Variable, 5k, 1-turn	156-5k
R14	MF, 1/4W, 1%, 7.32kΩ	110-7.32k-1
R15	MF, 1/4W, 1%, 4.99kΩ	110-4.99k-1
R16	MF, 1/4W, 1%, 4.99kΩ	110-4.99k-1
R17	MF, 1/4W, 1%, 100Ω	110-100-1
R18	MF, 1/4W, 1%, 4.99kΩ	110-4.99k-1
R19	MF, 1/4W, 1%, 4.99kΩ	110-4.99k-1
R20	MF, 1/4W, 1%, 16.5kΩ	110-16.5k-1
R21	Not Used	
R22	MF, 1/4W, 1%, 10kΩ	110-10k-1
R23	MF, 1/4W, 1%, 10kΩ	110-10k-1
R24	MF, 1/4W, 1%, 100kΩ	110-100k-1
R25	MF, 1/4W, 1%, 10kΩ	110-10k-1
R26	MF, 1/4W, 1%, 10kΩ	110-10k-1
R27	MF, 1/4W, 1%, 8.87kΩ	110-8.87k-1
R28	MF, 1/4W, 1%, 49.9kΩ	110-49.9-1
R29	MF, 1/4W, 1%, 2.8kΩ	110-2.8k-1
R30	MF, 1/4W, 1%, 14.7Ω	110-14.7-1
R31	MF, 1/4W, 1%, 14.7Ω	110-14.7-1
R32	MF, 1/4W, 1%, 14.7Ω	110-14.7-1
R33	MF, 1/4W, 1%, 14.7Ω	110-14.7-1
R34	MF, 1/4W, 1%, 14.7Ω	110-14.7-1
R35	MF, 1/4W, 1%, 14.7Ω	110-14.7-1
R36	MF, 1/4W, 1%, 2.8kΩ	110-2.8k-1
R37	MF, 1/4W, 1%, 42.2Ω	110-42.2-1
R38	MF, 1/4W, 1%, 42.2Ω	110-42.2-1
R39	MF, 1/4W, 1%, 42.2Ω	110-42.2-1
R40	MF, 1/4W, 1%, 42.2Ω	110-42.2-1
R41	MF, 1/4W, 1%, 10kΩ	110-10k-1
R42	MF, 1/4W, 1%, 9.76kΩ	110-9.76k-1
R43	MF, 1/4W, 1%, 3.65kΩ	110-3.65k-1
R44	MF, 1/4W, 1%, 80.6Ω	110-80.6-1
R45	MF, 1/4W, 1%, 80.6Ω	110-80.6-1
R46	MF, 1/4W, 1%, 34.8Ω	110-34.8-1
R47	MF, 1/4W, 1%, 34.8Ω	110-34.8-1
R48	MF, 1/4W, 1%, 34.8Ω	110-34.8-1
R49	MF, 1/4W, 1%, 34.8Ω	110-34.8-1
R50	MF, 1/4W, 1%, 3.65kΩ	110-3.65k-1
R51	MF, 1/4W, 1%, 121Ω	110-121-1
R52	MF, 1/4W, 1%, 121Ω	110-121-1
R53	MF, 1/4W, 1%, 121Ω	110-121-1
R54	MF, 1/4W, 1%, 121Ω	110-121-1
R55	MF, 1/4W, 1%, 10kΩ	110-10k-1
R56	MF, 1/4W, 1%, 10kΩ	110-10k-1
R57	MF, 1/4W, 1%, 10kΩ	110-10k-1
R58	MF, 1/4W, 1%, 10kΩ	110-10k-1
R59	MF, 1/4W, 1%, 10kΩ	110-10k-1
R60	MF, 1/4W, 1%, 10kΩ	110-10k-1
R61	Variable, 10k, 1-turn	156-10k
R62	Variable, 10k, 1-turn	156-10k
R63	MF, 1/4W, 1%, 46.4kΩ	110-46.4k-1
R64	MF, 1/4W, 1%, 8.25kΩ	110-8.25k-1
R65	MF, 1/4W, 1%, 100Ω	110-100-1
R66	MF, 1/4W, 1%, 3.65kΩ	110-3.65k-1
R67	MF, 1/4W, 1%, 3.65kΩ	110-3.65k-1
R68	WW, 3W, 5Ω	130-5-3
R69	WW, 3W, 5Ω	130-5-3
R70	WW, 3W, 5Ω	130-5-3
R71	MF, 1/4W, 1%, 10kΩ	110-10k-1
R72	MF, 1/4W, 1%, 10kΩ	110-10k-1
R73	MF, 1/4W, 1%, 9.76kΩ	110-9.76k-1
R74	MF, 1/4W, 1%, 10kΩ	110-10k-1
R75	MF, 1/4W, 1%, 8.82kΩ	110-8.82k-1

INTEGRATED CIRCUITS

REF. DES.	DESCRIPTION	WILTRON PART NO.
U1	Quad Exclusive OR 74LS86	54-125
U2	Comparator, LM311H	54-30
U3	Comparator, LM311H	54-30
U4	Op Amp, LF357	50-7
U5	Quad Switch DG201CJ	54-24
U6	Quad Switch DG201CJ	54-24
U7	Op Amp, LF357	50-7
U8	Op Amp, LF357	50-7
U9	Op Amp, LF357	50-7
U10	Op Amp, LF357	50-7
U11	Hex Inverter, 74LS04	54-74LS04
U12	Dual AND Driver, 75451	54-144
U13	Dual AND Driver, 75451	54-144
U14	Dual AND Driver, 75451	54-144
U15	Dual AND Driver, 75451	54-144

MISCELLANEOUS

REF. DES.	DESCRIPTION	WILTRON PART NO.
TP1 thru TP6	Pin, Test Point	706-44
—	Heatsink, Transistor #6030	553-53
—	Ejector, P.C. Board	553-96

Table 6-9. A13 Switching Power Supply PCB, Dwg. 660-D-8013-3
(See Figure 6-4 for next higher assembly)

CAPACITORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
C1	Monolithic, .1µF, 50V	230-37
C2	Tantalum, 1µF, 35V	250-19
C3	Tantalum, 10µF, 25V	250-42
C4	Monolithic, .1µF, 50V	230-37
C5	Mylar, 1000pF, 500V, 5%	227-13
C6	Tantalum, 10µF, 25V	250-42
C7	Tantalum, 2.2µF, 20V	250-40
C8	Tantalum, 4.7µF, 35V	250-39
C9	Mylar, .01µF, 200V	210-20
C10	Monolithic, .1µF, 50V	230-37
C11	Mylar, 1000pF, 500V, 5%	227-13
C12	Monolithic, .1µF, 50V	230-37
C13	Tantalum, 10µF, 25V	250-42

C14	Tantalum, 12µF, 350V	250-85
C15	Tantalum, 12µF, 350V	250-85
C16	Mica, 470pF	220-470
C17	Disc., .0027µF, 100V	230-34
C18	Disc., .0027µF, 100V	230-34
C19	Tantalum, 6.8µF, 35V	250-41A
C20	Electrolytic, 150µF, 25V	250-52
C21	Electrolytic, 150µF, 25V	250-52
C22	Tantalum, 6.8µF, 35V	250-41A
C23	Tantalum, 6.8µF, 35V	250-41A
C24	Disc., .0027µF, 100V	230-34
C25	Disc., .0027µF, 100V	230-34
C26	Tantalum, 6.8µF, 35V	250-41A
C27	Electrolytic, 150µF, 25V	250-52
C28	Electrolytic, 150µF, 25V	250-52
C29	Tantalum, 6.8µF, 35V	250-41A
C30	Tantalum, 6.8µF, 35V	250-41A
C31	Tantalum, 6.8µF, 35V	250-41A
C32	Tantalum, 6.8µF, 35V	250-41A
C33	Electrolytic, 47µF, 63V	250-51
C34	Disc., .0027µF, 100V	230-34
C35	Tantalum, 6.8µF, 35V	250-41A
C36	Disc., .002µF, 500V	230-33
C37	Disc., .002µF, 500V	230-33
C38	Tantalum, 6.8µF, 35V	250-41A
C39	Mylar, .1µF, 250V	210-30
C40	Electrolytic, 47µF, 63V	250-51
C41	Tantalum, 6.8µF, 35V	250-41A
C42	Disc., .002µF, 500V	230-33
C43	Disc., .002µF, 500V	230-33
C44	Tantalum, 6.8µF, 35V	250-41A
C45	Mylar, .1µF, 250V	210-30
C46	Electrolytic, 47µF, 63V	250-51
C47	Tantalum, 6.8µF, 35V	250-41A
C48	Monolithic, .1µF, 50V	230-37
C49	Mica, 15pF	220-15
C50	Disc, Ceramic, .01µF, 1kV	230-26
C51	Disc, Ceramic, .01µF, 1kV	230-26
C52	Tantalum, .0047µF, 3kV	250-97
C53	Tantalum, .0047µF, 3kV	250-97

DIODES

REF. DES.	DESCRIPTION	WILTRON PART NO.
CR1	Silicon, 1N4446	10-1N4446
CR2	Silicon, 1N4446	10-1N4446
CR3	Silicon, 1N4446	10-1N4446
CR4	Silicon, 1N4446	10-1N4446
CR5	Silicon, 1N4446	10-1N4446
CR6	Silicon, 1N4446	10-1N4446
CR7	Silicon, 1N4446	10-1N4446
CR8	Silicon, 1N4446	10-1N4446
CR9	Zener, 15V, 1W, 5%, 1N4744A	10-1N4744A
CR10	Silicon, 1N4446	10-1N4446
CR11	Fast Recovery, 400V, 1A, 1N4936	10-23
CR12	Fast Recovery, 400V, 1A, 1N4936	10-23
CR13	Schottky, 40V, 5A, 1N5825	10-22
CR14	Schottky, 40V, 5A, 1N5825	10-22
CR15	Zener, 25V, 5W, 5%, 1N5360A	10-24
CR16	Fast Recovery, 100V, 3A, MR851	10-27
CR17	Fast Recovery, 100V, 3A, MR851	10-27
CR18	Fast Recovery, 100V, 3A, MR851	10-27
CR19	Fast Recovery, 100V, 3A, MR851	10-27
CR20	Fast Recovery, 200V, 3A, MR852	10-26
CR21	Fast Recovery, 200V, 3A, MR852	10-26
CR22	Fast Recovery, 200V, 3A, MR852	10-26
CR23	Fast Recovery, 200V, 3A, MR852	10-26
CR24	Fast Recovery, 200V, 3A, MR852	10-26
CR25	Fast Recovery, 200V, 3A, MR852	10-26
CR26	Fast Recovery, 400V, 2A, MR854	10-25
CR27	Fast Recovery, 400V, 2A, MR854	10-25
CR28	Fast Recovery, 100V, 1A, 1N4934	10-31
CR29	Fast Recover, 100V, 1A, 1N4934	10-31

INDUCTOR ASSEMBLIES

REF. DES.	DESCRIPTION	WILTRON PART NO.
L1	SPEC-A-8076	310-66
L2	SPEC-A-8077	310-67
L3	SPEC-A-8074	310-64
L4	SPEC-A-8075	310-65
L5	SPEC-A-8076	310-66
L6	SPEC-A-8074	310-64

TRANSISTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
Q1	2N2907, PNP	20-2N2907
Q2	2N2222A, NPN	20-2N2222A
Q3	300V, .6W, PNP, MPSA92	20-MPSA92
Q4	300V, .6W, PNP, MPSA92	20-MPSA92
Q5	HEXFET, 1Ω, 350V, 3.5A, 1RF730	20-31
Q6	HEXFET, 1Ω, 350V, 3.5A, 1RF730	20-31

RESISTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
R1	MF, 1/4W, 1%, 147Ω	110-147-1
R2	MF, 1/4W, 1%, 3.16k	110-3.16k-1
R3	MF, 1/4W, 1%, 22.1k	110-22.1k-1
R4	MF, 1/4W, 1%, 2.26k	110-2.26k-1
R5	MF, 1/4W, 1%, 22.1k	110-22.1k-1
R6	Trimmer, 1k	156-1k
R7	MF, 1/4W, 1%, 6.49k	110-6.49k-1
R8	CC, 1/4W, 5%, 22M	101-22M-5
R9	MF, 1/4W, 1%, 42.2k	110-42.2k-1
R10	MF, 1/4W, 1%, 4.53k	110-4.53k-1
R11	MF, 1/4W, 1%, 147Ω	110-147-1
R12	MF, 1/4W, 1%, 750k	110-750k-1
R13	MF, 1/4W, 1%, 10k	110-10k-1
R14	MF, 1/4W, 1%, 10k	110-10k-1
R15	MF, 1/4W, 1%, 3.32k	110-3.32k-1
R16	MF, 1/4W, 1%, 3.32k	110-3.32k-1
R17	MF, 1/4W, 1%, 499Ω	110-499-1

R18	MF, 1/4W, 1%, 499Ω	110-499-1
R19	MF, 1/4W, 1%, 24.9k	110-24.9k-1
R20	MF, 1/4W, 1%, 1.47k	110-1.47k-1
R21	MF, 1/4W, 1%, 10k	110-10k-1
R22	MF, 1/4W, 1%, 100k	110-100k-1
R23	MF, 1/4W, 1%, 14.7k	110-14.7k-1
R24	MF, 1/4W, 1%, 13.3k	110-13.3k-1
R25	MF, 1/4W, 1%, 6.81k	110-6.81k-1
R26	MF, 1/4W, 1%, 8.45k	110-8.45k-1
R27	Trimmer, 5k	156-5k
R28	MF, 1/4W, 1%, 1k	110-1k-1
R29	MF, 1/4W, 1%, 1k	110-1k-1
R30	MF, 1/4W, 1%, 1k	110-1k-1
R31	MF, 1/4W, 1%, 1k	110-1k-1
R32	CC, 1/2W, 5%, 100k	102-100k-5
R33	CC, 1/2W, 5%, 100k	102-100k-5
R34	CC, 1/2W, 5%, 100k	102-100k-5
R35	CC, 2W, 5%, 750Ω	104-750-5
R36	MF, 1/4W, 1%, 10Ω	110-10-1
R37	MF, 1/4W, 1%, 10Ω	110-10-1
R38	MF, 1/4W, 1%, 30.1Ω	110-30.1-1
R39	MF, 1/4W, 1%, 30.1Ω	110-30.1-1
R40	CC, 1/2W, 5%, 51Ω	102-51-5
R41	MF, 1/4W, 1%, 100Ω	110-100-1
R42	MF, 1/4W, 1%, 100Ω	110-100-1
R43	CC, 1/2W, 5%, 150Ω	102-150-5
R44	CC, 1/2W, 5%, 150Ω	102-150-5
R45	MF, 1/4W, 1%, 100Ω	110-100-1
R46	MF, 1/4W, 1%, 1k	110-1k-1
R47	CC, 2W, 5%, 750Ω	104-750-5

TRANSFORMERS

REF. DES.	DESCRIPTION	WILTRON PART NO.
T1	Driver Transformer Assy SPEC-A-8078	320-56
T2	Driver Transformer Assy SPEC-A-8078	320-56
T3	Output Transformer Assy SPEC-A-8079	320-57
T4	Common-Mode-Isolation	320-70

INTEGRATED CIRCUITS

REF. DES.	DESCRIPTION	WILTRON PART NO.
U1	Voltage Regulator, 12V, µA7812	54-LM340T-12
U2	Op Amp, LF356H	50-2
U3	Timer, 555NE	54-555
U4	Pulse Width Modulator, MC3420P	54-140

MISCELLANEOUS

REF. DES.	DESCRIPTION	WILTRON PART NO.
TP1 thru TP10	Pins, Test Point	706-44
—	Ejector, P.C. Board	553-96

Table 6-10. A14 Motherboard PCB, Dwg. 660-D-8014
(See Figure 6-4 for next higher assembly)

CAPACITORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
C1	Disc Ceramic, 500V, 0.001µF	230-3
C2	Disc Ceramic, 500V, 0.001µF	230-3
C3	Disc Ceramic, 500V, 0.001µF	230-3
C4	Electrolytic, 35V, 470µF	250-87
C5	Disc Ceramic, 1kV, 0.01µF	230-40
C6	Disc Ceramic, 1kV, 0.01µF	230-40
C7	Disc Ceramic, 1kV, 0.01µF	230-40
C8	Disc Ceramic, 1kV, 0.01µF	230-40
C9	Disc Ceramic, 1kV, 0.01µF	230-40
C10	Disc Ceramic, 1kV, 0.01µF	230-40
C11	Disc Ceramic, 1kV, 0.01µF	230-40
C12	Electrolytic, 200V, 850µF	250-86
C13	Electrolytic, 200V, 850µF	250-86
C14	Disc Ceramic, .01µF	230-11
C15	Tantalum, 35V, 6.8µF	250-41A
C16	Tantalum, 35V, 6.8µF	250-41A
C17	Tantalum, 35V, 6.8µF	250-41A
C18	Electrolytic, 63V, 10µF	250-34
C19	Tantalum, 35V, 6.8µF	250-41A
C20	Tantalum, 35V, 6.8µF	250-41A
C21	Electrolytic, 63V, 47µF	250-51
C22	Electrolytic, 25V, 100µF	250-50
C23	Tantalum, 25V, 10µF	250-42
C24	Tantalum, 25V, 10µF	250-42
C25	Tantalum, 25V, 10µF	250-42
C26	Tantalum, 35V, 1µF	250-19
C27	Mylar, 250V, 0.1µF	210-30
C28	Mica, 560pF	223-560
C29	Mica, 560pF	223-560
C30	Mica, 560pF	223-560
C31	Mica, 560pF	223-560
C32	Disc Ceramic, .01µF	230-11
C33	Monolithic, 100V, 0.1µF	230-37
C34	Tantalum, 35V, 6.8µF	250-41A
C35	Monolithic, 100V, .1µF	230-37
C36	Electrolytic, 63V, 10µF	250-34
C37	Tantalum, 1µF, 35V	250-19

DIODES AND BRIDGE RECTIFIER

REF. DES.	DESCRIPTION	WILTRON PART NO.
CR1	Zener, 18V, 0.4W	10-1N967B
CR2	Zener, 5.6V, 0.4W	10-1N752A
CR3	Silicon	10-1N4446
CR4	Silicon	10-1N4446
CR5	Silicon Rectifier	10SI2
CR6	Silicon Rectifier	10-SI2
CR7	Silicon Rectifier	10-SI2
CR8	Silicon Rectifier	10-SI2
CR9	Silicon Rectifier	10-SI2
CR10	Silicon Rectifier	10-SI2
CR11	Silicon Rectifier	10-SI2
CR13	Silicon	10-1N4446
CR14	Zener, 4.7V, 0.4W	10-11
CR15	Silicon Rectifier	10-SI2
CR16	Silicon Rectifier	10-SI2
CR17	Silicon	10-1N4446
CR18	Silicon	10-1N4446
CR19	Silicon	10-1N4446
CR20	Silicon	10-1N4446
CR21	Silicon Rectifier	10-SI2
CR22	Silicon	10-1N4446
CR23	Silicon Rectifier	10-SI2
CR24	Silicon Rectifier	10-SI2

CR25	Silicon Rectifier	10-SI2
CR26	Silicon Rectifier	10-SI2
CR27	Silicon Rectifier	10-SI2
CR28	Silicon Rectifier	10-SI2
CR29	Silicon Rectifier	10-SI2
CR30	Silicon Rectifier	10-SI2
CR31	Silicon Rectifier	10-SI2
CR32	Silicon Rectifier	10-SI2
CR33	Silicon Rectifier	10-SI2
CR34	Silicon	10-1N4446
CR35	Silicon	10-1N4446
CR36	Silicon	10-1N4446

LED'S

REF. DES.	DESCRIPTION	WILTRON PART NO.
DS1	Light Emitting, Green	15-6
DS2	Light Emitting, Red	15-5
DS3	Light Emitting, Red	15-5
DS4	Light Emitting, Red	15-5
DS5	Light Emitting, Red	15-5

CONNECTORS

P1	10-Pin Straight	551-234
P2	4-Pin, Straight	551-88
P3	26-Pin, Straight	551-216
P4	26-Pin, Right Angle	551-217
P5	26-Pin, Right Angle	551-217
P6	26-Pin, Right Angle	551-217
P7	26-Pin, Right Angle	551-217
P8	3-Pin, Right Angle	551-238
P9	Not Used	
P10	4-Pin Right Angle	551-240
P11	Not Used	
P12	5-Pin	551-245
P13	16-Pin	551-242
P14	16-Pin	551-242
P15	10-Pin, Straight	551-234
P16	16-Pin	551-242
P17	16-Pin	551-242
P18 thru P30	3-Pin, Right Angle	551-238
P31	9-Pin	551-243
P32	Not Used	
P33	2-Pin, Right Angle	551-241
P34	2-Pin, Right Angle	551-241
P35	3-Pin, Right Angle	551-238
P36	3-Pin, Right Angle	551-238
P37	2-Pin, Right Angle	551-241
P38	2-Pin, Right Angle	551-241
P39	3-Pin, Right Angle	551-238
XA1 thru XA10 & XA13	Receptacle, PCB, 56-Pin	551-198
XA16	Socket, 16-Pin, DIP	553-48

TRANSISTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
Q1	Transistor, NPN	20-MPSA42
Q2	Transistor, PNP	20-MPSA92
Q3	Transistor, PNP	20-MPSA92
Q4	Transistor, NPN	20-2N3694
Q5	Transistor, PNP	20-2N4249
Q6	Transistor, PNP	20-2N4249
Q7	Transistor, PNP	20-2N4249
Q8	Transistor, NPN	20-2N3694
Q9	Transistor, PNP	20-2N4249
Q10	Transistor, NPN	20-2N3694
Q11	Transistor, PNP	20-2N4249
Q12	Transistor, NPN	20-2N3694
Q13	Transistor, PNP	20-2N4249
Q14	Transistor, PNP	20-2N4249
Q15	Transistor, NPN	20-2N3694
Q16	Transistor, PNP	20-2N4249
Q17	Transistor, PNP	20-2N4249
Q18	Transistor, NPN	20-2N3694
Q19	Transistor, PNP	20-2N4249
Q20	Transistor, PNP	20-2N4249
Q21	Transistor, PNP	20-2N4249
Q22	Transistor, NPN	20-2N3694

RESISTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
R1	MF, 1/4W, 1%, 16.9k	110-16.9k-1
R2	MF, 1/4W, 1%, 3.32k	110-3.32k-1
R3	MF, 1/4W, 1%, 196Ω	110-196-1
R4	MF, 1/4W, 1%, 1.78k	110-1.78k-1
R5	MF, 1/4W, 1%, 1.27k	110-1.27k-1
R6	MF, 1/4W, 1%, 5.9k	110-5.9k-1
R7	Variable, Single Turn, 2k	156-2k-A
R8	WW, 3W, 1Ω	130-1-3
R9	MF, 1/4W, 1%, 100Ω	110-100-1
R10	CC, 1/2W, 5%, 5.6k	102-5.6k-5
R11	MF, 1/4W, 1%, 12.7k	110-12.7k-1
R12	MF, 1/4W, 1%, 2.21k	110-2.21k-1
R13	MF, 1/4W, 1%, 10Ω	110-10-1
R14	CC, 1/2W, 5%, 100k	102-100k-5
R15	CC, 1/2W, 5%, 100k	102-100k-5
R16	WW, 3W, 1Ω	130-1-3
R17	MF, 1/4W, 1%, 100Ω	110-100-1
R18	MF, 1/4W, 1%, 365Ω	110-365-1
R19	MF, 1/4W, 1%, 3.32k	110-3.32k-1
R20	MF, 1/4W, 1%, 19.1Ω	110-19.1-1
R21	MF, 1/4W, 1%, 42.2Ω	110-42.2
R22	MF, 1/4W, 1%, 61.9k	110-61.9k-1
R23	MF, 1/4W, 1%, 88.7k	110-88.7k-1
R24	MF, 1/4W, 1%, 88.7k	110-88.7k-1
R25	MF, 1/4W, 1%, 215k	110-215k-1
R26	MF, 1/4W, 1%, 61.9k	110-61.9k-1
R27	MF, 1/4W, 1%, 107k	110-107k-1
R28	MF, 1/4W, 1%, 2k	110-2k-1
R29	MF, 1/4W, 1%, 6.81kΩ	110-6.81k-1
R30	MF, 1/4W, 1%, 2k	110-2k-1
R31	MF, 1/4W, 1%, 6.81kΩ	110-6.81k-1
R32	MF, 1/4W, 1%, 2k	110-2k-1
R33	MF, 1/4W, 1%, 6.81kΩ	110-6.81k-1
R34	WW, 3W, 120Ω	130-120-3
R35	MF, 1/4W, 1%, 10k	110-10k-1
R36	MF, 1/4W, 1%, 10k	110-10k-1
R37	CC, 2W, 5%, 220Ω	104-220-5
R38	MF, 1/4W, 1%, 10k	110-10k-1
R39	MF, 1/4W, 1%, 10k	110-10k-1
R40	MF, 1/4W, 1%, 69.8Ω	110-69.8-1
R41	MF, 1/4W, 1%, 100Ω	110-100-1
R42	MF, 1/4W, 1%, 69.8Ω	110-69.8-1
R43	MF, 1/4W, 1%, 69.8Ω	110-69.8-1
R44	MF, 1/4W, 1%, 6.81kΩ	110-6.81k-1
R45	MF, 1/4W, 1%, 2k	110-2k-1
R46	MF, 1/4W, 1%, 6.81kΩ	110-6.81k-1

R47	MF, 1/4W, 1%, 2k	110-2k-1
R48	MF, 1/4W, 1%, 68.1Ω	110-68.1-1
R49	Not Used	
R50	CC, 2W, 5%, 220Ω	104-220-5
R51	Not Used	
R52	Not Used	
R53	Not Used	
R54	Not Used	
R55	Not Used	
R56	Not Used	
R57	Not Used	
R58	Not Used	
R59	Not Used	
R60	Not Used	
R61	MF, 1/4W, 1%, 10k	110-10k-1
R62	Not Used	
R63	Not Used	
R64	Not Used	
R65	MF, 1/4W, 1%, 10k	110-10k-1
R66	Not Used	
R68	CC, 2W, 5%, 220Ω	104-220-5
R69	MF, 1/4W, 1%, 11.8k	110-11.8k-1
R70	MF, 1/4W, 1%, 10k	110-10k-1
R71	MF, 1/4W, 1%, 100Ω	110-100-1
R72	MF, 1/4W, 1%, 10.5k	110-10.5k-1
R73	MF, 1/4W, 1%, 12.7k	110-12.7k-1
R74	MF, 1/4W, 1%, 1.33k	110-1.33k-1
R75	MF, 1/4W, 1%, 15.4k	110-15.4k-1
R76	MF, 1/4W, 1%, 4.99k	110-4.99k-1
R77	MF, 1/4W, 1%, 10k	110-10k-1
R78	MF, 1/4W, 1%, 287Ω	110-287-1
R79	Variable, Single Turn, 5k	156-5k-A
R80	Variable, Single Turn, 5k	156-5k-A
R81	MF, 1/4W, 1%, 200k	110-200k-1
R82	MF, 1/4W, 1%, 10k	110-10k-1
R83	MF, 1/4W, 1%, 4.99k	110-4.99k-1
R84	MF, 1/4W, 1%, 2k	110-2k-1
R85	MF, 1/4W, 1%, 2k	110-2k-1
R86	MF, 1/4W, 1%, 2k	110-2k-1
R87	MF, 1/4W, 1%, 22.1k	110-22.1k-1
R88	MF, 1/4W, 1%, 12.1k	110-12.1k-1
R89	Variable, Multi-Turn, 100k	157-100kA
R90	MF, 1/4W, 1%, 287Ω	110-287-1
R91	MF, 1/4W, 1%, 287Ω	110-287-1
R92	MF, 1/4W, 1%, 287Ω	110-287-1
R93	MF, 1/4W, 1%, 22.1k	110-22.1k-1
R94	MF, 1/4W, 1%, 22.1k	110-22.1k-1
R95	MF, 1/4W, 1%, 22.1k	110-22.1k-1
R96	MF, 1/4W, 1%, 10k	110-10k-1
R97	MF, 1/4W, 1%, 10k	110-10k-1
R98	MF, 1/4W, 1%, 10k	110-10k-1
R99	CC, 1/2W, 5%, 0.5Ω	102-.5-5
R100	CC, 1/2W, 5%, 0.5Ω	102-.5-5
R101	CC, 1/2W, 5%, 0.5Ω	102-.5-5
R102	MF, 1/4W, 1%, 4.99k	110-4.99k-1
R103	MF, 1/4W, 1%, 2k	110-2k-1
R104	MF, 1/4W, 1%, 6.81k	110-6.81k-1
R105	MF. 1/4W, 1%, 68.1k	110-68.1-1
R106	MF, 1/4W, 1%, 100Ω	110-100-1
R107	MF, 1/4W, 1%, 31.6Ω	110-31.6-1
R108	MF, 1/4W, 1%, 68.1Ω	110-68.1-1
RP1	Resistor Network	123-6
RP2	Resistor Network	123-6
RP3	Resistor Network	123-6
RP4	Resistor Network	123-6

INTEGRATED CIRCUITS

REF. DES.	DESCRIPTION	WILTRON PART NO.
U1	Optical Isolator, 820	20-820
U2	Voltage Regulator, 24V	54-152
U3	Not Used	
U4	Op Amp, LM10	50-16
U5	Quad Comparator, MC3302P	54-MC3302P
U6	Octal Latch, 74LS374	54-41
U7	Octal Latch, 74LS373	54-103
U8	Octal Latch, 74LS373	54-103
U9	Dual D Flip-Flop 74LS74	54-44
U10	Octal Latch, 74LS373	54-103

MISCELLANEOUS

REF. DES.	DESCRIPTION	WILTRON PART NO.
—	Clip, Fuse	553-37
F1	Fuse, 5A, FB, 3AG	631-25
K1	Relay, 5V, SPDT	690-19
L1	Inductor Assembly, SPEC-A-8080	310-68
L2	Inductor Assembly, SPEC-A-8080	310-68
RT1	Thermistor	35-7
RT2	Thermistor	35-7
RV1	Varistor	35-6
RV2	Varistor	35-6
TP1 thru TP6	Test Points	706-44
XA16	Socket, 16 Pin, DIP	553-48

INDEX NO.	NAME	PART OR DWG. NO.
1	Potentiometer Assembly, EXTERNAL ALC GAIN	660-A-8024
2	Cable Assembly, (EXTERNAL INPUT to A14P37)	660-A-8023
3	A12 Microprocessor PCB (See Table 6-12)	660-D-8012
4	A11 Front Panel PCB (See Table 6-11)	660-D-8011
5	Switch Assembly, INCREASE-DECREASE	660-B-8017
6	Subpanel	660-D-8042
7	Button, RESET	560-A-7075
8	Button, Grey (40 ea.)	430-106
9	Button, SHIFT	660-A-8177
10	Buttons, Keypad	
	a. "1"	660-A-8073-1
	b. "2"	660-A-8073-2
	c. "3"	660-A-8073-3
	d. "4"	660-A-8073-4
	e. "5"	660-A-8073-5
	f. "6"	660-A-8073-6
	g. "7"	660-A-8073-7
	h. "8"	660-A-8073-8
	i. "9"	660-A-8073-9
	j. "0"	660-A-8073-10
	k. "."	660-A-8073-11
	l. "-"	660-A-8073-12
–	Knob (MANUAL SWEEP and MARKER AMPLITUDE)	61084-A-5452
–	Insert (2 ea.)	A710-56
–	Knob, Push to Check (EXTERNAL ALC GAIN)	660-A-8064
–	Insert	710-56
–	Front Panel (Plastic)	660-D-8043
–	Connector, BNC, Insulated (EXTERNAL INPUT)	510-31
–	Connector Housing, 2-pin	551-230
–	Female Pins	551-154
–	Connector, Insulated Displacement for RF 174	551-233
–	Knob Retainer	710-56
–	Cable Coax	800-5

Figure 6-5. A15 Front Panel Assembly, Dwg. 660-D-8015
(See Figure 6-4 for next higher assembly) (Sheet 1 of 2)

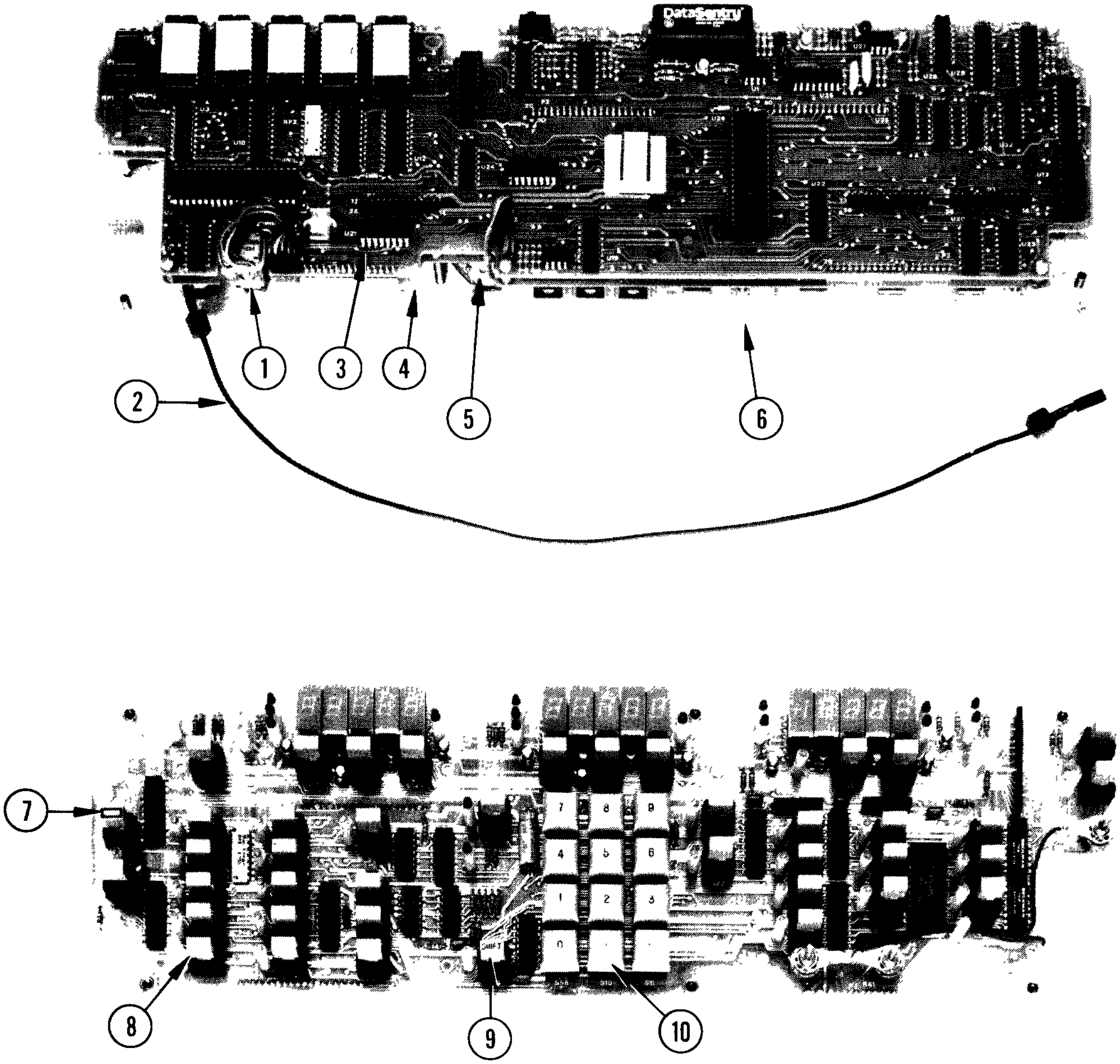


Figure 6-5. A15 Front Panel Assembly, Dwg. 660-D-8015
(See Figure 6-4 for next higher assembly) (Sheet 2 of 2)

Table 6-11. A11 Front Panel PCB, Dwg. 660-D-8011-3
(See Figure 6-5 for next higher assembly)

CAPACITORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
C1	Electrolytic, 250µF, 25V	250-53
C2	Monolithic, 0.1µF, 50V	230-37
C3	Monolithic, 0.1µF, 50V	230-37
C4	Monolithic, 0.1µF, 50V	230-37
C5	Monolithic, 0.1µF, 50V	230-37
C6	Monolithic, 0.1µF, 50V	230-37
C7	Monolithic, 0.1µF, 50V	230-37
C8	Monolithic, 0.1µF, 50V	230-37

DIODES

REF. DES.	DESCRIPTION	WILTRON PART NO.
DS1	Light Emitting, Red	15-5
DS2	Light Emitting, Red	15-5
DS3	Light Emitting, Red	15-5
DS4	Light Emitting, Red	15-5
DS5	Light Emitting, Red	15-5
DS6	Light Emitting, Red	15-5
DS7	Light Emitting, Red	15-5
DS8	Light Emitting, Red	15-5
DS9	Not Used	
DS10	Light Emitting, Red	15-5
DS11	Light Emitting, Red	15-5
DS12	Not Used	
DS13	Light Emitting, Red	15-5
DS14	Not Used	
DS15	Not Used	
DS16	Light Emitting, Yellow	15-7
DS17	Not Used	
DS18	Light Emitting, Red	15-5
DS19	Light Emitting, Yellow	15-7
DS20	Light Emitting, Yellow	15-7
DS21	Light Emitting, Yellow	15-7
DS22	Light Emitting, Yellow	15-7
DS23	Light Emitting, Yellow	15-7
DS24	Light Emitting, Yellow	15-7
DS25	Light Emitting, Yellow	15-7
DS26	Light Emitting, Yellow	15-7
DS27	Light Emitting, Yellow	15-7
DS28	Light Emitting, Yellow	15-7
DS29	Light Emitting, Yellow	15-7
DS30	Light Emitting, Yellow	15-7
DS31	Light Emitting, Yellow	15-7
DS32	Light Emitting, Yellow	15-7
DS33	Light Emitting, Yellow	15-7
DS34	Not Used	
DS35	Light Emitting, Red	15-5
DS36	Light Emitting, Yellow	15-7
DS37	Light Emitting, Yellow	15-7
DS38	Light Emitting, Yellow	15-7
DS39	Light Emitting, Yellow	15-7
DS40	Light Emitting, Yellow	15-7
DS41	Light Emitting, Yellow	15-7
DS42	Light Emitting, Yellow	15-7
DS43	Light Emitting, Yellow	15-7
DS44	Light Emitting, Yellow	15-7
DS45	Light Emitting, Yellow	15-7
DS46	Light Emitting, Yellow	15-7
DS47	Light Emitting, Yellow	15-7
DS48	Display, 7-Segment, LED	15-15
DS49	Display, 7-Segment, LED	15-15
DS50	Display, 7-Segment, LED	15-15
DS51	Display, 7-Segment, LED	15-15
DS52	Display, 7-Segment, LED	15-15
DS53	Display, 7-Segment, LED	15-15
DS54	Display, 7-Segment, LED	15-15
DS55	Display, 7-Segment, LED	15-15
DS56	Display, 7-Segment, LED	15-15
DS57	Display, 7-Segment, LED	15-15
DS58	Display, +/- 1, LED	15-14
DS59	Display, 7-Segment, LED	15-15
DS60	Display, 7-Segment, LED	15-15
DS61	Display, 7-Segment, LED	15-15
DS62	Display, 7-Segment, LED	15-15
DS63	Light Emitting, Red	15-5
DS64	Light Emitting, Red	15-5
DS65	Light Emitting, Yellow	15-7
DS66	Light Emitting, Yellow	15-7
DS67	Light Emitting, Yellow	15-7
DS68	Light Emitting, Yellow	15-7
DS69	Light Emitting, Yellow	15-7
DS70	Light Emitting, Yellow	15-7
DS71	Light Emitting, Yellow	15-7
DS72	Light Emitting, Yellow	15-7
DS73	Light Emitting, Red	15-5

CONNECTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
J1	20 Pin, SIP, Female	551-173
J2	20 Pin, SIP, Female	551-173
J3	20 Pin, SIP, Female	551-173
J4	20 Pin, SIP, Female	551-173

TRANSISTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
Q1	PNP, 2N2907	20-2N2907
Q2	PNP, 2N2907	20-2N2907
Q3	PNP, 2N2907	20-2N2907
Q4	PNP, 2N2907	20-2N2907
Q5	PNP, 2N2907	20-2N2907
Q6	PNP, 2N2907	20-2N2907
Q7	PNP, 2N2907	20-2N2907
Q8	PNP, 2N2907	20-2N2907
Q9	PNP, 2N2907	20-2N2907
Q10	PNP, 2N2907	20-2N2907
Q11	PNP, 2N2907	20-2N2907
Q12	PNP, 2N2907	20-2N2907
Q13	PNP, 2N2907	20-2N2907
Q14	PNP, 2N2907	20-2N2907
Q15	PNP, 2N2907	20-2N2907

RESISTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
R1	MF, 1/4W, 1%, 215Ω	110-215-1
R2	MF, 1/4W, 1%, 215Ω	110-215-1
R3	MF, 1/4W, 1%, 215Ω	110-215-1
R4	Not Used	
R5	MF, 1/4W, 1%, 215Ω	110-215-1

R6	MF, 1/4W, 1%, 215Ω	110-215-1
R7	MF, 1/4W, 1%, 215Ω	110-215-1
R8	Not Used	
R9	MF, 1/4W, 1%, 215Ω	110-215-1
R10	MF, 1/4W, 1%, 215Ω	110-215-1
R11	MF, 1/4W, 1%, 215Ω	110-215-1
R12	MF, 1/4W, 1%, 215Ω	110-215-1
R13	MF, 1/4W, 1%, 215Ω	110-215-1
R14	MF, 1/4W, 1%, 215Ω	110-215-1
R15	MF, 1/4W, 1%, 215Ω	110-215-1
R16	MF, 1/4W, 1%, 215Ω	110-215-1
R17	MF, 1/4W, 1%, 215Ω	110-215-1
R18	MF, 1/4W, 1%, 215Ω	110-215-1
R19	Not Used	
R20	MF, 1/4W, 1%, 215Ω	110-215-1
R21	MF, 1/4W, 1%, 215Ω	110-215-1
R22	MF, 1/4W, 1%, 215Ω	110-215-1
R23	MF, 1/4W, 1%, 215Ω	110-215-1
R24	MF, 1/4W, 1%, 147Ω	110-147-1
R25	MF, 1/4W, 1%, 147Ω	110-147-1
R26	MF, 1/4W, 1%, 147Ω	110-147-1
R27	MF, 1/4W, 1%, 147Ω	110-147-1
R28	MF, 1/4W, 1%, 147Ω	110-147-1
R29	MF, 1/4W, 1%, 147Ω	110-147-1
R30	MF, 1/4W, 1%, 147Ω	110-147-1
R31	MF, 1/4W, 1%, 147Ω	110-147-1
R32	MF, 1/4W, 1%, 215Ω	110-215-1
R33	MF, 1/4W, 1%, 4.64k	110-4.64k-1
R34	MF, 1/4W, 1%, 215Ω	110-215-1
R35	MF, 1/4W, 1%, 215Ω	110-215-1
R36	MF, 1/4W, 1%, 215Ω	110-215-1
R37	MF, 1/4W, 1%, 215Ω	110-215-1
R38	MF, 1/4W, 1%, 10k	110-10k-1
R39	Not Used	
R40	Variable, 20k	146-3
R41	Variable, 20k	146-3
R42	Not Used	
R43	Variable, 20k	146-5
RP1	DIP, 56Ω	123-11
RP2	DIP, 220Ω	123-12
RP3	DIP, 220Ω	123-12
RP4	DIP, 220Ω	123-13
RP5	SIP, 220Ω	123-14
RP6	SIP, 220Ω	123-14
RP7	SIP, 4.7k	123-15
RP8	SIP, 4.7k	123-15

SWITCHES

REF. DES.	DESCRIPTION	WILTRON PART NO.
S1	SPST, Momentary	430-130
S2	SPST, Momentary	430-130
S3	SPST, Momentary	430-130
S4	SPST, Momentary	430-130
S5	SPST, Momentary	430-130
S6	SPST, Momentary	430-130
S7	SPST, Momentary	430-130
S8	SPST, Momentary	430-130
S9	SPST, Momentary	430-130
S10	SPST, Momentary	430-130
S11	SPST, Momentary	430-130
S12	SPST, Momentary	430-130
S13	DPST, Momentary	430-131
S14	DPST, Momentary	430-131
S15	SPST, Momentary	430-130
S16	SPST, Momentary	430-130
S17	DPST, Momentary	430-131
S18	SPST, Momentary	430-130
S19	SPST, Momentary	430-130
S20	Not Used	
S21	Not Used	
S22	SPST, Momentary	430-130
S23	SPST, Momentary	430-130
S24	SPST, Momentary	430-130
S25	SPST, Momentary	430-130
S26	Not Used	
S27	SPST, Momentary	430-130
S28	SPST, Momentary	430-130
S29	SPST, Momentary	430-130
S30	SPST, Momentary	430-130
S31	SPST, Momentary	430-130
S32	SPST, Momentary	430-130
S33	SPST, Momentary	430-130
S34	SPST, Momentary	430-130
S35	SPST, Momentary	430-130
S36	SPST, Momentary	430-130
S37	DPST, Momentary	430-131
S38	DPST, Momentary	430-131
S39	SPST, Momentary	430-130
S40	Not Used	
S41	Not Used	
S42	SPST, Momentary	430-130
S43	SPST, Momentary	430-130
S44	SPST, Momentary	430-130
S45	SPST, Momentary	430-130
S46	SPST, Momentary	430-130
S47	SPST, Momentary	430-130
S48	SPST, Momentary	430-130
S49	SPST, Momentary	430-130
S50	SPST, Momentary	430-130
S51	SPST, Momentary	430-130
S52	SPST, Momentary	430-130
S53	SPST, Momentary	430-130
S54	DPST, Momentary	430-131
S55	SPST, Momentary	430-130
S56	SPST, Momentary	430-130
S57	SPST, Momentary	430-130
S58	SPST, Momentary	430-130

INTEGRATED CIRCUITS

REF. DES.	DESCRIPTION	WILTRON PART NO.
U1	74LS374, Octal Latch	54-41
U2	74LS374, Octal Latch	54-41
U3	74LS374, Octal Latch	54-41
U4	74LS374, Octal Latch	54-41
U5	74LS374, Octal Latch	54-41
U6	74LS374, Octal Latch	54-41
U7	74LS138, 3 to 8 Decoder	54-74LS138
U8	7406, HEX Inverter	54-104
U9	7406, HEX Inverter	54-104
U10	7406, HEX Inverter	54-104
U11	74154, 4 to 16 Decoder	54-147

MISCELLANEOUS

REF. DES.	DESCRIPTION	WILTRON PART NO.
—	Socket, DIP, 14 Pin	551-143
—	Standoff, Nylon (Long LED)	790-129
—	Standoff, Nylon (Short LED)	790-130
—	Standoff, Nylon (Display LED)	790-131

Table 6-12. A12 Microprocessor PCB, Dwg. 660-D-8012-3
(See Figure 6-5 for next higher assembly)

CAPACITORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
C1	Tantalum, 10μF, 25V	250-42
C2	Tantalum, 10μF, 25V	250-42
C3	Mylar, 0.047μF, 250V	210-28
C4	Tantalum, 1μF, 35V	250-19
C5	Disc Ceramic, 0.01μF, 100V	230-11
C6	Mylar, 0.1μF, 250V	210-30
C7	Disc Ceramic, 0.01μF, 100V	230-11
C8	Disc Ceramic, 0.01μF, 100V	230-11
C9	Disc Ceramic, 0.01μF, 100V	230-11
C10	Monolithic, 0.1μF, 50V	230-37
C11	Monolithic, 0.1μF, 50V	230-37
C12	Monolithic, 0.1μF, 50V	230-37
C13	Monolithic, 0.1μF, 50V	230-37
C14	Monolithic, 0.1μF, 50V	230-37
C15	Monolithic, 0.1μF, 50V	230-37
C16	Monolithic, 0.1μF, 50V	230-37
C17	Monolithic, 0.1μF, 50V	230-37
C18	Monolithic, 0.1μF, 50V	230-37
C19	Monolithic, 0.1μF, 50V	230-37
C20	Monolithic, 0.1μF, 50V	230-37

DIODES

REF. DES.	DESCRIPTION	WILTRON PART NO.
CR1	Rectifier	10-SI2
CR2	1N4446	10-1N4446
CR3	1N4446	10-1N4446
CR4	1N4446	10-1N4446
CR5	1N4446	10-1N4446

CONNECTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
P1	20 Pin, Male	551-215
P2	20 Pin, Male	551-215
P3	20 Pin, Male	551-215
P4	20 Pin, Male	551-215
P5	26 Pin, Male	551-102
P6	26 Pin, Male	551-102
P7	26 Pin, Male	551-102
P8	3 Pin, Male	551-207
P9	Plug, DIP, 18 Pin	551-236

TRANSISTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
Q1	PNP, MJE371	20-24
Q2	NPN, 2N2222A	20-2N2222A
Q3	NPN, 2N2222A	20-2N2222A
Q4	NPN, 2N2222A	20-2N2222A

RESISTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
R1	MF, 1/4W, 1%, 12.1k	110-12.1k-1
R2	MF, 1/4W, 1%, 150Ω	110-150-1
R3	MF, 1/4W, 1%, 46.4k	110-46.4k-1
R4	MF, 1/4W, 1%, 10kΩ	110-10k-1
R5	MF, 1/4W, 1%, 68.1k	110-68.1k-1
R6	MF, 1/4W, 1%, 237k	110-237k-1
R7	MF, 1/4W, 1%, 100k	110-100k-1
R8	MF, 1/4W, 1%, 10kΩ	110-10k-1
R9	MF, 1/4W, 1%, 100k	110-100k-1
R10	MF, 1/4W, 1%, 1M	110-1M-1A
R11	CC, 1/2W, 5%, 430Ω	102-430-5
R12	MF, 1/4W, 1%, 10kΩ	110-10k-1
R13	MF, 1/4W, 1%, 10kΩ	110-10k-1
R14	MF, 1/4W, 1%, 10kΩ	110-10k-1
R15	MF, 1/4W, 1%, 10kΩ	110-10k-1
R16	MF, 1/4W, 1%, 100k	110-100k-1
R17	MF, 1/4W, 1%, 10kΩ	110-10k-1
R18	MF, 1/4W, 1%, 10kΩ	110-10k-1
R19	MF, 1/4W, 1%, 10kΩ	110-10k-1
R20	MF, 1/4W, 1%, 10kΩ	110-10k-1
R21	MF, 1/4W, 1%, 100k	110-100k-1
R22	MF, 1/4W, 1%, 100k	110-100k-1
R23	MF, 1/4W, 1%, 100k	110-100k-1
R24	MF, 1/4W, 1%, 10kΩ	110-10k-1
R25	MF, 1/4W, 1%, 10kΩ	110-10k-1
R26	MF, 1/4W, 1%, 10kΩ	110-10k-1
R27	MF, 1/4W, 1%, 100k	110-100k-1
R28	MF, 1/4W, 1%, 10kΩ	110-10k-1
R29	MF, 1/4W, 1%, 215Ω	110-215-1
R30	MF, 1/4W, 1%, 215Ω	110-215-1
R31	MF, 1/4W, 1%, 10kΩ	110-10k-1
R32	MF, 1/4W, 1%, 10kΩ	110-10k-1
R33	MF, 1/4W, 1%, 10kΩ	110-10k-1
R34	MF, 1/4W, 1%, 10kΩ	110-10k-1
R35	MF, 1/4W, 1%, 10kΩ	110-10k-1
R36	MF, 1/4W, 1%, 82.5k	110-82.5k-1
R37	MF, 1/4W, 1%, 31.6k	110-31.6k-1
R38	MF, 1/4W, 1%, 10kΩ	110-10k-1
R39	MF, 1/4W, 1%, 10kΩ	110-10k-1
R40	MF, 1/4W, 1%, 10kΩ	110-10k-1
R41	MF, 1/4W, 1%, 20k	110-20k-1
R42	MF, 1/4W, 1%, 20k	110-20k-1
R43	MF, 1/4W, 1%, 31.6k	110-31.6k-1
R44	MF, 1/4W, 1%, 100k	110-100k-1
R45	MF, 1/4W, 1%, 20k	110-20k-1
R46	Variable, Single turn, 10k	156-10k
R47	MF, 1/4W, 1%, 20k	110-20k-1
R48	MF, 1/4W, 1%, 100Ω	110-100-1
R49	MF, 1/4W, 1%, 10kΩ	110-10k-1
R50	MF, 1/4W, 1%, 10kΩ	110-10k-1
R51	MF, 1/4W, 1%, 1k	110-1k-1
RP1	SIP, 10k	123-6
RP2	DIP, 100k	123-10

INTEGRATED CIRCUITS

REF. DES.	DESCRIPTION	WILTRON PART NO.
U1	Micropower Comparator	54-151
U2	8085A, Microprocessor	54-93
U3	74LS373, Octal Latch	54-103
U4	74LS138, Decoder	54-74LS138
U5	2716, 2k x 8 EPROM	56-3
U6	2716, 2k x 8 EPROM	56-3
U7	2716, 2k x 8 EPROM	56-3
U8	2716, 2k x 8 EPROM	56-3
U9	Not Used	

U10	74LS244, Octal Tri-state Driver	54-143
U11	5101L-1, 256x4 CMOS RAM	54-146
U12	5101L-1, 256x4 CMOS RAM	54-146
U13	DP8304B, Bidirectional Bus Driver	54-128
U14	DP8304B, Bidirectional Bus Driver	54-128
U15	74LS04, HEX Inverter	54-74LS04
U16	74LS01, Quad NAND Gate	54-74LS01
U17	Not Used	
U18	74LS138, Decoder	54-74LS138
U19	74LS138, Decoder	54-74LS138
U20	74LS138, Decoder	54-74LS138
U21	74LS138, Decoder	54-74LS138
U22	74LS138, Decoder	54-74LS138
U23	74LS138, Decoder	54-74LS138
U24	74LS30, 8-input NAND	54-58
U25	8279-5, Keyboard/Display Interface	54-97
U26	96L02, Dual Monostable	54-96L02
U27	555, Timer	54-555
U28	74LS161, 4-Bit Binary Counter	54-60
U29	74LS374, Octal Latch	54-41
U30	74LS374, Octal Latch	54-41
U31	74LS374, Octal Latch	54-41
U32	74LS04, HEX Inverter	54-74LS04
U33	74LS04, HEX Inverter	54-74LS04
U34	74LS02, Quad 2-Input NOR	54-57
U35	74LS02, Quad 2-Input NOR	54-57
U36	TL072, Dual Op Amp	54-53

MISCELLANEOUS

REF. DES.	DESCRIPTION	WILTRON PART NO.
B1	Battery, 2.4V	633-8
S1	Switch, Slide, SPDT	420-14
Y1	Crystal, 6.000 MHz	630-17
—	Socket, 20 Pin DIP	553-98
—	Socket, 24 Pin DIP	553-67
—	Socket, 40 Pin DIP	553-66
TP1 thru TP27	Pin, Test Point	706-44

INDEX NO.	NAME	PART OR DWG. NO.
1	Shield, Fan	660-B-8142
2	Fan	650-4
3	Plug, Button, 5/8	790-42
4	Plug, Button, 1/4	790-146
5	Cover, GPIB (In place of cover, A18 GPIB Connector PCB is shown installed. See Figure 6-7 for part no.)	560-A-7041
6	Connector Housing, 15 Pin (Not shown)	553-90
	Receptacle	553-89
7	Switch, DPDT	430-49
8	Connector, BNC (10 ea.)	510-5
9	Connector, BNC, Insulated (4 ea.)	510-31
10	Plug, Button, 3/8	790-41
11	Transformer	320-58
12	Voltage Selector Module	551-142
	Female Pins, 14 ea.	551-155
13	Panel 660-D-8026	660-D-8026
14	Connector Housing, 10 Pin	551-199
	Female Pins (Pins 1 & 3-10)	551-35
	Female Pin (Pin 2)	551-200
15	Switch, POWER	430-139
–	Connector Housing, 4 Pin	551-229
–	Connector Housing, 2 Pin	551-230
	Female Pins, 6 ea.	551-154
–	Connector Insulation (Displacement for RG 174)	551-233
–	Filter, Air, SPEC-A-8063	783-116
–	Finger Guard	790-142
–	Thumb Nut	790-143
–	Cable, Shielded Pair	800-28
–	Cable, Coax, RG174	800-5
–	Cable Assembly, Flat (Between A14X16 and BNC connectors)	802-16A-15.4
–	Connector Housing, 3 Pin	551-202
	Receptacle	551-250
–	Terminal Strip	701-15

Figure 6-6. A16 Rear Panel Assembly, Dwg. 660-D-8016
(See Figure 6-4 for next higher assembly)

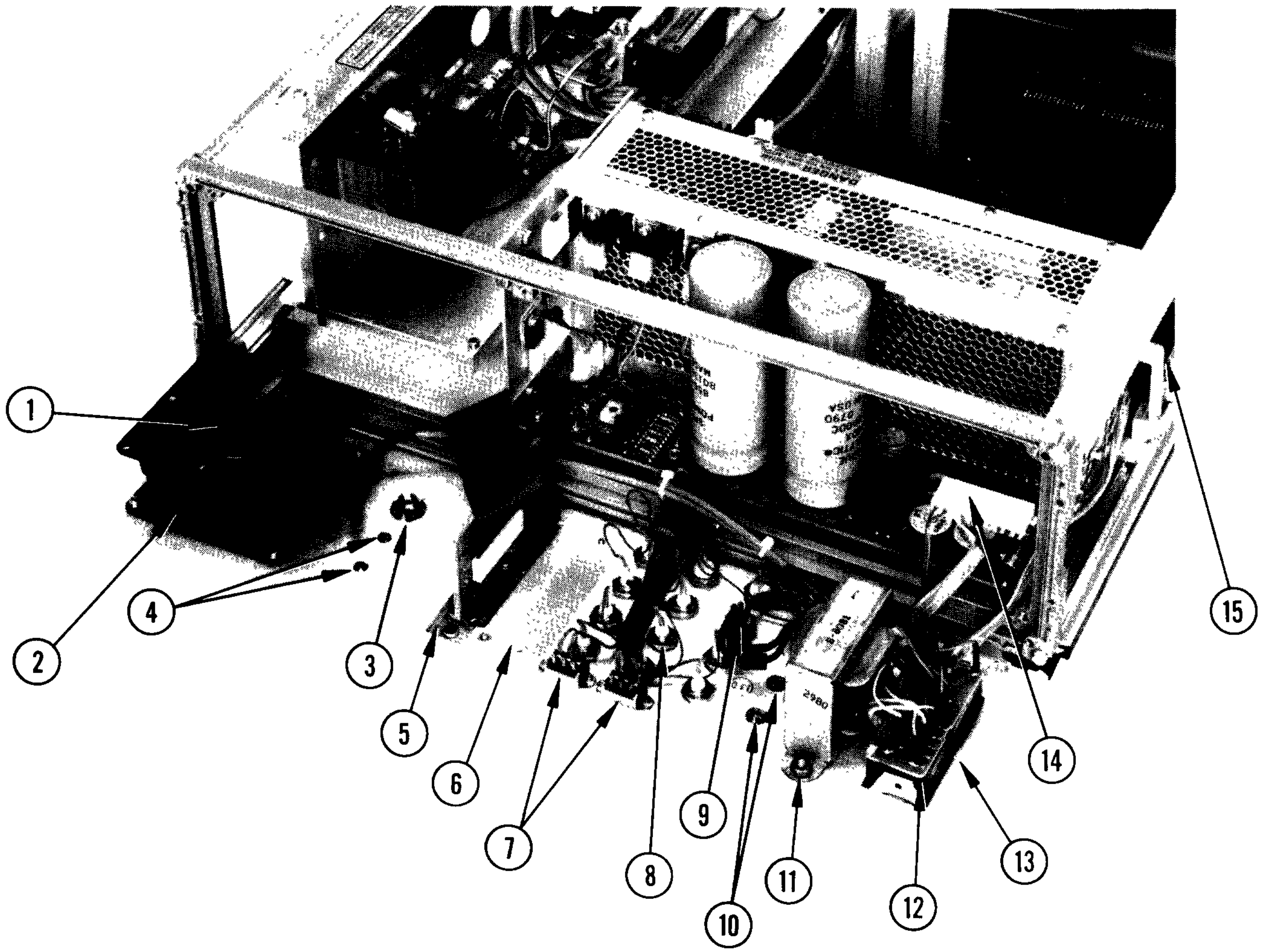
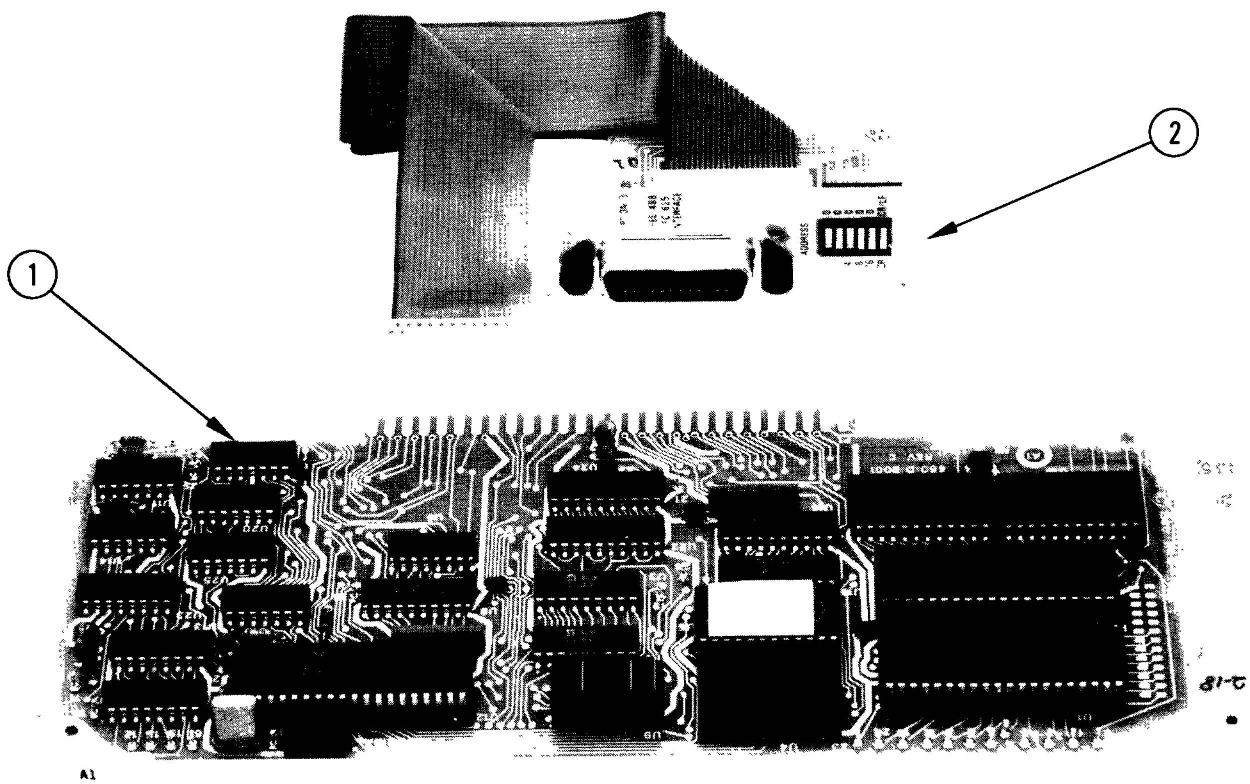


Figure 6-6. A16 Rear Panel Assembly, Dwg. 660-D-8016
(See Figure 6-4 for next higher assembly) (Sheet 2 of 2)



INDEX NO.	NAME	PART OR DWG. NO.
1	A1 GPIB Interface PCB (See Table 6-13)	660-D-8001-3
2	A18 GPIB Connector PCB (See Table 6-14)	660-B-8018

Figure 6-7. Option 3, GPIB Assembly

Table 6-13. A1 GPIB Interface PCB, Dwg. 660-D-8001-3
(See Figure 6-7 for next higher assembly)

CAPACITORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
C1	Tantalum, 2.2µF, 20V	250-40A
C2	Tantalum, 2.2µF, 20V	250-40A
C3	Tantalum, 10µF, 25V	250-42
C4	Monolithic, .1µF, 50V	230-37
C5	Monolithic, .1µF, 50V	230-37
C6	Monolithic, .1µF, 50V	230-37
C7	Monolithic, .1µF, 50V	230-37
C8	Monolithic, .1µF, 50V	230-37
C9	Monolithic, .1µF, 50V	230-37

RESISTORS

REF. DES.	DESCRIPTION	WILTRON PART NO.
R1	MF, 1/4W, 1%, 5.11k	110-5.11k-1
R2	MF, 1/4W, 1%, 10k	110-10k-1
R3	MF, 1/4W, 1%, 10k	110-10k-1
R4	MF, 1/4W, 1%, 10k	110-10k-1
R5	MF, 1/4W, 1%, 10k	110-10k-1
R6	MF, 1/4W, 1%, 40.2k	110-40.2k-1
R7	MF, 1/4W, 1%, 487Ω	110-487-1
R8	MF, 1/4W, 1%, 40.2k	110-40.2k-1
R9	MF, 1/4W, 1%, 10k	110-10k-1
RP1	Resistor Network, 10k, 8-Pin, 7-Resistor	123-6
RP2	Resistor Network, 10k, 8-Pin, 7-Resistor	123-6

INTEGRATED CIRCUITS, SOCKETS, AND PLUGS

REF. DES.	DESCRIPTION	WILTRON PART NO.
U1	8255A, Programmable Interface	54-155
U2	PD211ALC-4 256 x 4 Static RAM	54-11
U3	PD211ALC-4 256 x 4 Static RAM	54-11
U4	2716 2k x 8 EPROM	56-3
U5	2716 2k x 8 EPROM	56-3
U6	74LS155, Dual 1-of-4 Decoder	54-101
U7	74LS138, 1-of-8 Decoder	54-74LS138
U8	74LS373, Octal Latch	54-103
U9	Not Used	
U10	74LS04, Hex Inverter	54-74LS04
U11	74LS01, Quad Open Collector NAND	54-74LS01
U12	8085A, CPU	54-93
U13	74LS123 one shot	54-116
U14	7474, Dual D-Flip Flop	54-7474
U15	74LS244, Non-inverting Octal Tri-State Driver	54-143
U16	74LS244, Non-inverting Octal Tri-State Driver	54-143
U17	8291 GPIB Listener/Talker	54-124
U18	MC3447 Motorola GPIB Transreceiver, ceramic pkg., Cs. 623	54-142
U19	MC3447 Motorola GPIB Transreceiver, ceramic pkg., Cs. 623	54-142
U20	74LS74, Dual D-Flip Flop	54-44
U21	74LS74, Dual D-Flip Flop	54-44
U22	74LS374, Octal Latch	54-41
U23	74LS112, Dual JK-Flip Flop	54-74LS112
U24	74LS374, Octal Latch	54-41
U25	74LS00, Quad NAND	54-74LS00
—	Socket, Dip, 18 Pin; U9	551-148
—	Socket, Dip, 40 Pin; U1, 12, 17	553-66
—	Socket, Dip, 24 Pin; U4, 5	553-67
—	Plug, Dip, 18 Pin; U9	551-236

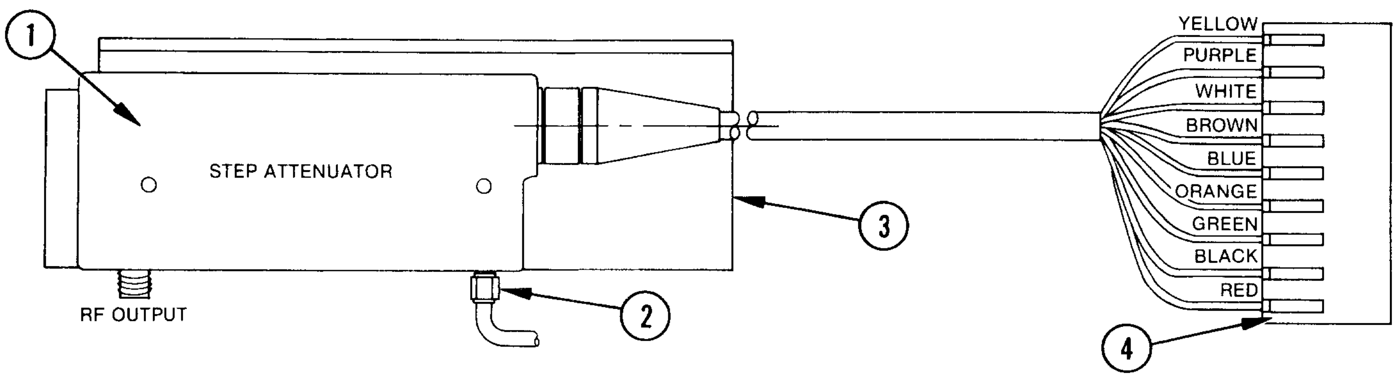
MISCELLANEOUS

REF. DES.	DESCRIPTION	WILTRON PART NO.
Q1	Transistor, 2N4249, PNP	20-2N4249
S1	Switch, Slide, SPDT	420-14
TP1 thru TP22	Test Point Pins	706-44
Y1	Crystal, 6.000 MHz	630-17
—	Ejector, P.C. Board	553-96

Table 6-14. A18 GPIB Connector PCB, Dwg. 660-B-8018

MISCELLANEOUS

REF. DES.	DESCRIPTION	WILTRON PART NO.
J2	Socket, 14 Pin Right Angle	551-149
P1	Connector, GPIB Interface	553-72
P2	Connector, Mounting Hardware	553-72A
R1	Resistor, 1/4W, 1%, 10Ω	110-10-1
S1	Switch, SPST, 6 Section	430-105
—	Cable Assy. (A18 to A14P4)	804-26E1-16 1/4



INDEX NO.	NAME	PART OR DWG. NO.
1	Option 2 Step Attenuator	1010-27
2	Cable Assembly (Coupler to Step Attenuator)	660-A-8121-1
3	Bracket, Attenuator Mounting	660-B-8119
4	Connector Housing, 9 Pin Female Pins	551-200
–	Cable Assembly, Attenuator to Rear Panel SMA Connector	660-A-8143-1
–	Option 9, Rear Panel SMA Connector Assembly (N Male) to SMA (Female) Bulkhead Connector)	660-A-8123-1
–	Option 10, Auxiliary Rear Panel RF Output	
–	SMA Connector Assembly, Panel Mounted Coupler	660-A-8143-3
–	SMA Connector Assembly, Deck Mounted Coupler	660-A-8143-4
–	RF Take-Off Assembly	660-A-9970

Figure 6-8. RF Output Options

SECTION VII

SERVICE

7-1 INTRODUCTION

This section contains general information, disassembly/reassembly instructions, and service information – circuit descriptions, schematics, parts locator diagrams, and troubleshooting data – for the overall sweep generator and individual printed circuit boards (PCBs). This service information is organized as follows:

7-2 GENERAL INFORMATION

7-2.1 Printed Circuit Board (PCB) Exchange Program

WILTRON has an exchange program that includes most of the 6600 Series PCBs. Upon request, WILTRON will immediately ship a replacement for any sweep generator PCB covered by this program. The customer has 30 days in which to return the defective PCB. Contact Customer Service at 415-969-6500 to make arrangements for an exchange.

7-2.2 Recommended Test Equipment for Troubleshooting

A list of the recommended test equipment for troubleshooting the Model 6637, 6638, 6647, and 6648 Programmable Sweep Generators is provided in Table 7-1.

7-3 6600 SERIES PROGRAMMABLE SWEEP GENERATOR, REMOVAL AND REINSTALLATION INSTRUCTIONS

Instructions for the removal and reinstallation or the disassembly and reassembly of certain 6600 Series Sweep Generator components and subassemblies are provided in paragraphs 7-3.1 thru 7-3.5.

7-3.1 Front Panel Assembly, Removal and Reinstallation Instructions

a. Removal.

1. Turn off ac power.
2. Remove the top, bottom, and side covers of the basic frame as follows:
   (a) Remove the four corner brackets from the rear panel (Figure 7-1).
   (b) Slide the covers to the rear and remove.
3. Stand the sweep generator on its side, with the RF Components Deck up.
4. Disconnect the cable connector from A14P37 (Figure 7-2).
5. Using a 3/32-inch hex wrench, remove the four corner and two mid-panel screws securing the front panel assembly to the basic frame (Figure 7-3).
6. Reposition the sweep generator top-side up (sitting on its feet); gently push the front panel assembly away from the front of the basic-frame assembly.

Table 7-1. Recommended Test Equipment for Troubleshooting

INSTRUMENT	REQUIRED CHARACTERISITCS	RECOMMENDED MANUFACTURER
Digital Multimeter	Dc Voltage: .05% to 30V .002% to 10V.	John Fluke Co. Model 8600A
Oscilloscope	60 MHz bandwidth, 1mV vertical sensitivity, and variable external horizontal input capability.	Tektronix Models 5440/ 5A18/5B10
Scalar Network Analyzer	Ability to display frequency response of sweep generator.	WILTRON Model 560
RF Detector	Ability to detect signals within the 10 MHz to 18 GHz frequency range.	WILTRON Model 75N50
Signature Analyzer	Ability to make signature analysis of microprocessor circuitry.	Hewlett-Packard Model 5004A
Directional Coupler	Ability to couple signals within a portion of the 10 MHz to 18 GHz frequency range.	NARDA Model 3202B-10

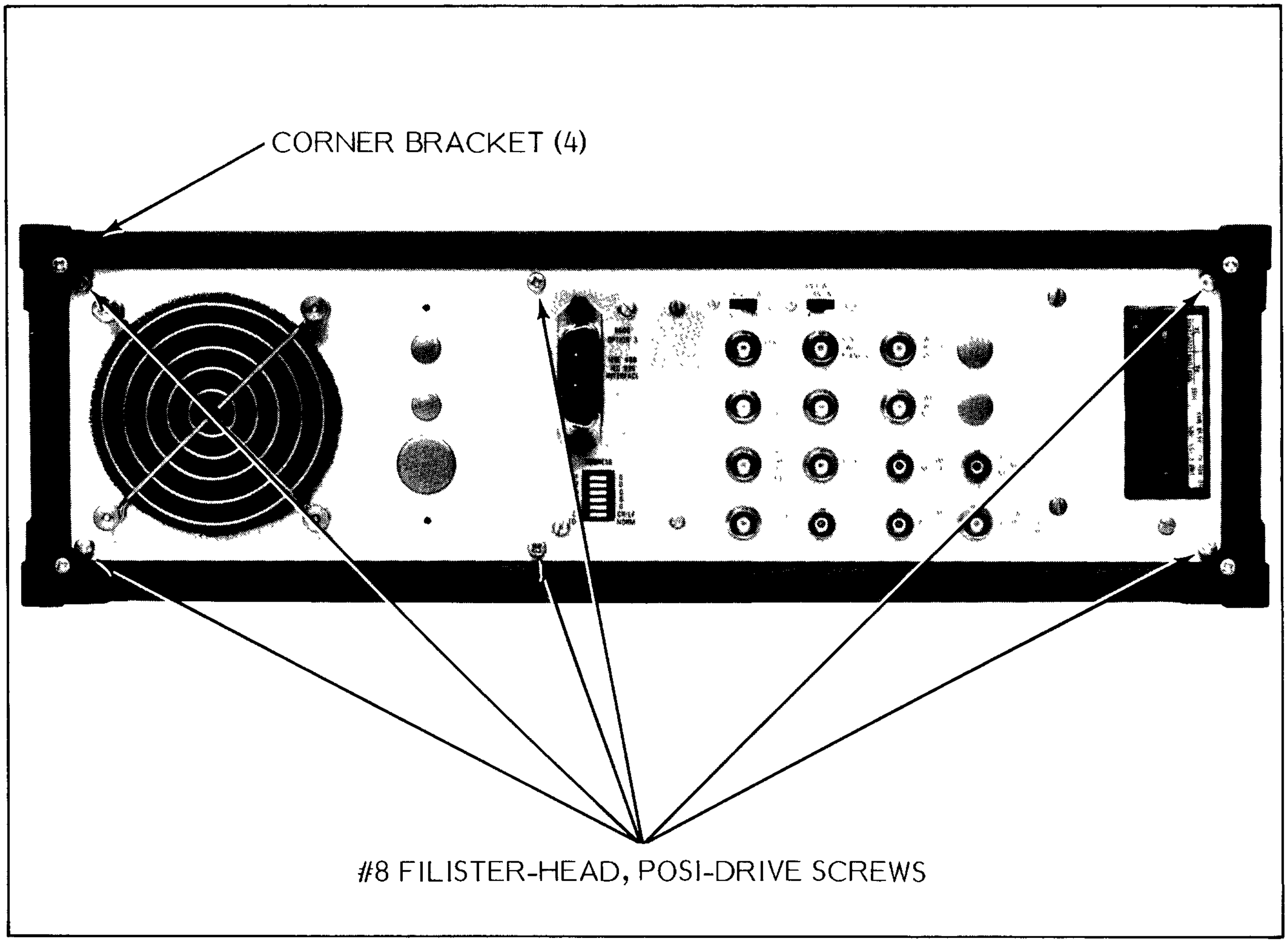


Figure 7-1. 6600 Series Programmable Sweep Generator, Rear Panel

7. Disconnect the ribbon connectors from P5, P6, and P7 on the A12 Microprocessor PCB. Use care to avoid bending the connector pins.

b. Reinstallation. The reinstallation procedure for the front panel assembly is a reversal of the removal procedure.

CAUTION

To prevent chafing, insure that the 3-wire harness going to A12P8 is well clear of the bottom mid-panel screw that secures the front panel assembly to the basic frame.

7-3.2 Front Panel, Disassembly and Reassembly Instructions

a. Disassembly.

1. Remove the front panel assembly from the basic frame; refer to paragraph 7-3.1.

CAUTION

The INCREASE-DECREASE lever extends out approximately 1/4 inch beyond the surfaces of the front panel pushbuttons. Use care to prevent bending the lever shaft.

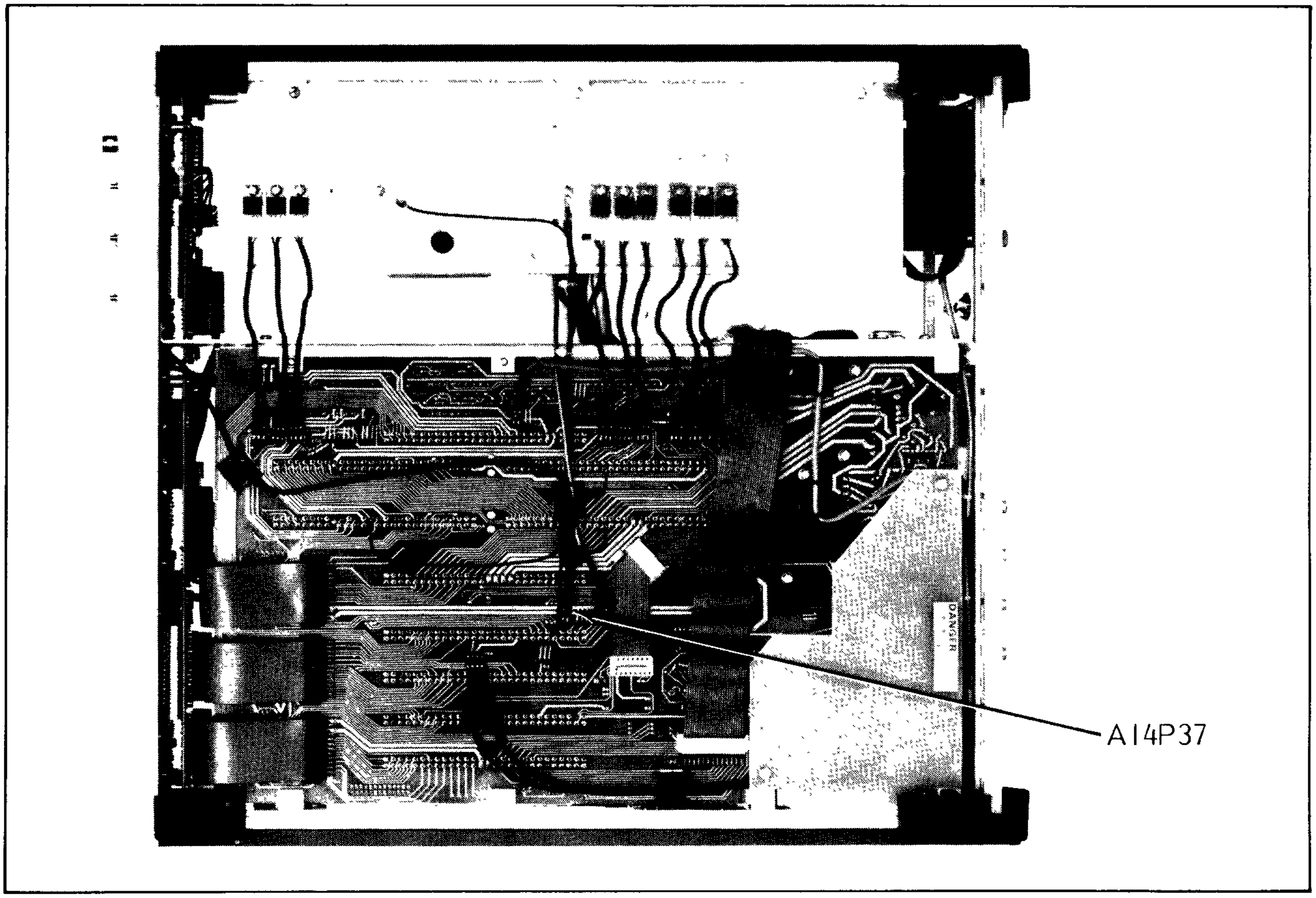


Figure 7-2. 6600 Series Programmable Sweep Generator, Bottom View

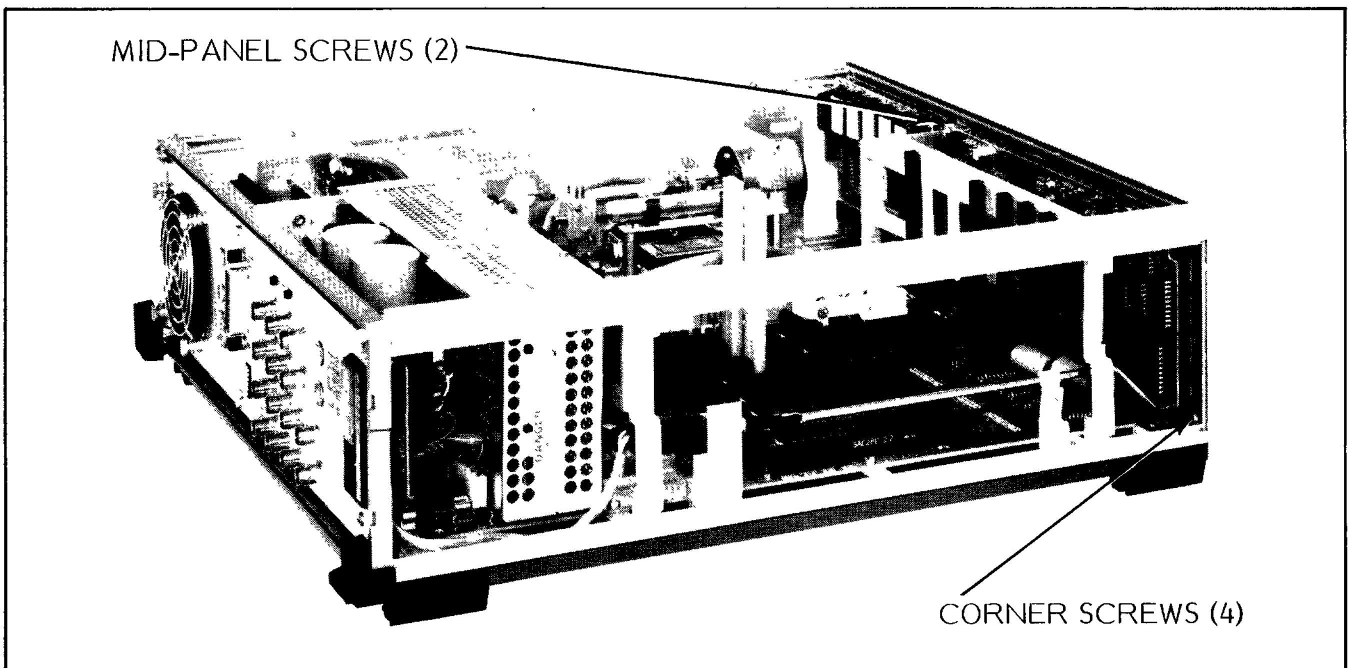


Figure 7-3. 6600 Series Programmable Sweep Generator, Side View

2. Disconnect the 5-wire connector from A12P4.

3. Disconnect the 3-wire connector from A12P8.

CAUTION

The A12 and A11 PCBs are interconnected using 4 in-line-pin connectors (Figure 7-4). When separating the two PCBs, use care to avoid bending connector pins.

4. Remove the six 1/2-inch 4-40 screws, flatwashers, and lockwashers from the A12 PCB; separate the A12 PCB from the A11 PCB.

5. Remove the knobs from the MANUAL SWEEP, MARKER AMPLITUDE, and EXTERNAL ALC GAIN controls. To remove, pull knobs straight off.

6. Remove the eight 7/8-inch 4-40 screws, flatwashers, and lockwashers from the A11 PCB.

7. Separate the A11 PCB from the front panel.

b. Reassembly.

1. Mount the A11 PCB onto the front panel. Use care to insure that the LEDs and pushbuttons are properly aligned with their respective cutouts on the front panel.

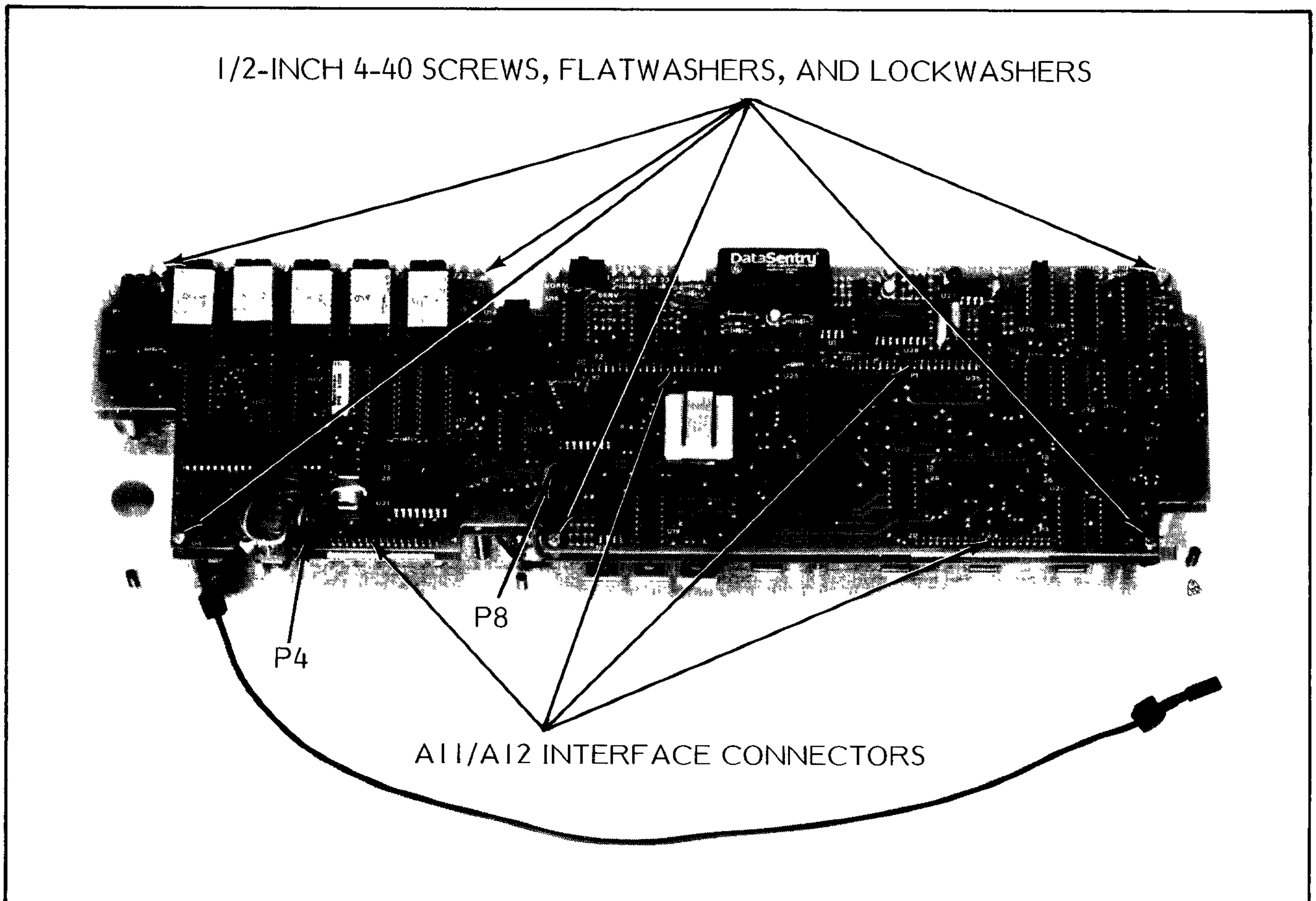


Figure 7-4. 6600 Series Programmable Sweep Generator, Front Panel Assembly

2. Reinstall the eight 7/8-inch 4-40 screws, flatwashers, and lockwashers so that they are snug, but not tight, to the PCB.

3. Check each pushbutton, especially those on the keypad, and insure that none is binding. Reposition the A11 PCB slightly, if required, to prevent pushbutton binding.

4. Tighten the eight A11 retaining screws.

5. Reinstall the knobs on the MANUAL SWEEP, MARKER AMPLITUDE, and EXTERNAL ALC GAIN controls.

NOTE

The knob with the "shoulder" goes on the EXTERNAL ALC GAIN potentiometer.

6. Rejoin the A11 and A12 PCBs, as follows:

   (a) Position the A12 PCB so that the male pins on P3 and P4 mate with their respective female pins on A11J3 and A11J4. Insure that the pins of A12P1 and A12P2 are aligned with their mating pins on A11J1 and A11J2.

   (b) While observing the four connectors, gently press the two PCBs together until the connectors are properly seated.

   (c) Reinstall the six 1/2-inch 4-40 screws, flatwashers, and lockwashers.

7. Reconnect the 5-wire connector to A12P4 (green wire to pin 20); see Figure 7-4.

8. Reconnect the 3-wire connector to A12P8 (brown wire to pin 1); see Figure 7-4.

9. Reinstall the front panel assembly into the basic frame; refer to paragraph 7-3.1.

7-3.3 INCREASE-DECREASE Lever, Switch-Assembly Replacement

The INCREASE-DECREASE lever switch-assembly is not repairable in the field. In the event of an electrical or mechanical failure, the entire switch-assembly must be replaced. To replace this assembly, proceed as follows:

NOTE

The knob on the INCREASE-DECREASE lever is secured to the lever shaft with an epoxy compound. The removal of this knob may cause its destruction. Consequently, when ordering a replacement INCREASE-DECREASE lever switch-assembly, a replacement knob (WILTRON part number 430-106) should be ordered also.

a. Remove the front panel assembly from the basic frame; refer to paragraph 7-3.1.

b. Disassemble the front panel assembly; refer to paragraph 7-3.2.

c. Remove the knob from the INCREASE-DECREASE lever (see NOTE).

d. Remove the two 1/4-inch 4-40 screws, flatwashers, and lockwashers, and remove the assembly from the front panel.

e. Install the new assembly and secure using the 4-40 hardware.

f. Install new knob on lever shaft, and secure it in place using a quick-drying cement (such as a 3-minute epoxy compound).

g. Reassemble the front panel assembly; refer to paragraph 7-3.2.

h. Reinstall the front panel assembly into basic frame; refer to paragraph 7-3.1.

7-3.4 Rear Panel Assembly, Removal and Reinstallation Instructions

a. Removal.

1. Turn off ac power and disconnect the input line voltage.

2. Remove the top and side covers from the sweep generator as follows:

   (a) Remove the 4 corner-brackets from the rear panel of the sweep generator, Figure 7-1.

   (b) Slide the top and side covers to the rear and remove.

WARNING

There are dangerous charged-capacitor voltages present on P1 pins 3 thru 10 when power is removed. Discharge these pins to chassis ground before performing maintenance.

3. Disconnect the Molex connector from A14P1 (Figure 7-5).

4. Remove the six #8 fillister-head, posi-drive screws from the rear panel (Figure 7-1).

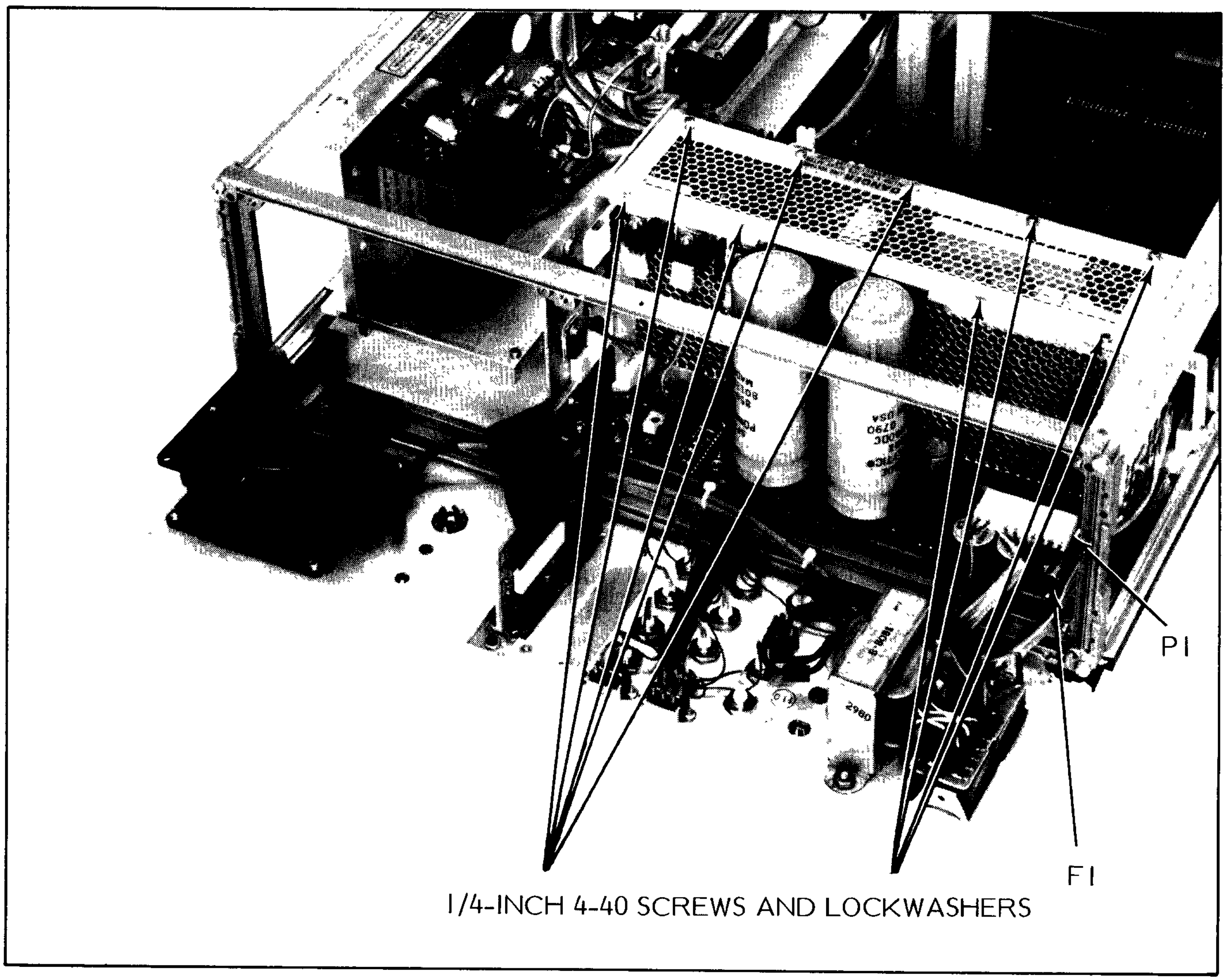


Figure 7-5. 6600 Series Programmable Sweep Generator, Rear Quarter Panels and Assemblies

5. Gently push the rear panel out from the basic frame and lay it back on the work surface. It is not necessary to remove the rear panel assembly completely; all rear panel components are accessible with the panel in this position.

b. Reinstallation. The reinstallation procedure for the rear panel assembly is a reversal of the removal procedure.

7-3.5 A13 Switching Power Supply PCB, Removal and Reinstallation

WARNING

Voltages hazardous to life are present through the A13/A14 Switching Power Supply, even when power is turned off and the ac line cord is removed. Before performing maintenance on this power supply, observe the following precautions:

After ac power is turned off and the line cord is removed, allow 5 minutes for the capacitor voltages to decay.

Avoid touching the terminals on the 5A FB fuse, A14F1, (Figure 7-5) when power is turned on. +165 Vdc is present on these terminals.

a. Removal.

1. Turn off the ac power and disconnect the ac line cord from the Voltage Selector Module.

2. Remove the top cover from the sweep generator, as follows:

   (a) Remove the two top, corner brackets from the rear panel of the sweep generator (Figure 7-1).

   (b) Slide the cover to the rear and remove.

3. Remove the ten 1/4-inch 4-40 screws and lockwashers from the top cover of the A13 card-cage assembly, and remove the cover.

4. Using the ejectors on the ends of the PCB, eject the PCB from the XA13 socket.

b. Reinstallation. The reinstallation instructions are a reversal of the removal instructions.

NOTE

The A13 PCB power supply switching-frequency is in the RF spectrum (50 kHz). To prevent this RF energy from being radiated, insure that the card-cage cover is securely seated and fastened with all ten screws before the ac power is reapplied.

7-4 6600 SERIES PROGRAMMABLE SWEEP GENERATOR OVERALL CIRCUIT DESCRIPTION

The 6600 Series Programmable Sweep Generator is a microprocessor-based instrument that uses a combination of digital and analog circuitry to produce its swept- and CW-frequency outputs. An overall block diagram of the sweep generator is shown in Figure 7-6.

The A12 Microprocessor PCB provides overall control for RF signal generation. As shown in Figure 7-6, the A12 PCB interfaces with the Analog Circuits via the **µP Bus**, and with the front panel controls via the A11 PCB. The A12 PCB is described in paragraph 7-6.1.

The A11 Front Panel PCB provides an interface for all of the front panel pushbuttons, except RESET and SELF TEST. These two pushbuttons are connected directly to the A12, where their activation causes microprocessor interrupt routines to be generated. The A11 PCB is described in paragraph 7-7.1.

The A1 GPIB Interface PCB is only installed for sweep generators containing Option 3. This PCB provides interface between the IEEE 488 Interface Bus (General Purpose

Interface Bus—GPIB) and the sweep generator. The A1 PCB is described in paragraph 7-8.1.

The A2 Ramp Generator PCB is the sweep-generation source when either the TRIGGER-AUTO, -LINE, or -EXT OR SINGLE SWEEP pushbutton is used to select the triggering mode. These three pushbuttons control the A2 sweep ramp via the **µP BUS.** Triggering for the A2 sweep ramp is accomplished via the **µP Bus** for the single sweep mode, via the **EXT TRIGGER IN** line for the external sweep mode, or via the **AC LINE VOLTAGE** input for the line trigger mode. The remaining two input lines, **INTENSITY MARKER** and **EOB,** cause the A2 sweep ramp to dwell momentarily. The **INTENSITY MARKER** line causes the ramp to dwell when an intensity marker is commanded. And the **EOB** line causes the ramp to dwell during an oscillator bandswitch (see NOTE). The A2 PCB output lines include the **RAMP OUT** signal that goes to the A5 PCB and the five signals that go to the rear panel connectors: **BANDSWITCH BLANKING** (+), (-); **RETRACE BLANKING** (+), (-); and **SEQ SYNC.** The A2 PCB is described in paragraph 7-9.1.

NOTE

> As shown in the figure, three YIG oscillators are used to generate a full-band sweep with the Models 6637/38/47/48. The frequency at which the sweep (or CW tuning) goes from a lower- to a higher-frequency oscillator (or from the heterodyne band to the first oscillator band) is known as the bandswitch point. In the 6647/48 there are three bandswitch points, at 2, 8, and 12.4 GHz. In the 6637/38 there are two such points, at 8 and 12.4 GHz.

The A3 Marker Generator PCB generates the F0, M1, and M2 markers. The marker frequency and mode (VIDEO, RF, INTENSITY) data enters A3 via the **µP BUS.** The frequency data is converted to an analog voltage, compared with the **RAMP, 0-10V,** signal, and used to generate the frequency marker. The mode data selects the type of marker to be displayed: either intensity, RF, or video. The **RAMP, 0-10V,** signal is also buffered on A3 and supplied to the rear panel HORIZ OUTPUT connector. The A3 PCB, in addition to generating markers, also contains the logic circuitry associated with the front panel INCREASE-DECREASE lever. The **MODIFY SIGNAL** line provides the input to this logic circuitry. The frequency data generated by this logic circuitry is in the form of an 8-bit digital word. This word is sent to the microprocessor via the **µP Bus.** The A3 PCB is described in paragraph 7-10.1.

The A4 Automatic Level Control PCB is the control arm for the RF-output-signal leveling loop. The input arm for the leveling loop is either the built-in Coupler/Detector that is used for internal leveling, or it is the external coupler and detector (or power meter) that is required for external leveling. The output arm of the leveling loop is the PIN switch atttenuator current-driver circuit (not shown) located on the A6, A7, and A8 YIG Driver PCBs. These current-driver circuits operate the **MOD DRIVER 1, 2,** and **3** lines used to control Mod and PIN switch attenuation. The A4 also performs the following functions:

a. It sets the magnitude of the RF output power, which the user selects using the front panel LEVEL pushbutton.

b. It creates a "dip" in output power at the RF marker frequency.

c. It provides the RF SLOPE correction to the output power signal.

The A4 PCB, in addition to controlling the leveling loop, provides a latch for the **ATTN 1** through **ATTN 4** control bits. These control bits come from the microprocessor and go to the A10 PCB. The A4 PCB is described in paragraph 7-11.1.

The A5 Frequency Instruction PCB generates tuning and bandswitch-control voltages for the A6-A8 YIG Driver PCBs. The bandswitch-control voltage is the **FCEN/VPF** signal, and the tuning voltages are the **F CEN,**

ΔF>50 MHz, and **F CORR** signals. There are three sweep-voltage-producing sources in the sweep generator: The A2 PCB, the front panel MANUAL SWEEP potentiometer, and the Step Frequency DAC (digital-to-analog converter) (paragraph 3-7.2) located on A5. One of these sources, as determined by the microprocessor, is selected on A5 and used to generate the **ΔF>50 MHz** signal. The center frequency, which the user selects using the front panel FREQUENCY RANGE controls, provides the **F CEN** signal. And a correction voltage, which is the sum of the FREQUENCY VERNIER signal from the front panel and the Linearizing ROM signal (see NOTE) from the applicable A6-A8 YIG Driver PCB, provides the **F CORR** signal. The FREQUENCY VERNIER signal enters A5 via the **μP Bus** and the linearizing ROM signal enters via the **FC** (frequency correction) **Bus.** The A5 PCB also supplies a tuning signal, **ΔF≤50 MHz**, for the FM coil in the YIG oscillator; this signal goes to the A10 PCB. The **ΔF≤50 MHz** signal sweeps the YIG oscillator via the FM coil when the sweep width is ≤50 MHz. The A5 PCB is described in paragraph 7-12.1.

NOTE

> Many YIG oscillators, though inherently linear, often have linearity errors due to magnetic saturation effects. To correct for linearity errors, digital data providing up to ±64 MHz of frequency correction may be stored in read only memory (ROM). If required by the installed YIG oscillator, two Linearizing ROMs are mounted on the applicable A6, A7, or A8 YIG Driver PCB.

The A6 Het-YIG Driver, A7, and A8 YIG Driver PCBs provide tuning and bias currents for the Osc 1, 2, and 3 YIG tuning coils. The tuning currents are derived from the three tuning voltages (**F CEN**, **ΔF>50 MHz**, **F CORR**) supplied by the A5 PCB. The oscillator bias currents are generated individually on each A6-A8 PCB. In addition to tuning and bias currents, the A6 PCB also generates a tracking filter voltage, which is supplied to the A10 PCB. This voltage indirectly provides tuning for the YIG tracking filter that is built into the Osc 1 YIG module. With the exception of the MOD DRIVER signals previously described, the other A6-A8 outputs are control lines. The **SNB** and **SNR** lines are select next band and select next ROM lines, respectively. When the presently-selected oscillator band has reached its upper-most frequency, the **SNB** line selects the next oscillator band and the **SNR** line enables this next-oscillator-band's linearizing ROM. The **HET YIG SEL** and **YIG 1, 2,** and **3 FM COIL SEL** lines are supplied to the A10 PCB. A detailed overall description of the A6-A8 PCBs is given in paragraph 7-12.2. The A6 PCB is described in paragraph 7-12.3 and the A7 and A8 PCBs are described in paragraph 7-12.4.

The A10 FM/Attenuator PCB provides a tuning current for both the YIG Osc 1, 2, and 3 FM (frequency modulation) coils and the Osc 1 YIG tracking filter. The tracking filter tuning current is derived from the **TRACK FILTER 1** voltage generated on the A6 PCB. The FM coil tuning current may be derived from either of two sources: an external FM signal from the rear panel via the EXT FM ∅LOCK INPUT connector or a sweep width voltage from the A5 PCB via the **ΔF≤50 MHz** signal line. In addition to the FM and tracking filter currents, the A10 generates an end-of-band pulse (**EOB**) whenever a bandswitch occurs. The **HET YIG SEL** (6647/48) and **YIG 1, 2,** and **3 FM COIL SEL** lines from the A6-A8 PCBs provide the input for the **EOB** circuit. The A10 PCB is described in paragraph 7-13.1.

The RF Components Deck is a subassembly; it contains all of the sweep generator RF components. This subassembly is described in paragraph 7-14.

The A14 Motherboard PCB provides an interconnecting plane for the A1 through A10 PCBs. It also provides interconnection via connectors between the A1-A10 PCBs and the A12 PCB, the rear panel connectors, and the RF Components deck components. The A14 PCB also contains diagnostic (self-test) and PIN Switch port drive and attenuator

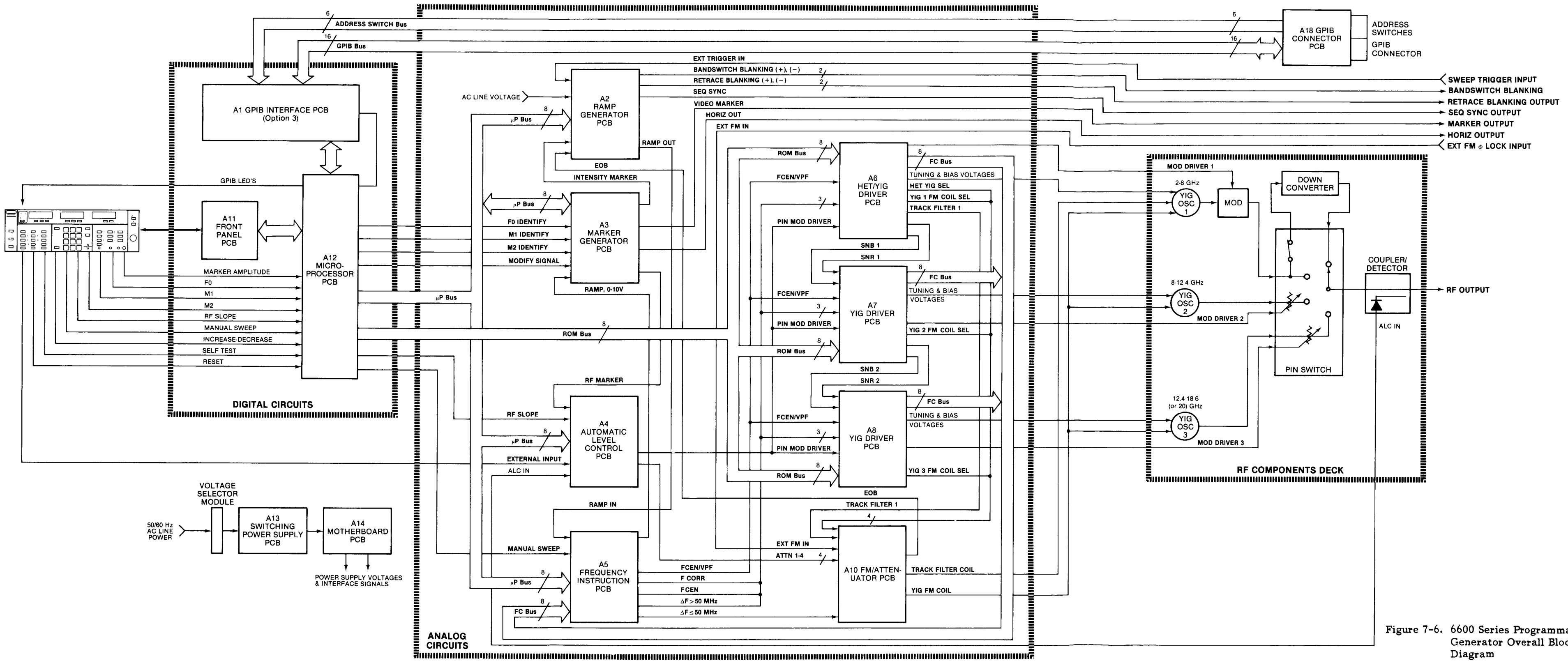


Figure 7-6. 6600 Series Programmable Sweep Generator Overall Block Diagram

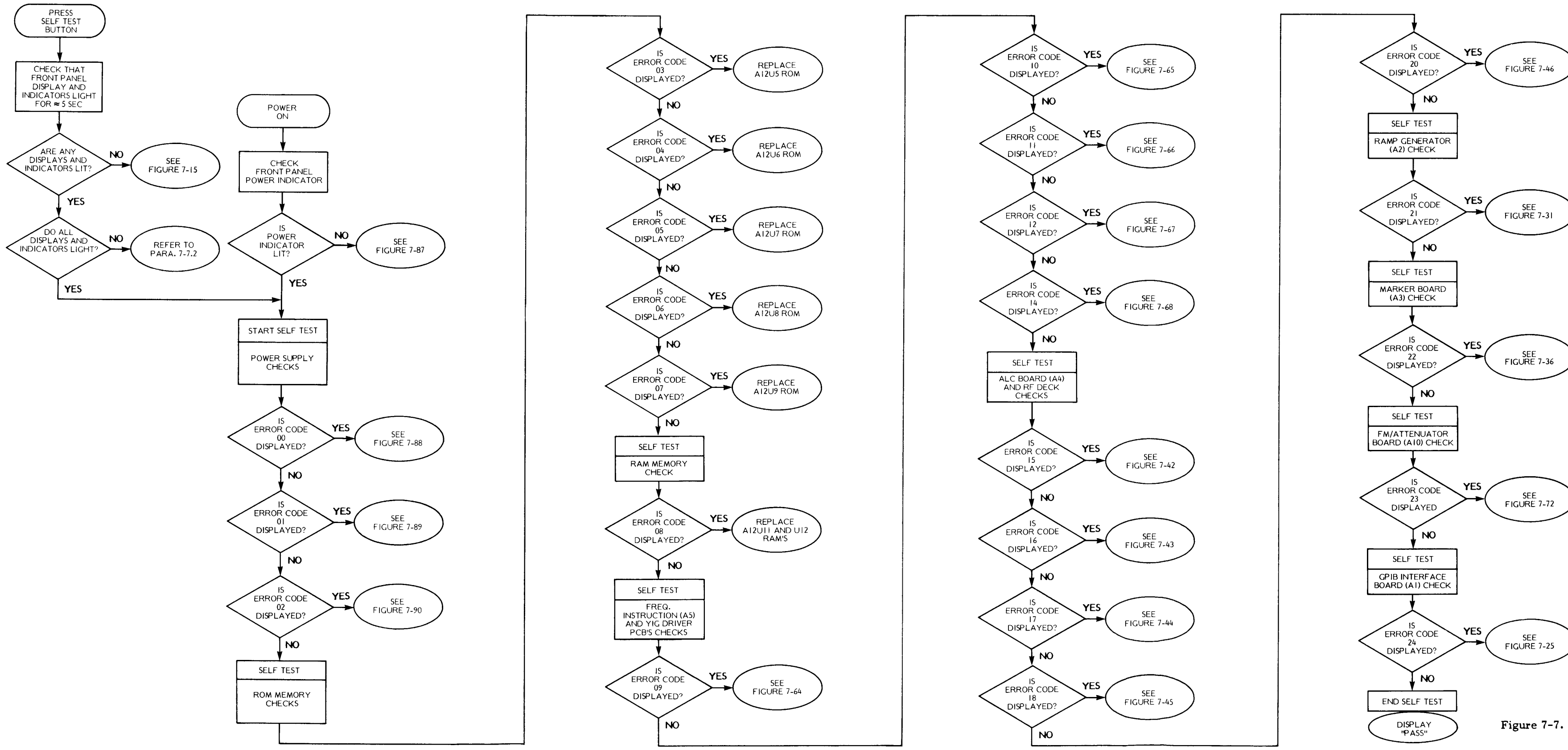


Figure 7-7. 6600 Series Overall Troubleshooting Flowchart

circuitry; it also contains part of the switching power supply circuitry. The A14 PCB is described in paragraph 7-15.2.

The A13 Switching Power Supply PCB, in conjunction with the power supply circuits on the A14 PCB, provides power supply voltages for the sweep generator circuits. The A13/A14 Switching Power Supply is described in paragraph 7-15.1.

The A18 GPIB Interface Connector PCB provides a connecting plane for the Option 3 rear panel GPIB connector and address switches. This PCB is installed only on sweep generators containing Option 3. The A18 PCB is described in paragraph 7-16.

7-5 6600 SERIES PROGRAMMABLE SWEEP GENERATOR OVERALL TROUBLESHOOTING

Troubleshooting for the 6600 Series Sweep Generators is facilitated by the self-test error codes described in paragraph 3-4. When used with the supplemental flowcharts and block diagrams provided in this section, these error codes can be used to isolate most malfunctions to the defective functional or integrated circuit. A flowchart for troubleshooting the self-test error codes is provided in Figure 7-7 (facing page).

7-6 A12 MICROPROCESSOR PCB

7-6.1 A12 Microprocessor PCB Circuit Description

The A12 Microprocessor PCB controls the operation of the sweep generator. It also provides, via the A11 Front Panel PCB, the interface between the front panel pushbuttons and the analog sweep- and microwave-generating circuitry. To provide this control, the A12 PCB contains an 8085 Microprocessor integrated circuit (IC), an 8279 Keyboard/Display Interface IC, 10k bytes of read-only memory (ROM), and 256 bytes of read/write memory (RAM). A block diagram of the A12 PCB circuitry is provided in Figure 7-8. A diagram showing the distribution of control-group data between the A12 PCB and the A2-A5 and A14 PCBs is provided in Figure 7-9; descriptions of these data are provided in Appendix III. A flowchart showing the microprocessor's ac power-on operational program is provided in Figure 7-10. A parts locator diagram for the A12 PCB is provided in Figure 7-11. And the A12 PCB schematics (5 sheets) are provided in Figure 7-12.

The 8279 IC (U25) (Figure 7-8) interfaces the microprocessor with the front panel pushbuttons and numeric displays. This IC, via its scan lines (the **SL0-SL3&LCAD Bus**), causes the front panel pushbuttons and numeric-display digits to be continually scanned. When the user selects a pushbutton, an 8-bit digitally-coded word (keycode) representing that pushbutton is sent over the **COL1-COL8 Bus** to the keyboard controller (8279), and eventually to the microprocessor. Conversely, when the microprocessor selects a numeric display for update, a likewise-coded word representing the display segment is sent over the **NA0-NA3/NB0-NB3 Bus** to one of the three displays.

The Latch (U31) and Flash Logic (U34, U35) circuits interface the microprocessor with the EXTERNAL ALC GAIN CAL (ALC CAL), SWEEPING, RF OFF, and UNLEVELED (flashing) front panel LEDs. The interface with the other (non-flashing) LEDs is via the data bus and six latches on the A11 PCB.

The Bidirectional Buffer #2 circuit (U13) interfaces the microprocessor with analog PCBs A2-A5, ROM Bus latch A14U6, and diagnostic (self-test) latches A14U7, U8, and U10 — all on the motherboard. Also, if Option 3 is installed, U13 interfaces the microprocessor with the A1 GPIB Interface PCB.

The Control Signal Input Ports (U29, U30) are latch/buffers that allow control signal data from the A2, A3, and A4 analog PCBs; the A1 GPIB Interface PCB (Option 3 only); and the A11 Front Panel PCB to be input into the microprocessor.

The Bidirectional Buffer #1 circuit (U14) buffers the input/output interface circuitry from the microprocessor "kernel," the control element on the A12 PCB. This kernel consists of:

a. 8085 Microprocessor (U2). U2 is a complete central-processing unit (CPU); it contains all of the necessary registers and the arithmetic logic unit (ALU) and control circuitry.

b. Address Decoders (U3, U4). U3 and U4 decode the A8-A14 and A0-A7 address lines, providing addresses for the memory circuits.

c. 5101 RAM (U11, U12), RAM Buffer (U10), and RAM Battery (B1, U1). The RAM circuits store the data input via the front panel pushbuttons. The RAM Battery provides operating power for the read/write memory when the ac power is turned off, making this memory non-volatile.

d. 2716 ROM (U5-U9). The ROM circuits contain both the microprocessor ac power-on operational program (Figure 7-10) and the reset (default) parameter data (paragraph 3-7.1).

e. **Free-Run Socket (J9). J9 provides for testing of the microprocessor. The removal of J9 forces a series of no-operation (NOP) instructions on the microprocessor, thus causing it to free run.**

f. Port Decoders (U18-U23). The port decoders are divided between input and output ports. U19-U21 are output port decoders; U22 and U23 are input port decoders; and U18 is a port-decoder-enable circuit.

U19-U21 decode the microprocessor output-port data and select one of 24 output ports. The selected port then receives the data that the microprocessor has concurrently sent over the data bus. The output-port-select lines are **SP0** thru **SP23**. The **SP0-SP15** lines go to the analog PCB ports, located on the individual A2-A5 and A14 PCBs (Figure 7-9). **SP16-SP21** go to the front-panel non-flashing LED ports, A11U1 thru A11U6. The **SP22** line goes to the front-panel flashing LED port, A12U31. And the **SP23** line goes to the GPIB Interface PCB µP-data input port, A1U22 (Option 3 only).

U22 and U23 decode the microprocessor input-port data and select one of the eight latch/buffer circuit input ports. When selected, the port then allows the data that is concurrently on the A14 **µP Data Bus** to be input into the microprocessor. The input port data is divided into four types: diagnostics (self-test) data, GPIB data (Option 3 only), INCREASE-DECREASE-lever-frequency data, and control signal data. Input port select lines **SX1, SX2,** and **SX7** select the diagnostics data; **SX3** selects the GPIB data; **SX4** and **SX29** select the INCREASE-DECREASE lever frequency data; and **SX24** and **SX25** select the control signal data.

g. SERVICE-NORMAL Switch **(S1)**. In the SERVICE position, S1 interrupts the microprocessor and causes it to run a stimulus routine for signature-analysis testing.

The A14 Motherboard PCB components that are functionally part of the microprocessor circuitry consist of the Linearizer ROM Latch, A14U6, and the Diagnostic (Self Test) Latches A14U7, U8, and U10.

The Linearizer-ROM Latch, U6, supplies address data to the linearizer ROMs located on the A6, A7, and A8 YIG Driver PCBs. When clocked by SP5, U5 latches the microprocessor-supplied ROM address data from its input to its output circuit. The output-circuit data is supplied to each of the YIG driver PCBs, via the ROM bus.

The Diagnostic (Self Test) and Misc'l Signal Buffers, U7, U8, and U10, are respectively enabled by the **SX1, SX2,** and **SX7** input-port select lines from the microprocessor. When a buffer is enabled, the data latched in its input circuit is allowed to pass to its output circuit. The input lines to the diagnostic buffers are as follows:

7-6.1 cont.

h. U7 Buffer:

1. **L YIG 1 FM COIL SELECT,** from A6 PCB.
2. **L YIG 2 FM COIL SELECT,** from A7 PCB.
3. **L YIG 3 FM COIL SELECT,** from A8 PCB.
4. **L YIG 4 FM COIL SELECT** (not used).
5. **H SNR 1,** from A6 PCB.
6. **H SNR 2,** from A7 PCB.
7. **H SNR 3,** from A8 PCB.
8. **H SNR 4** (not used).

i. U8 Buffer:

1. **H DWELL,** from A2 PCB.
2. **L HET YIG SEL,** from A6 PCB.
3. **H FM DIAG,** from A10 PCB.

j. U10 Buffer:

1. **L OR,** from A14U5 (switching power supply).
2. **L HL,** from A14U5 (switching power supply).
3. **L LL,** from A14U5 (switching power supply).
4. **GPIB IN,** from A1 PCB (Option 3).
5. **L DWELL DETECTED,** from A2 PCB.
6. **HORIZ OUTPUT DURING CW,** from XA16 connector.

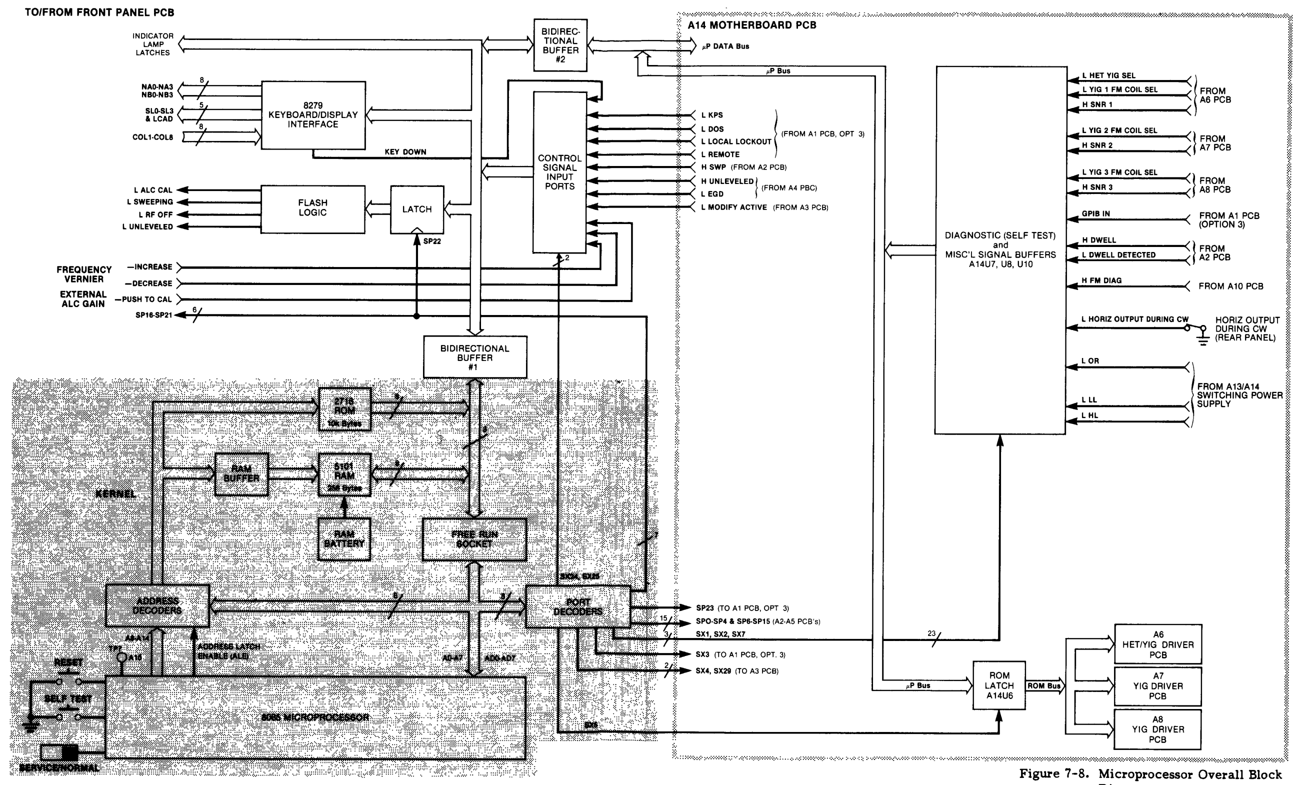


Figure 7-8. Microprocessor Overall Block Diagram

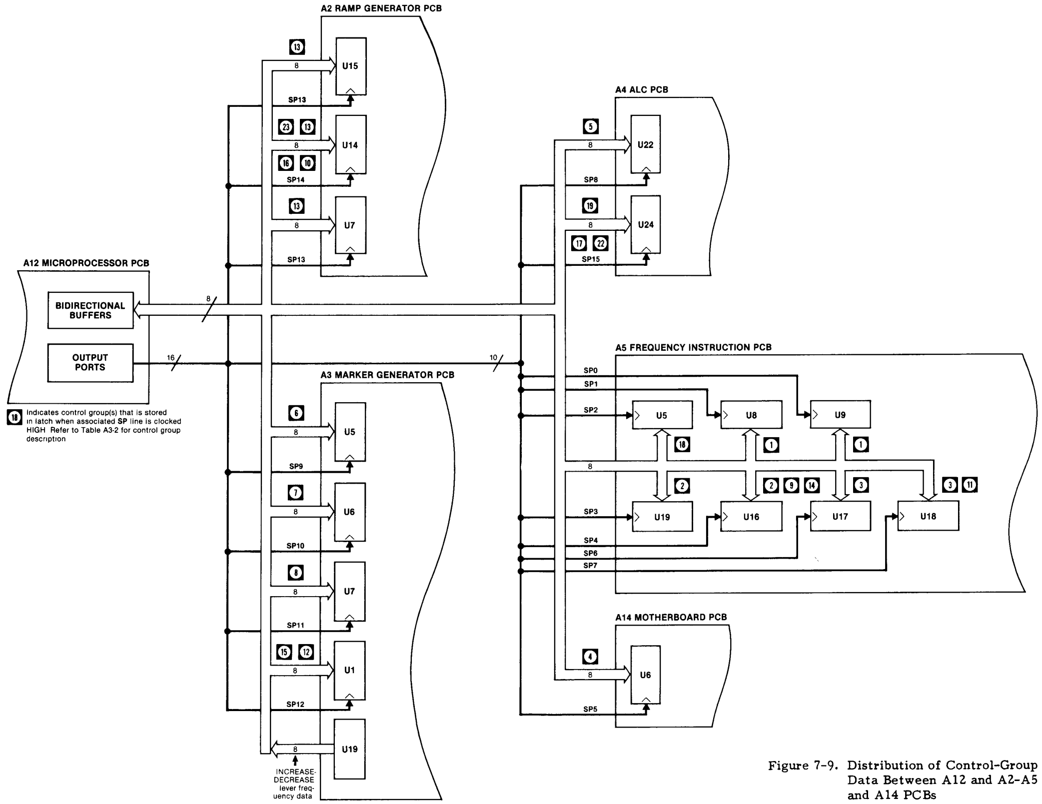


Figure 7-9. Distribution of Control-Group Data Between A12 and A2-A5 and A14 PCBs

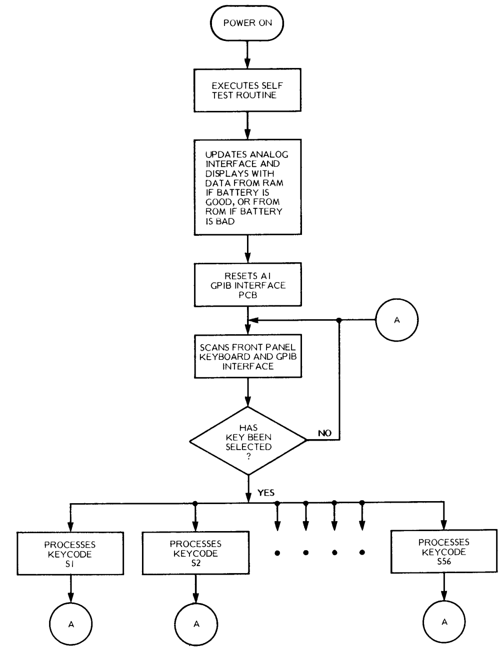


Figure 7-10. A12 Microprocessor PCB AC Power-On Operational Flowchart

Figure 7-9.

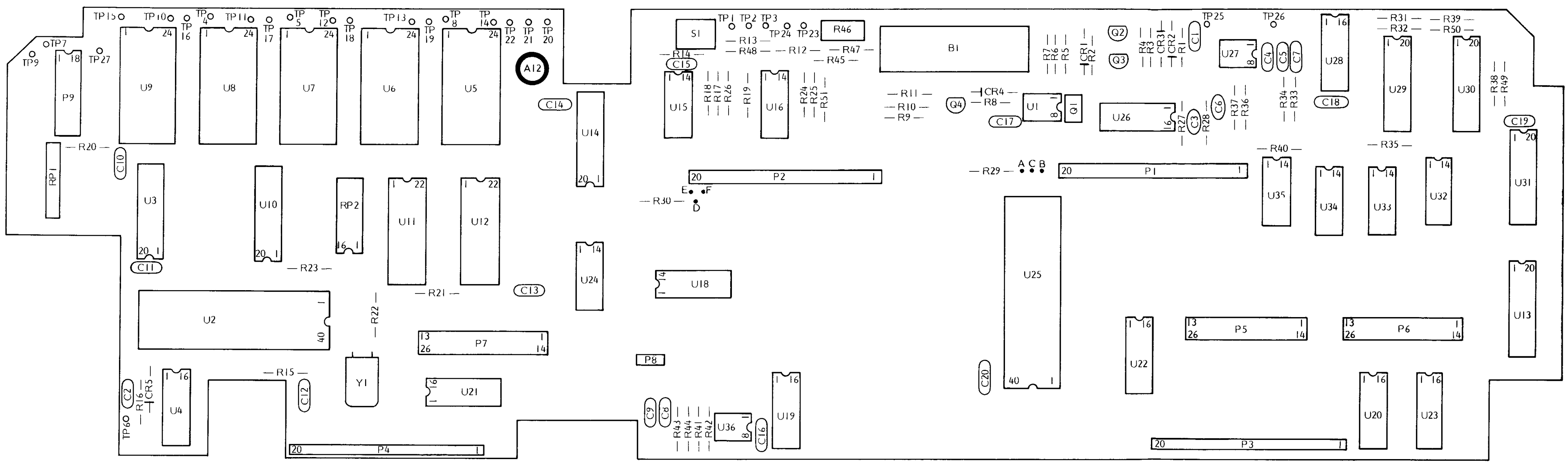
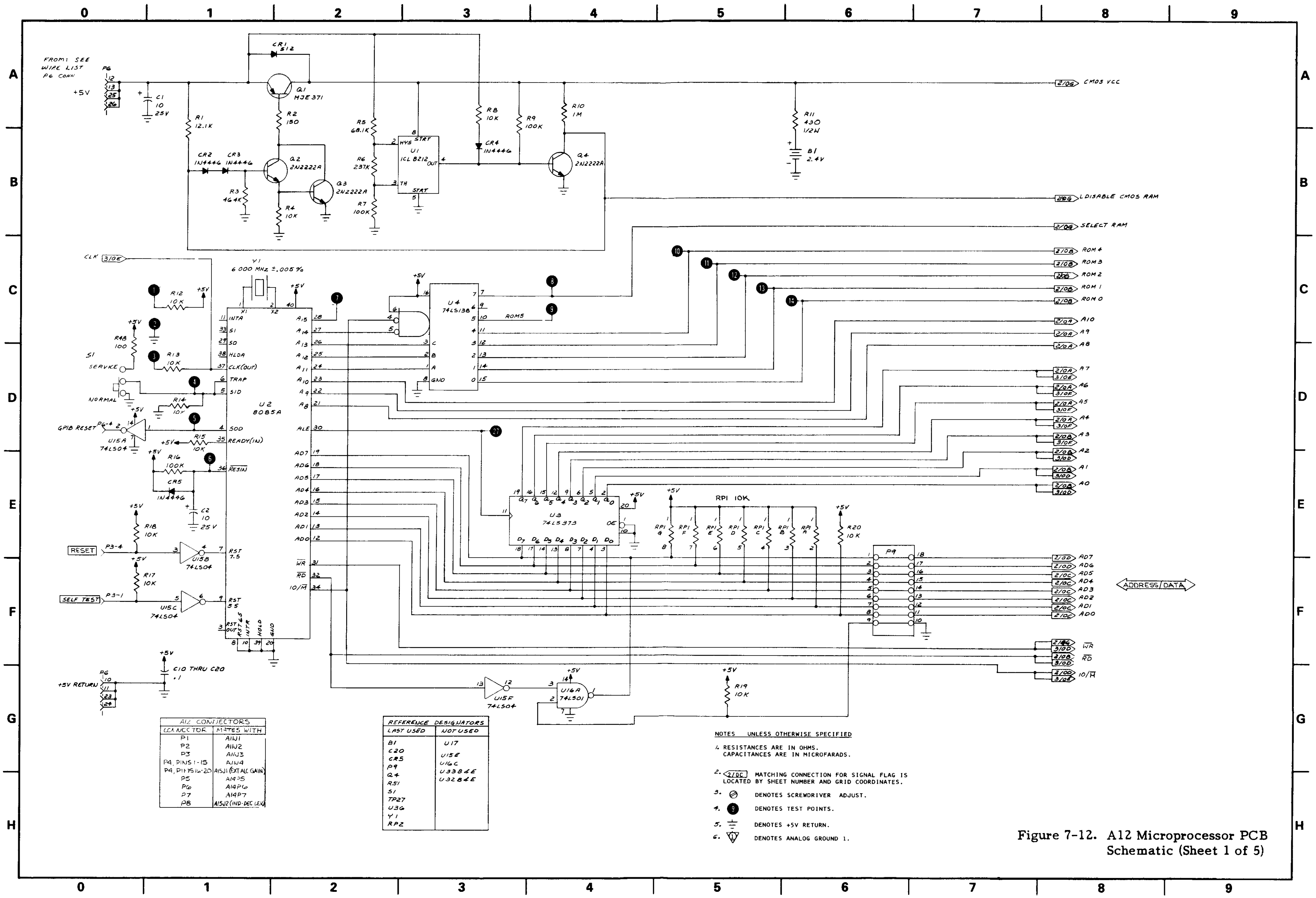


Figure 7-11. A12 Microprocessor PCB Parts Locator Diagram



A12 CONNECTORS	
CONNECTOR	MATES WITH
P1	A1J1
P2	A1J2
P3	A1J3
P4, PINS 1-15	A1J4
P4, PINS 16-20	A15J1 (EXT ALC GAIN)
P5	A1P5
P6	A1P6
P7	A1P7
P8	A15J2 (IND-DEC LEX)

REFERENCE DESIGNATORS	
LAST USED	NOT USED
B1	U17
C20	U15E
CR5	U16C
P9	U33B&E
Q4	U32B&E
R51	
S1	
TP27	
U36	
Y1	
RP2	

NOTES UNLESS OTHERWISE SPECIFIED

1. RESISTANCES ARE IN OHMS. CAPACITANCES ARE IN MICROFARADS.
2. 2/0C MATCHING CONNECTION FOR SIGNAL FLAG IS LOCATED BY SHEET NUMBER AND GRID COORDINATES.
3. ⊘ DENOTES SCREWDRIVER ADJUST.
4. ❾ DENOTES TEST POINTS.
5. ⏚ DENOTES +5V RETURN.
6. ▽ DENOTES ANALOG GROUND 1.

Figure 7-12. A12 Microprocessor PCB Schematic (Sheet 1 of 5)

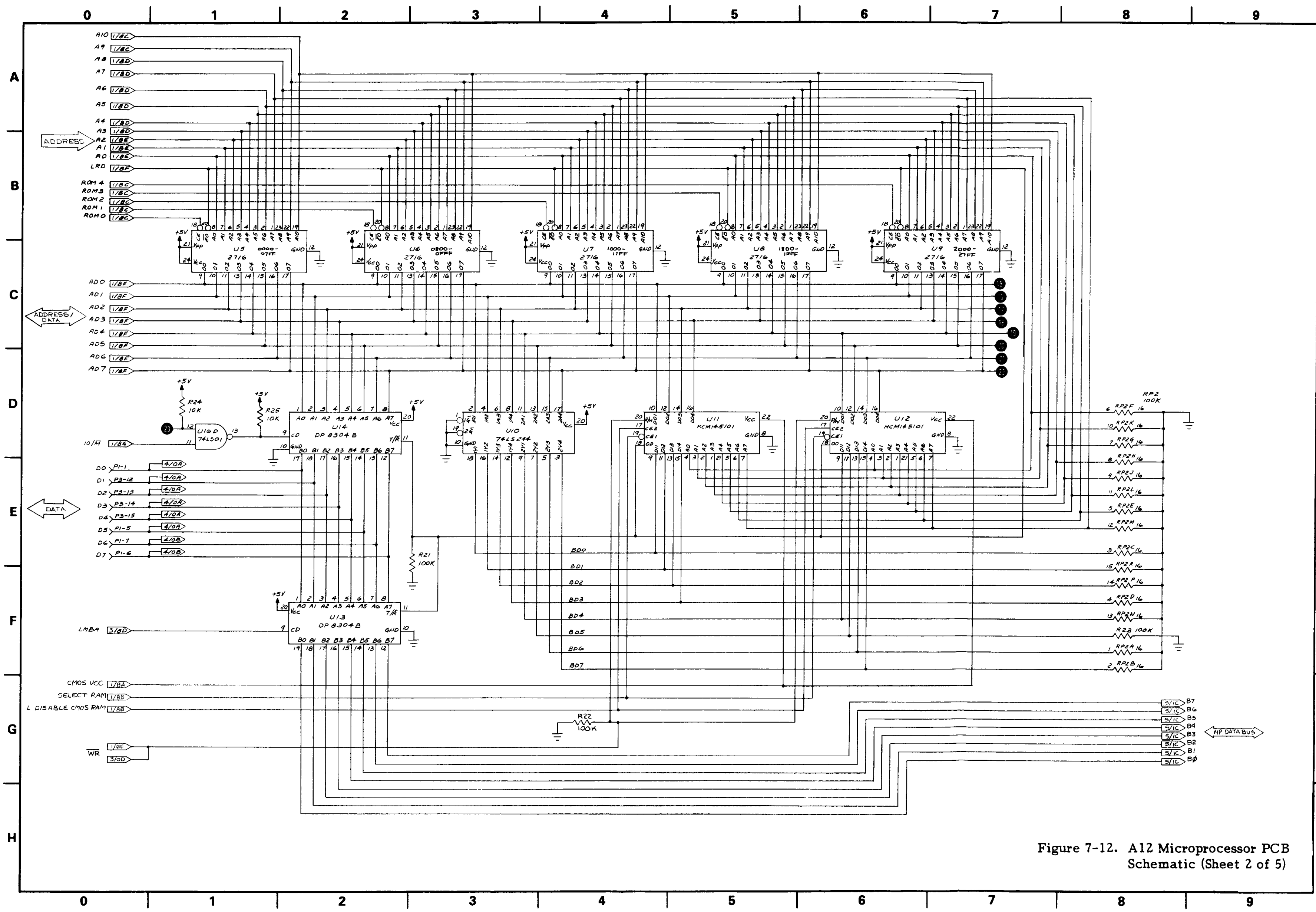


Figure 7-12. A12 Microprocessor PCB Schematic (Sheet 2 of 5)

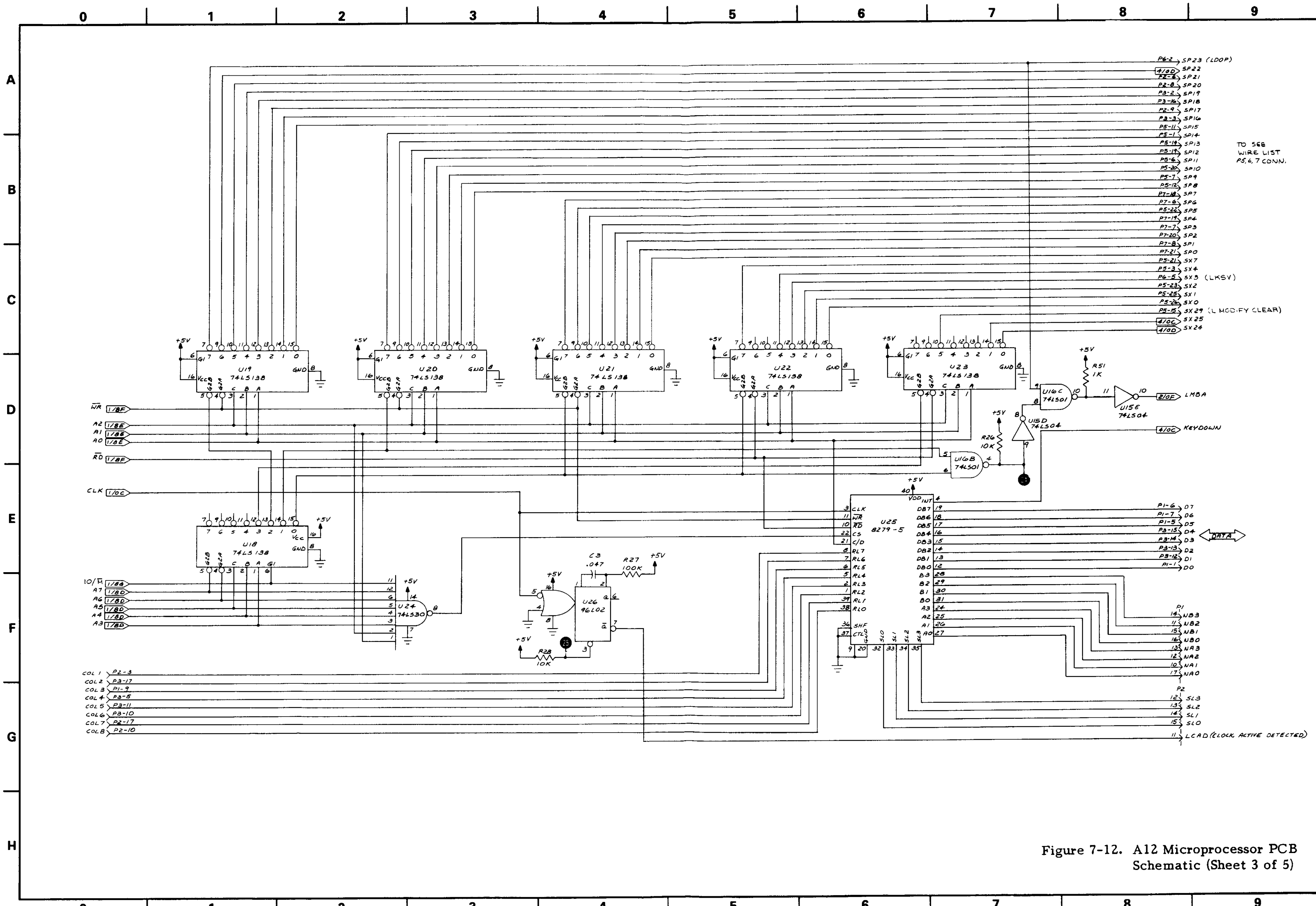


Figure 7-12. A12 Microprocessor PCB Schematic (Sheet 3 of 5)

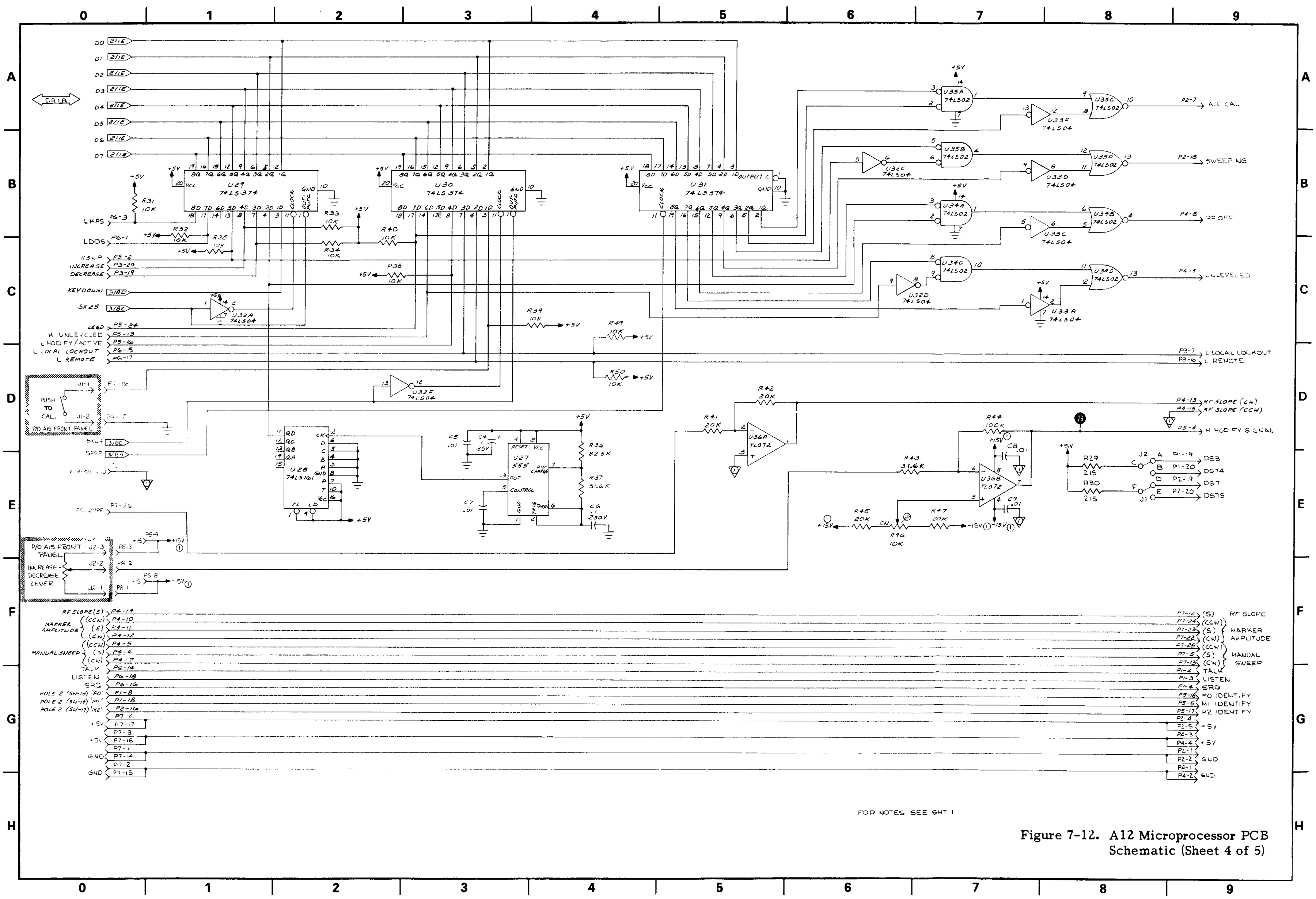


Figure 7-12. A12 Microprocessor PCB Schematic (Sheet 4 of 5)

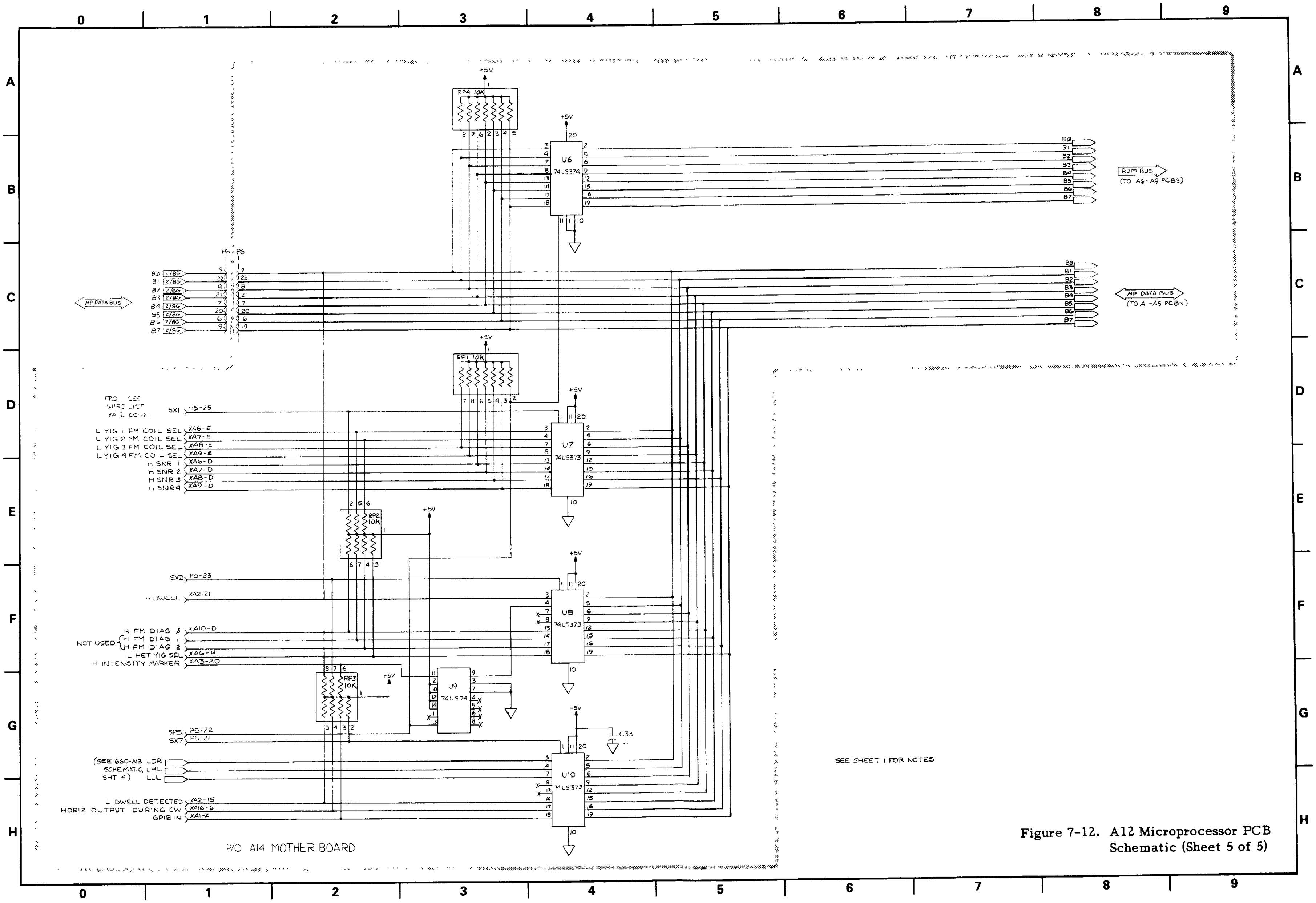


Figure 7-12. A12 Microprocessor PCB Schematic (Sheet 5 of 5)

7-6.2 A12 Microprocessor PCB Troubleshooting Information and Data

There is no error code for the A12 Microprocessor PCB. Read-only-memory (ROM) or read/write memory (RAM) malfunctions occurring in the microprocessor kernel (Figure 7-8) will cause the respective ROM's or RAM's error code to be displayed. Other malfunctions occurring within the kernel will probably result in the sweep generator's not turning on. And malfunctions occurring outside the kernel will probably result in the display of one or more analog circuit error codes. The test equipment setup for troubleshooting the A12 PCB is provided in Figure 7-13; the troubleshooting flowchart is provided in Figure 7-15.

Signature analysis is the recommended method for troubleshooting A12 circuits. In addition to a free-run mode (explained in HP Application Note 222-2), the A12 PCB also has a service mode. In this mode, routines stored in ROM U5 provide two methods for isolating to faulty components. The first uses a "loop-on-fail" technique (Figure 7-14) that allows the signature analyzer to quickly isolate to a malfunctioning RAM or ROM circuit. In this method the signature analyzer will display one of seven characteristic (Vcc) signatures, depending on which loop is being executed. If no defaults are found, a specific signature is displayed. A fault in the RAM provides a different signature. And a fault in the ROM provides one of five different signatures, depending upon which chip (U5-U9) has the fault.

The second service-mode method, a routine which writes to the output ports and 8279 Keyboard/Display Interface IC, provides for signature analysis of these components. Thus, signature analysis can be used to verify whether a selected analog-PCB-mounted output port is being enabled. It can also be used to test whether the 8279 will respond to selected front panel pushbuttons. These tests are contained in Tables 7-4 and 7-5 respectively. Note that the Table 7-4 signatures are dependent on the software version contained in ROM. The software-version number (e.g. 1.5, 1.6, 1.7, etc.) momentarily appears on a front panel display at the beginning of self test. It also appears on a label affixed to ROMs U5-U9.

For free-run signature analysis, two tables of signatures are provided. Tables 7-2 and 7-3 respectively provide signatures for the microprocessor's read and write spaces. Both of these tables provide test and signature analyzer setup conditions. When these conditions are met, a characteristic (Vcc) signature will be displayed; the microprocessor circuit may then be accurately tested.

In addition to signatures, the 5004A Signature Analyzer data probe may be used like a logic probe. When a circuit node is touched, the probe tip will either flash, light steadily, or not be lit. A steadily-lit probe indicates a logic 1 or Vcc. An unlit probe indicates a logic 0 or ground. And a flashing probe usually indicates pulses; however, it can also indicate noise. A noise indication sometimes occurs when the probe is touched to an open node, or when it is touched to a tri-state-buffer node where the buffer is in its off state. When testing such nodes, the 5004A will read the Vcc signature when its RESET button is pressed. To help minimize probe-noise pickup, ground the probe at the same point the test pod is grounded.

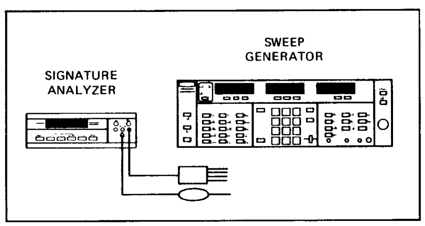


Figure 7-13. Test Setup for Troubleshooting A12 PCB

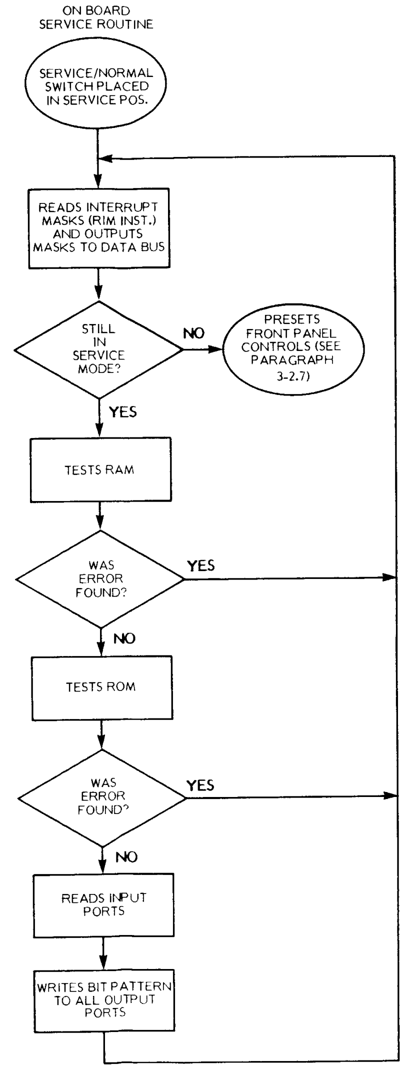


Figure 7-14. A12 PCB On-Board Service Routine

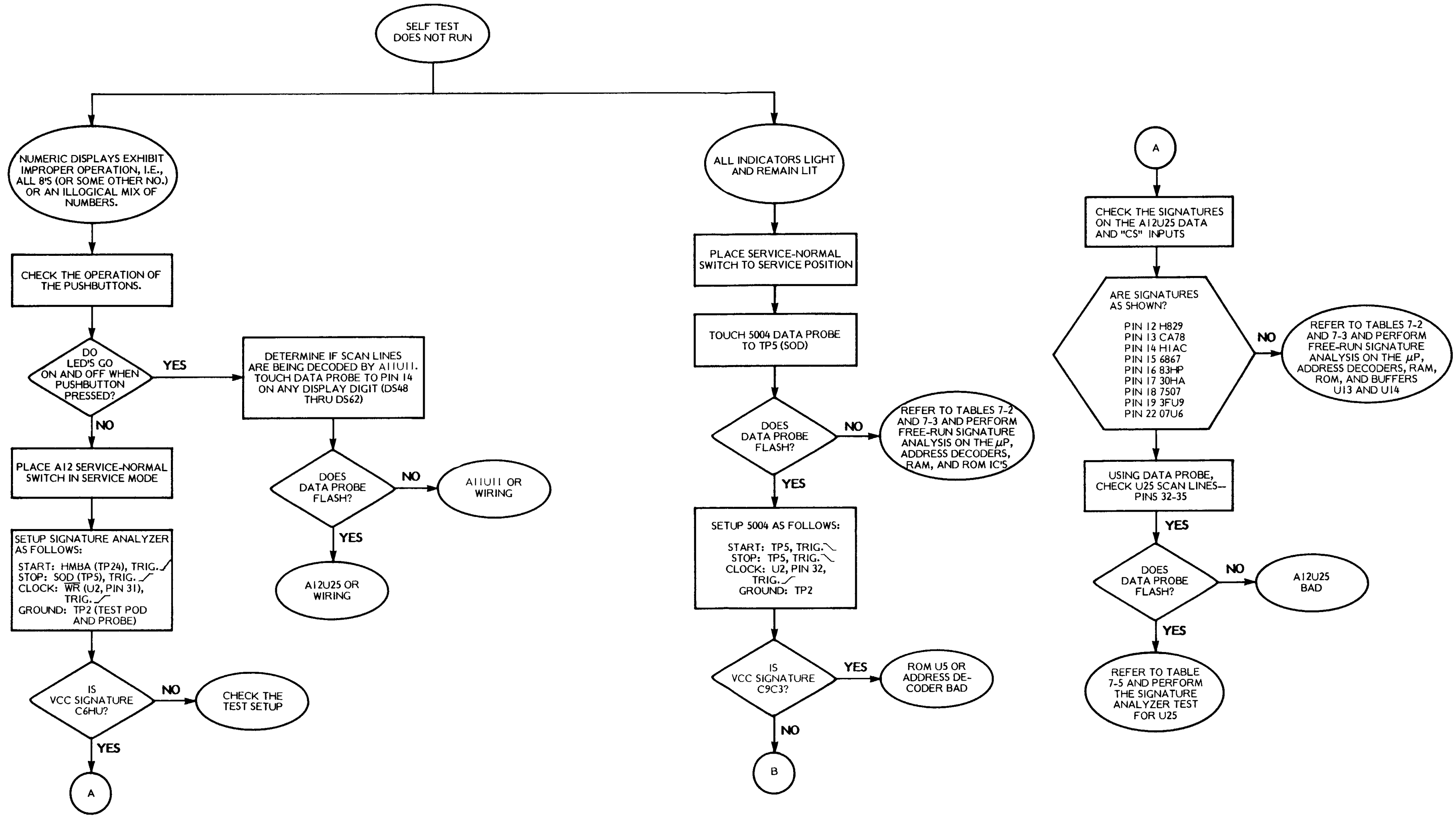


Figure 7-15. A12 PCB Troubleshooting Flowchart (Sheet 1)

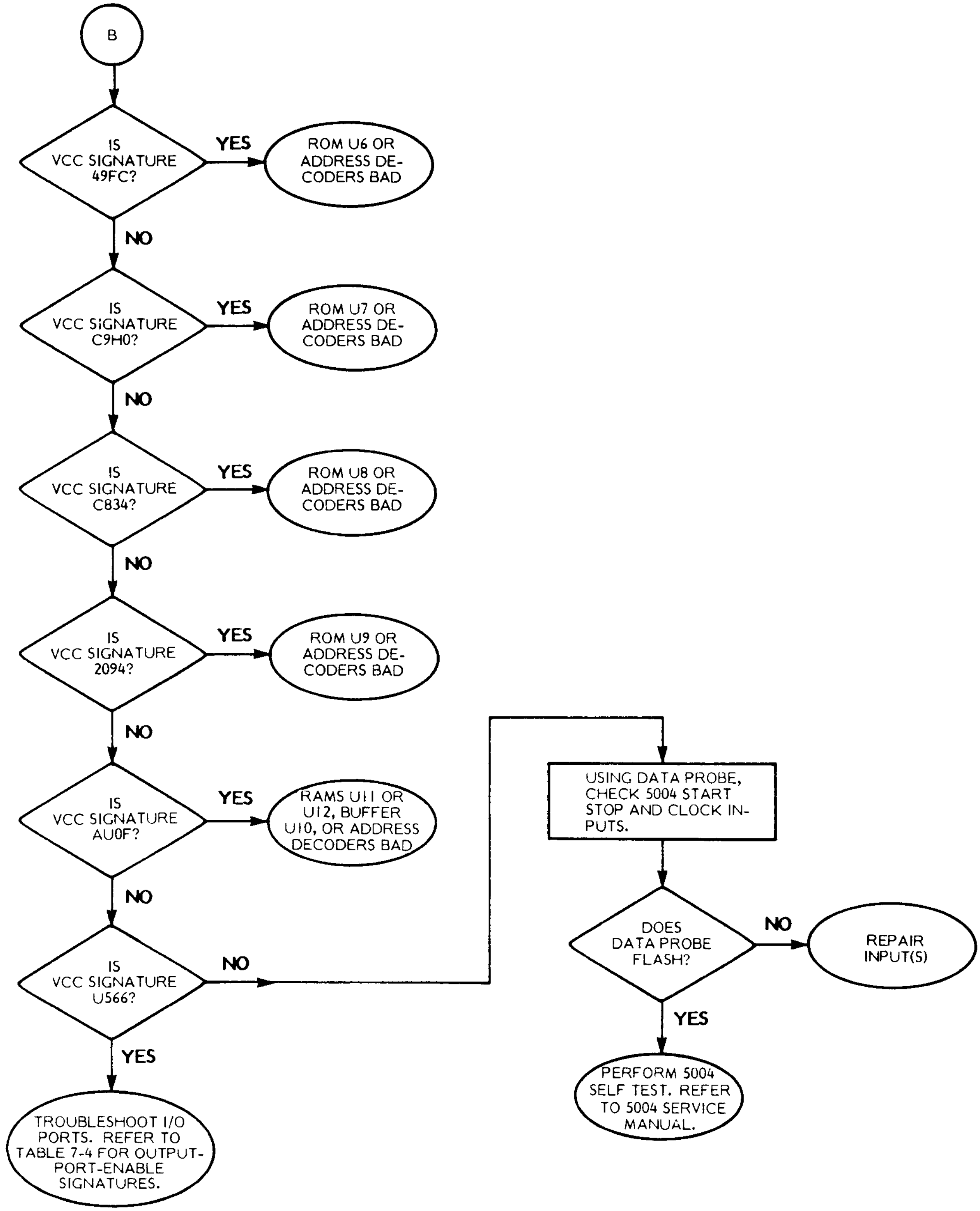


Figure 7-15. A12 PCB Troubleshooting Flowchart (Sheet 2)

Table 7-2. A12 PCB Free-run Mode Signatures – Read Space Test

GENERAL:

Test Conditions: TEST-NORMAL Switch in NORMAL.
Free-run jumper J9 removed.

Signature Analyzer Setup:

START: Bit A15 (TP7), Trigger ╲ (Button In)

STOP: Bit A15 (TP7), Trigger ╱ (Button Out)

CLOCK: $\overline{RD}$ (U2, Pin 32), Trigger ╱ (Button Out)

GROUND: TP2 (Test Pod and Probe)

Vcc Signature: 755U

NOTES

[1] Test probe flashes.
[2] Signature may be unstable.
[3] May have to press RESET on probe.

IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE
U1	1	755U	U2	32	0000[1]	U4	10	2F25	U6	24	755U	U9	5	0772
	2	755U		33	755U		11	8UH9					6	7050
	3	755U		34	0000		12	340A	U7	1	A3C1		7	C113
	4	0000		35	755U		13	P352		2	7211		8	H335
	5	0000		36	755U		14	U1U2		3	AA08		12	0000
	6	0000		37	755U[1]		15	4CP2		4	C4C3		18	8UH9
	7	0000		38	0000		16	755U		5	0772		19	HH86
	8	755U		39	0000					6	7050		20	0000
				40	755U	U5	1	A3C1		7	C113		21	755U
U2	1	0000[1]					2	7211		8	H335		22	577A
	2	755U[1]	U3	1	0000		3	AA08		12	0000		23	7707
	3	0000		2	H335		4	C4C3		18	P352		24	755U
	4	0000		3	755U[1]		5	0772		19	HH86			
	5	0000		4	755U[1]		6	7050		20	0000[1]	U18	1	0772
	6	0000		5	C113		7	C113		21	755U		2	C4C3
	7	0000		6	7050		8	H335		22	577A		3	AA08
	8	0000		7	755U[1]		12	0000		23	7707		4	7211
	9	0000		8	755U[1]		18	4CP2		24	755U		5	A3C1
	10	0000		9	0772		19	HH86					6	0000
	11	755U		10	0000		20	0000[1]	U8	1	A3C1		7	755U
	12	755U[1]		11	0000[1]		21	755U		2	7211		8	0000
	13	755U[1]		12	C4C3		22	577A		3	AA08		9	755U
	14	755U[1]		13	755U[1]		23	7707		4	C4C3		10	755U
	15	755U[1]		14	755U[1]		24	755U		5	0772		11	755U
	16	755U[1]		15	AA08					6	7050		12	755U
	17	755U[1]		16	7211	U6	1	A3C1		7	C113		13	755U
	18	755U[1]		17	755U[1]		2	7211		8	H335		14	755U
	19	0000[1]		18	0000[1]		3	AA08		12	0000			
	20	0000		19	A3C1		4	C4C3		18	340A	U19	1	H335
	21	7707		20	755U		5	0772		19	HH86		2	C113
	22	577A					6	7050		20	0000[1]		3	7050
	23	HH86	U4	1	89F1		7	C113		21	755U		4	755U
	24	89F1		2	AC99		8	H335		22	577A		5	755U
	25	AC99		3	PCF3		12	0000		23	7707		6	755U
	26	PCF3		4	1180		18	U1U2		24	755U		7	755U
	27	1180		5	0000		19	HH86					8	0000
	28	0000[1]		6	755U		20	0000[1]	U9	1	A3C1		9	755U
	29	755U		7	6F7P		21	755U		2	7211		10	755U
	30	0000[1]		8	0000		22	577A		3	AA08			
	31	755U		9	F615		23	7707		4	C4C3			

Table 7-3. A12 PCB Free-run-Mode Signatures – Address Space Test

GENERAL:

Test Conditions: SERVICE-NORMAL switch is NORMAL.
Free-run jumper J9 removed.

Signature Analyzer Setup:

START: Bit A15 (TP7), Trigger ‾_ (Button In)

STOP: Bit A15 (TP7), Trigger _/‾ (Button Out)

CLOCK: ALE (TP27), Trigger ‾_ (Button In)

GROUND: TP2 (Test Pod and Probe)

Vcc Signature: 755U

NOTE

[1] Test probe flashes.
[2] Signature may be unstable.
[3] May have to press RESET on probe.

IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE
U1	1	755U	U2	28	0000[1]	U4	1	89F1	U6	1	A3C1	U8	1	A3C1
	2	755U		29	755U		2	AC99		2	7211		2	7211
	3	755U		30	755U		3	PCF3		3	AA08		3	AA08
	4	0000		31	755U		4	1180		4	C4C3		4	C4C3
	5	0000		32	755U[1]		5	0000		5	0772		5	0772
	6	755U[3]		33	755U		6	755U		6	7050		6	7050
	7	755U		34	0000		7	6F7P		7	C113		7	C113
	8	755U		35	755U		8	0000		8	H335		8	H335
				36	755U		9	F615		12	0000		12	0000
U2	1	0000[1]		37	755U[1]		10	2F25		18	U1U2		18	340A
	2	0000[1]		38	0000		11	8UH9		19	HH86		19	HH86
	3	0000		39	0000		12	340A		20	755U[1]		20	755U[1]
	4	0000		40	755U		13	P352		21	755U		21	755U
	5	755U					14	U1U2		22	577A		22	577A
	6	755U	U3	1	0000		15	4CP2		23	7707		23	7707
	7	0000		2	H335		16	755U		24	755U		24	755U
	8	0000		3	H335									
	9	0000		4	C113	U5	1	A3C1	U7	1	A3C1	U9	1	A3C1
	10	0000		5	C113		2	7211		2	7211		2	7211
	11	755U		6	7050		3	AA08		3	AA08		3	AA08
	12	H335		7	7050		4	C4C3		4	C4C3		4	C4C3
	13	C113		8	0772		5	0772		5	0772		5	0772
	14	7050		9	0772		6	7050		6	7050		6	7050
	15	0772		10	0000		7	C113		7	C113		7	C113
	16	C4C3		11	755U[1]		8	H335		8	H335		8	H335
	17	AA08		12	C4C3		12	0000		12	0000		12	0000
	18	7211		13	C4C3		18	4CP2		18	P352		19	HH86
	19	A3C1		14	AA08		19	HH86		19	HH86		20	755U[1]
	20	0000		15	AA08		20	755U[1]		20	755U[1]		21	755U
	21	7707		16	7211		21	755U		21	755U		22	577A
	22	577A		17	7211		22	577A		22	577A		23	7707
	23	HH86		18	A3C1		23	7707		23	7707		24	755U
	24	89F1		19	A3C1		24	755U		24	755U			
	25	AC99		20	755U									
	26	PCF3												
	27	1180												

Table 7-3. A12 PCB Free-run-Mode Signatures – Address Space Test (continued)

IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE
U15	1	0000	U15	13	755U[1]	U16	10	0000	U18	6	0000	U19	1	H335
	2	755U		14	755U		11	0000		7	755U		2	C113
	3	755U					12	755U		8	0000		3	7050
	4	0000	U16	1	A3C1		13	755U		9	755U		4	755U
	5	755U		2	755U		14	755U		10	755U		5	755U
	6	0000		3	0000[1]					11	755U		6	755U
	7	0000		4	0000	U18	1	0772		12	755U		7	755U
	8	755U		5	755U		2	C4C3		13	755U		8	0000
	9	0000		6	755U		3	AA08		14	755U		9	755U
	10	755U		7	0000		4	7211		15	755U		10	755U
	11	0000		8	755U		5	A3C1		16	755U			
	12	0000[1]		9	755U									

Table 7-4. A12 PCB Output-Port-Enable Lines Test (Software Version 1-7)

Purpose: This test checks whether the output ports, located on individual A1 thru A5 PCBs, are being enabled. The signatures are read on A14P3. Each P3 pin shows the corresponding A12 PCB IC and pin number.

Test Conditions: SERVICE-NORMAL switch in SERVICE mode.
Free-run jumper J9 installed.

Signature Analyzer Setup:

START: HMBA (TP24), Trigger _/‾ (Button Out)

STOP: SOD (TP5), Trigger _/‾ (Button Out)

CLOCK: $\overline{WR}$ (U2, pin 31), Trigger _/‾ (Button Out)

GROUND: TP2 (Test Pod and Probe)

Vcc Signature: C6HU

PIN	MNE-MONIC	A12 IC & PIN	SIGNATURE	PIN	MNE-MONIC	A12 IC & PIN	SIGNATURE
1	SP13	U20-10	P946	14	SP14	U20-9	7326
2	SP11	U20-12	2U87	15	SP12	U20-11	4U4A
3	SP9	U20-14	PPFU	16	SP10	U20-13	235P
4	SP5	U21-10	4659	17	SP15	U20-7	7A80
5	SP8	U20-15	37HO	18	SP7	U21-7	A62U
6	SP6	U21-9	C9H7	19	SP4	U21-4	CPC4
7	SP3	U21-12	3069	20	SP2	U21-13	HHC2
8	SP1	U21-14	0004	21	SP0	U21-15	HC6U
9	B0	TP15	C6HU	22	B1	TP16	3227
10	B2	TP17	3227	23	B3	TP18	3227
11	B4	TP19	3227	24	B5	TP20	3227
12	B6	TP21	3227	25	B7	TP22	3227
13	GND	TP2	0000	26	+5V	TP1	C6HU

Table 7-5. Service Mode Signature Analysis of A12U25

Purpose: This table provides a means of testing the 8279 Keyboard/Display Interface IC. This IC can be tested in a limited fashion by verifying that the signatures at selected A12 data-bus test points (TP15-22) change when certain front panel pushbuttons are pressed.

Test Conditions: SERVICE-NORMAL switch in SERVICE mode.
Free-run jumper J9 installed

Signature Analyzer Setup:

START: ROM 5 line (TP9), Trigger _/‾ (Button Out).

STOP: SOD (TP5), Trigger _/‾ (Button Out).

CLOCK: $\overline{RD}$ (U2, Pin 32), Trigger _/‾ (Button Out).

GND: A12TP2 (Test pod and probe)

Vcc Signature: 9FUF

NOTE

- The A2 Ramp Generator PCB causes unstable signatures. Remove this PCB before making a signature analysis of the 8279.
- The 555 Timer circuit (A12U27, U28) causes the the signatures on data-bus bit D1 (Figure 7-12) to be unstable. Disable U27 by grounding its threshold input, pin 6.

Procedure: When activated, each of the front panel pushbuttons causes a unique keycode to be sent over the data bus (Table 7-6). This keycode can be used to verify operation of the 8279, as follows:

1. Set up the Signature Analyzer as shown above.
2. Select a test point for monitoring that has a binary weight (8, 4, 2, 1) large enough to provide a stable signature (such as TP18, 19, or 20).
3. Read the signature at the test point and verify it is stable.
4. While monitoring this stable signature, press a pushbutton that will cause the logic state of the monitored data-bus line to change; see the test points at the bottom of Table 7-6.
5. Verify that the signature either changed or became unstable when the selected pushbutton was pressed. For example: Monitor TP20 and, after ensuring a stable signature, alternately press CW F1 and ΔF F1. The signature should be unstable during operation of the two pushbuttons.

Table 7-6. Front Panel Keycode Chart

FRONT PANEL PUSHBUTTON	Decimal	FRONT PANEL KEYCODE							
		MS Byte			Binary			LS Byte	
		8	4	2	1	8	4	2	1
0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	1
2	2	0	0	0	0	0	0	1	0
3	3	0	0	0	0	0	0	1	1
4	4	0	0	0	0	0	1	0	0
5	5	0	0	0	0	0	1	0	1
6	6	0	0	0	0	0	1	1	0
7	7	0	0	0	0	0	1	1	1
8	8	0	0	0	0	1	0	0	0
9	9	0	0	0	0	1	0	0	1
Decimal Point (.)	10	0	0	0	0	1	0	1	0
Minus Sign (-)	11	0	0	0	0	1	0	1	1
F1	12	0	0	0	0	1	1	0	0
F0	13	0	0	0	0	1	1	0	1
M1	14	0	0	0	0	1	1	1	0
F2	15	0	0	0	0	1	1	1	1
ΔF	16	0	0	0	1	0	0	0	0
M2	17	0	0	0	1	0	0	0	1
LEVEL	18	0	0	0	1	0	0	1	0
SWEEP TIME	19	0	0	0	1	0	0	1	1
	20	0	0	0	1	0	1	0	0
	21	0	0	0	1	0	1	0	1
GHz/dBm/Sec	22	0	0	0	1	0	1	1	0
MHz/dB/mS	23	0	0	0	1	0	1	1	1
CLEAR ENTRY	24	0	0	0	1	1	0	0	0
SHIFT	25	0	0	0	1	1	0	0	1
	26	0	0	0	1	1	0	1	0
F1-F2	27	0	0	0	1	1	0	1	1
M1-M2	28	0	0	0	1	1	1	0	0
FULL	29	0	0	0	1	1	1	0	1
ΔF F0	30	0	0	0	1	1	1	1	0
ΔF F1	31	0	0	0	1	1	1	1	1
CW F1	32	0	0	1	0	0	0	0	0
CW F0	33	0	0	1	0	0	0	0	1
CW M1	34	0	0	1	0	0	0	1	0
CW F2	35	0	0	1	0	0	0	1	1
CW M2	36	0	0	1	0	0	1	0	0
INCREASE (F. Ver.)	37	0	0	1	0	0	1	0	1
DECREASE (F. Ver.)	38	0	0	1	0	0	1	1	0
OFF (F. Ver.)	39	0	0	1	0	0	1	1	1
	40	0	0	1	0	1	0	0	0
STEP SWEEP (GPIB)	41	0	0	1	0	1	0	0	1
MANUAL SWEEP	42	0	0	1	0	1	0	1	0
AUTO TRIGGER	43	0	0	1	0	1	0	1	1
LINE TRIGGER	44	0	0	1	0	1	1	0	0
EXT OR SINGLE SWEEP	45	0	0	1	0	1	1	0	1
VIDEO MARKER	46	0	0	1	0	1	1	1	0
RF MARKER	47	0	0	1	0	1	1	1	1
INTENSITY MARKER	48	0	0	1	1	0	0	0	0
INTERNAL LEVELING	49	0	0	1	1	0	0	0	1
POWER METER LEVELING	50	0	0	1	1	0	0	1	0
DETECTOR LEVELING	51	0	0	1	1	0	0	1	1
RF ON	52	0	0	1	1	0	1	0	0
RETRACE RF - ON	53	0	0	1	1	0	1	0	1
SELF TEST	54	0	0	1	1	0	1	1	0
RETURN TO LOCAL	55	0	0	1	1	0	1	1	1
FM AND PHASELOCK	56	0	0	1	1	1	0	0	0
DATA BUS TEST POINTS		TP 22	TP 21	TP 20	TP 19	TP 18	TP 17	TP 16	TP 15

7-7 A11 FRONT PANEL PCB

7-7.1 A11 Front Panel PCB Circuit Description

The A11 Front Panel PCB is the mounting plane for the front panel pushbuttons, indicators, and numeric displays. A block diagram of the A11 PCB circuitry is shown in Figure 7-16. A parts locator diagram is provided in Figure 7-17. A diagram of the front panel showing switch and LED numbering is provided in Figure 7-18. And the A11 PCB schematic (2 sheets) is provided in Figure 7-19.

The A11 PCB (Figure 7-16) is functionally divided into three circuits: display, switch, and LED. The display circuitry consists of the 3-to-16 Decoder (U11), the Current Source circuit (Q1-Q15), the Numeric Display digits (DS48-DS62), and the Current Sink circuit (U8, U10). The inputs to the display circuitry are scan data via the **SL0-SL3&LCAD Bus** and display-segment data via the **NA0-NA3/NB0-NB3 Bus;** both buses are from the 8279 Keyboard/Display Interface integrated circuit (A12U25). The scan data, when decoded, causes the display digits to be scanned; the segment data causes the selected segment to be lit.

The switch circuitry is divided into two groups of switches. The main switch group consists of the 3-to-8 Decoder (U7) and the 8x8 Switch Matrix (S1-S19, S22-S25, S27-S39, S42-S56, S58). The inputs to this switch circuit are the **SL0-SL3** scan bus lines from A12U25. These lines, after being decoded, sequentially scan the 8 rows of switch-matrix switches; key status is sent back to A12U25 via the 8-bit **COL1-COL8 Bus.**

The second group of switches consists of:

a. SELF TEST, which causes a microprocessor interrupt when momentarily depressed, and
b. F0, M1, M2, FREQUENCY VERNIER-INCREASE and -DECREASE, which communicate information when held depressed (paragraphs 3-2.4 and 3-2.2c respectively).

These switches have two sets of contacts—the ones shown here and another set located in the switch matrix.

The LED circuitry consists of three groups of LEDs: GPIB LEDs, LEDs that flash, and LEDs that light steadily. The GPIB LEDs are the REMOTE, LOCAL LOCKOUT, TALK, LISTEN, and SRQ indicators. The flashing LEDs are the UNLEVELED, RF OFF, SWEEPING, and EXTERNAL ALC GAIN CAL (ALC CAL) indicators. Both the GPIB and the flashing LEDs are directly controlled by lines from the A12 PCB. Except for those LEDs mentioned, all of the other front panel LEDs are non-flashing types. These non-flashing LEDs are controlled by the microprocessor via the LED Latches (U1-U6). Latches U1 thru U6 are respectively clocked by select port lines **SP16-SP21.**

7-7.2 A11 Front Panel PCB Troubleshooting Information

There is no error code for the A11 Front Panel PCB. Malfunctions occurring on this PCB should be observable from the front panel. Use the circuit description in paragraph 7-7.1 and the block diagram in Figure 7-16 to aid in troubleshooting the A11 PCB.

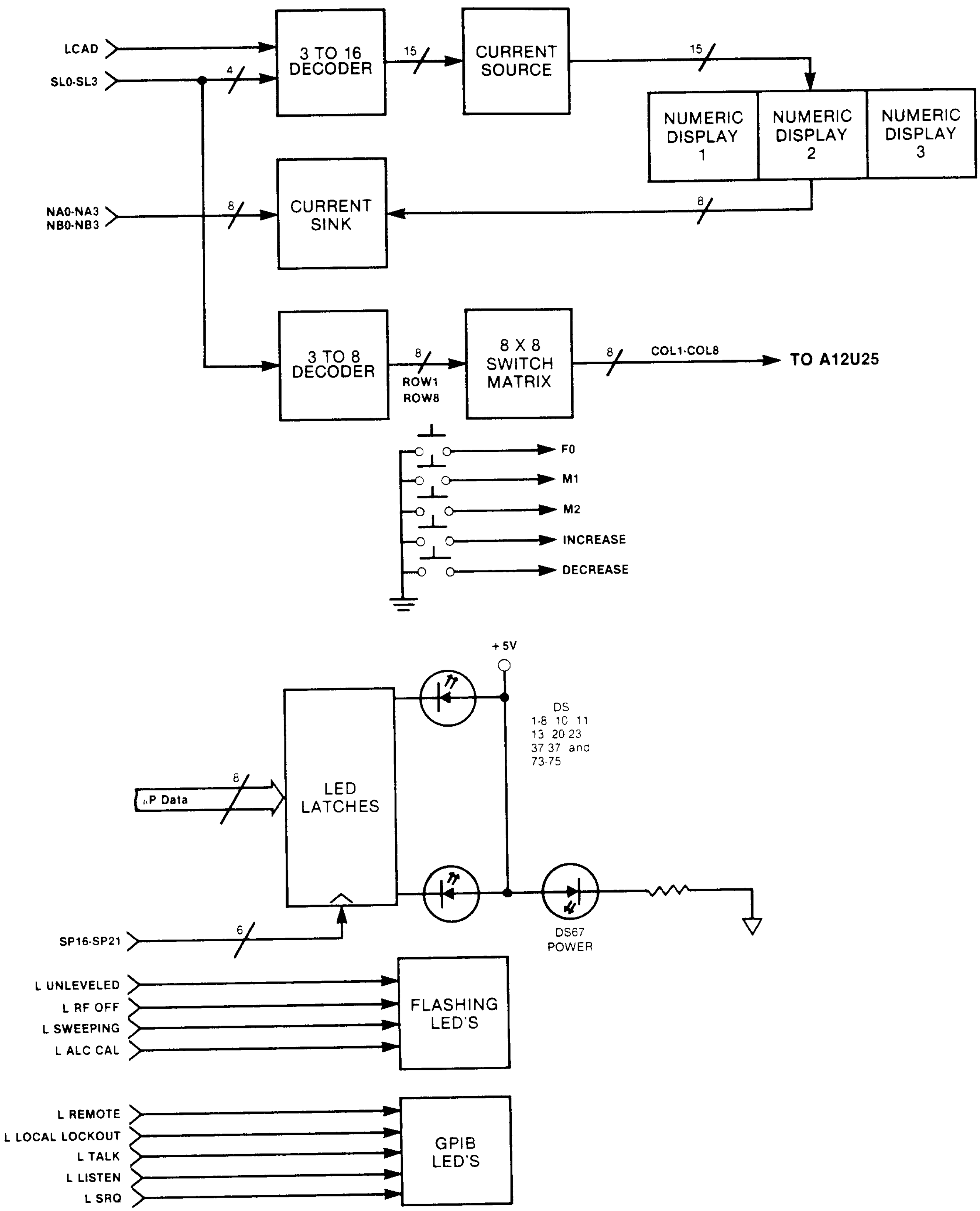
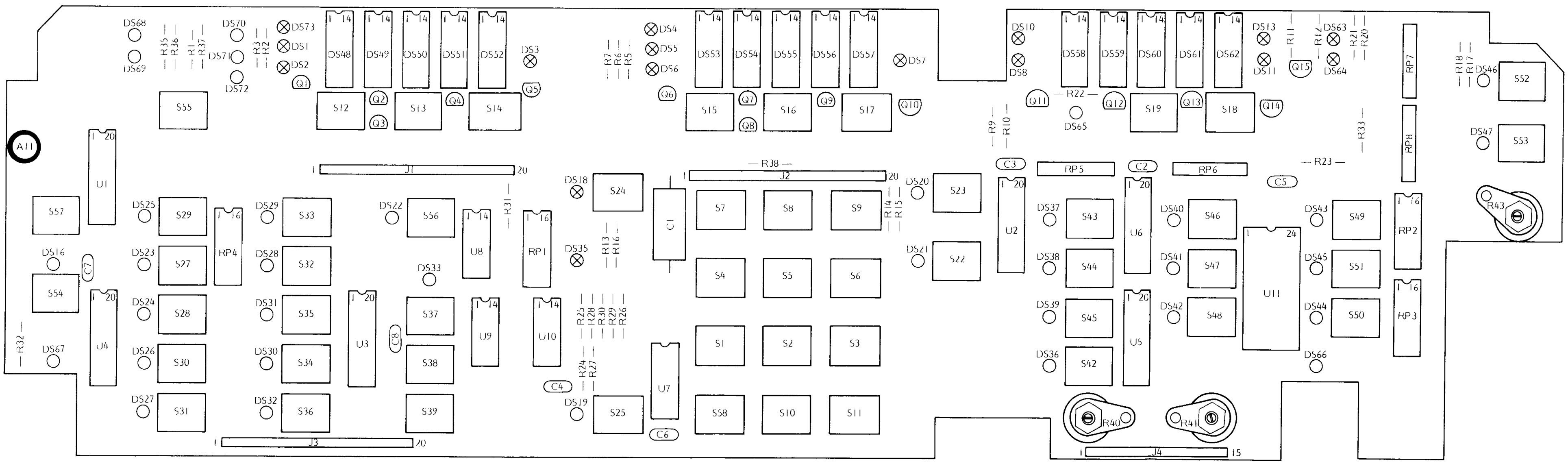


Figure 7-16. A11 Front Panel PCB, Block Diagram



NOTES:

◯ DENOTES YELLOW LED

⊗ DENOTES RED LED

Figure 7-17. A11 Front Panel PCB Parts Locator Diagram

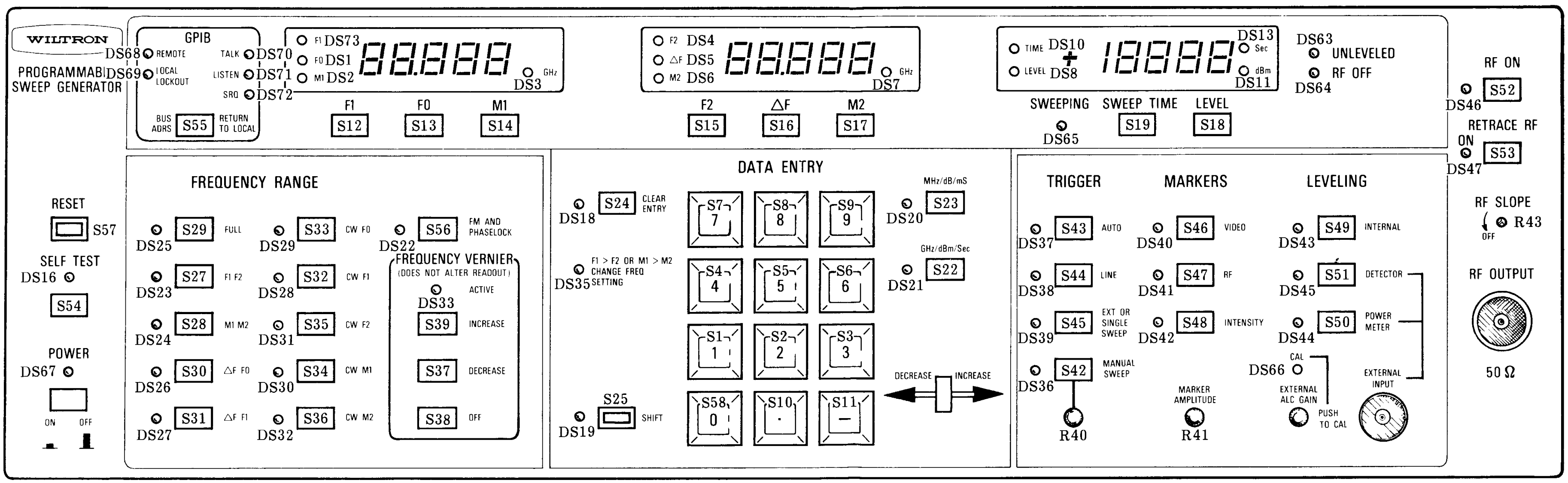
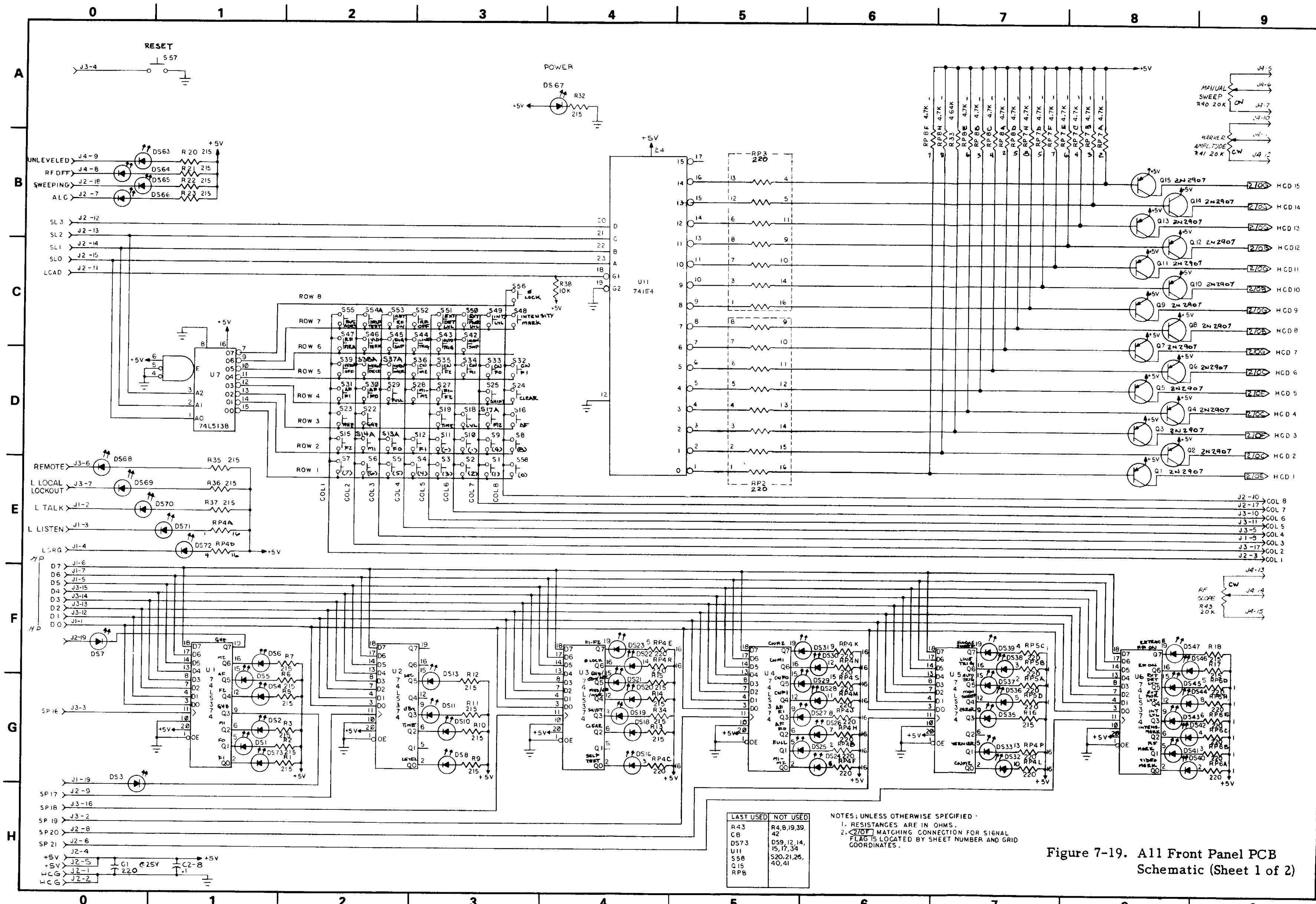


Figure 7-18. 6600 Series Front Panel, Showing Reference Designators for LEDs, Displays, Switches, and Controls



LAST USED	NOT USED
R43	R4,8,19,39,42
C8	
DS73	DS9,12,14,15,17,34
U11	
S58	S20,21,26,40,41
Q15	
RP8	

NOTES; UNLESS OTHERWISE SPECIFIED -
1. RESISTANCES ARE IN OHMS.
2. <270F] MATCHING CONNECTION FOR SIGNAL FLAG IS LOCATED BY SHEET NUMBER AND GRID COORDINATES.

Figure 7-19. A11 Front Panel PCB Schematic (Sheet 1 of 2)

7-8 A1 GPIB INTERFACE PCB

7-8.1 A1 GPIB Interface PCB Circuit Description

The A1 PCB provides the interface between the sweep generator and the IEEE-488 GPIB. The A1 PCB is microprocessor-controlled, and contains an on-board 8085 Microprocessor and 8291 GPIB Interface IC. The 8085 provides (1) control for the 8291 and other on-board circuits, and (2) communications between the A1 PCB and the A12 Microprocessor PCB. The 8291 provides communications between the sweep generator and the GPIB. Its capabilities include the following:

- Data transfer
- Handshake protocol
- Talker/listener addressing procedures
- Device clearing and triggering
- Service request (SRQ) control
- Serial and parallel-poll servicing

A functional block diagram of the A1 PCB is shown in Figure 7-20, the power-up operational program flowchart is shown in Figure 7-21, and the schematic (3 sheets) is contained in Figure 7-22.

As shown in Figure 7-20, the A1 PCB is composed of the following major circuits:

a. 6600 Analog Interface Circuits. These circuits provide the interface between the analog circuits in the sweep generator that can cause an SRQ (service request) and the GPIB microprocessor. The Analog Interface circuits are composed of the following ICs: U10C, U23A, U23B, U25D, U10A, U25A, U25B, U25C, U20B, U20A, U10D, and U16 (Figure 7-22, Sheet 2).

b. GPIB Address Switches Input Port. This circuit is the A1 PCB microprocessor input port for the rear panel GPIB address and data delimiter (CR/CR-LF) switches. The circuit is composed of U15 and its associated resistors (Figure 7-22, Sheet 2).

c. LED Drivers. These circuits drive the REMOTE, LOCAL LOCKOUT, TALK, LISTEN, and SRQ front panel GPIB LED indicators. The circuits are composed of the following components: Q1, U11D, U14A, U14B (Figure 7-22, Sheet 2), U13A, and U13B (Figure 7-22, Sheet 1).

d. 6600 μP Interface. These circuits provide interface between the A1 PCB circuits and the A12 Microprocessor PCB. The circuits are composed of the following ICs: U21A, U21B, U22, and U24 (Figure 7-22, Sheet 2).

e. ROM 2716. The ROM (read-only memory) contains the A1 PCB operational program that is flowcharted in Figure 7-21. Read-only memory consists of U4 and U5 (Figure 7-22, Sheet 1).

f. RAM 2114. The RAM (random-access memory) is the "scratchpad memory" for temporarily storing the received GPIB commands. Random-access memory consists of U2 and U3 (Figure 7-22, Sheet 1).

g. Free-Run Circuit. This circuit consists of the 18-pin jumper DIP socket U9 and its associated gates and resistors. Socket U9 is used for testing purposes—the removal of U9 causes a no-operation ("NOP") instruction to be forced into the microprocessor, causing it to free-run.

h. Address Decoder. This circuit decodes the microprocessor address bus. The outputs from this circuit are (1) active-low CE (chip enable) lines for the RAM, ROM, 8255, and 8291 ICs and (2) enable inputs for the U13A and U13B TALK and LISTEN indicator drivers.

i. Option Interface 8255. This circuit, consisting of the 8255 Microprocessor Interface IC (U1), is not presently used.

j. Microprocessor 8085 and GPIB Interface IC 8291. These two circuits are described in the opening paragraph under the A1 PCB Circuit Description heading.

k. SERVICE NORMAL Switch (S1). In the SERVICE position, S1 interrupts the microprocessor and causes it to run a stimulus routine for signature-analysis testing.

When the front panel POWER switch is depressed and ac power is turned on, the A1 PCB goes into the flowcharted routine of Figure 7-21. The A1 PCB remains in this looping routine until the ac power is turned off.

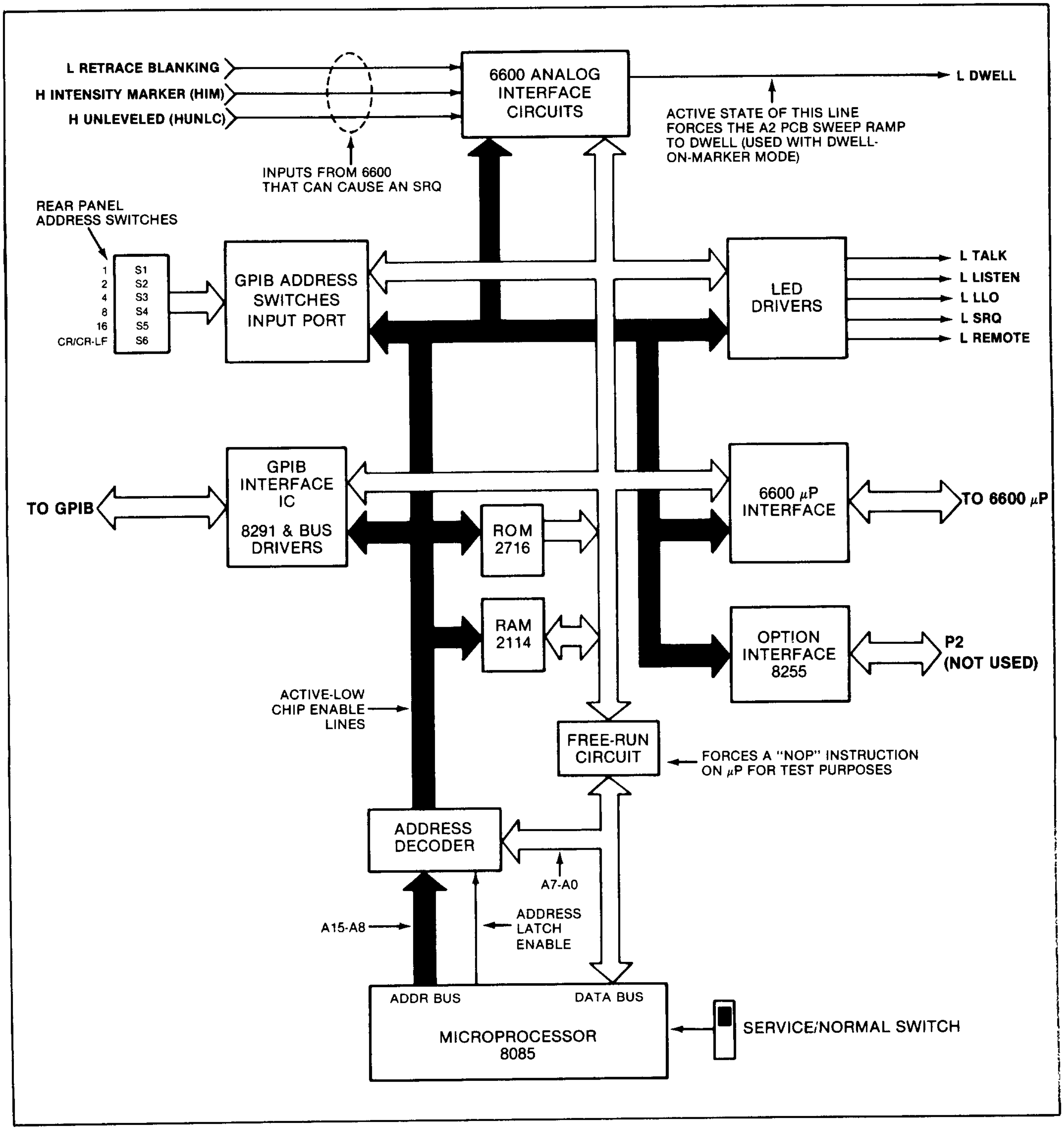


Figure 7-20. A1 GPIB Interface PCB, Overall Block Diagram

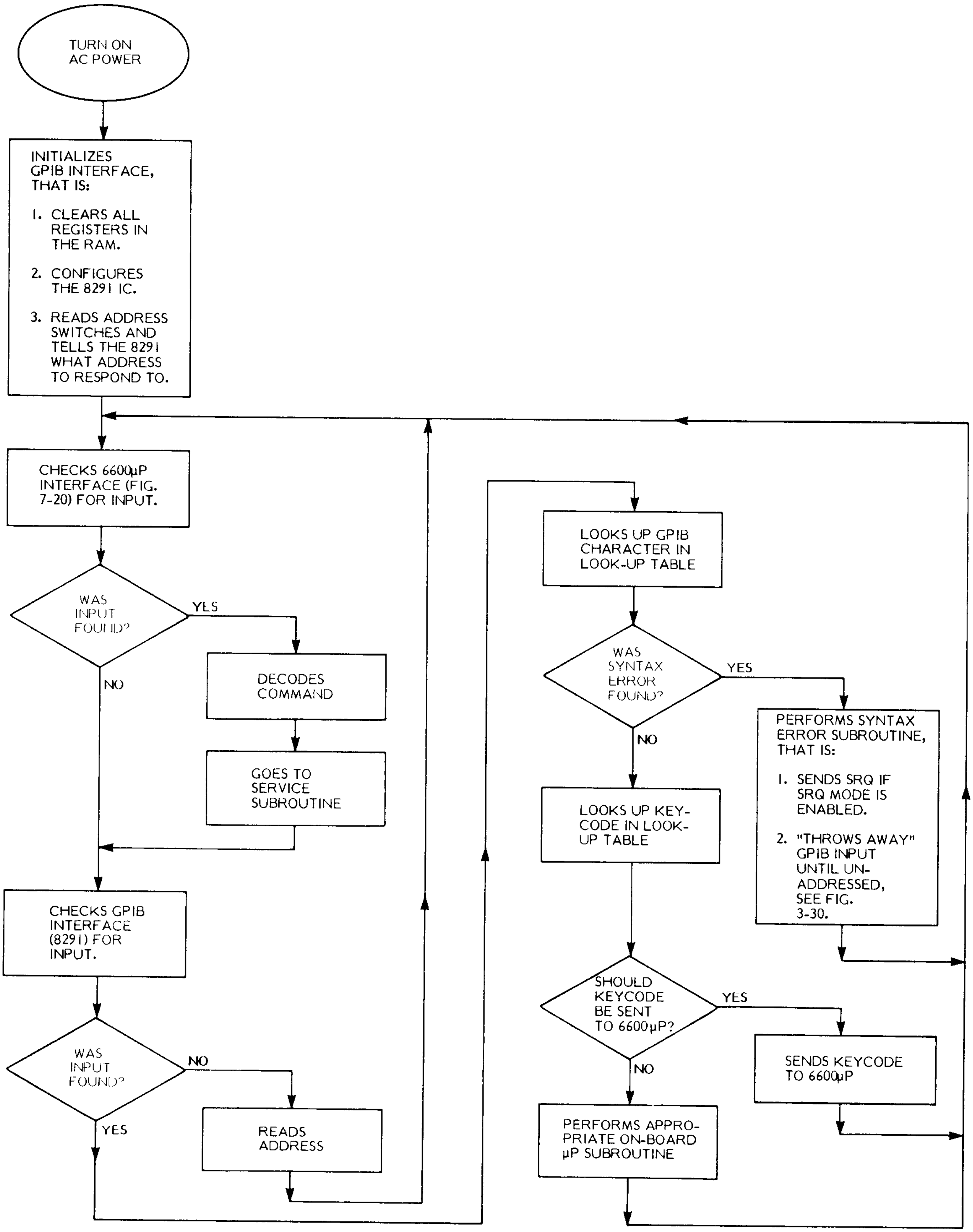
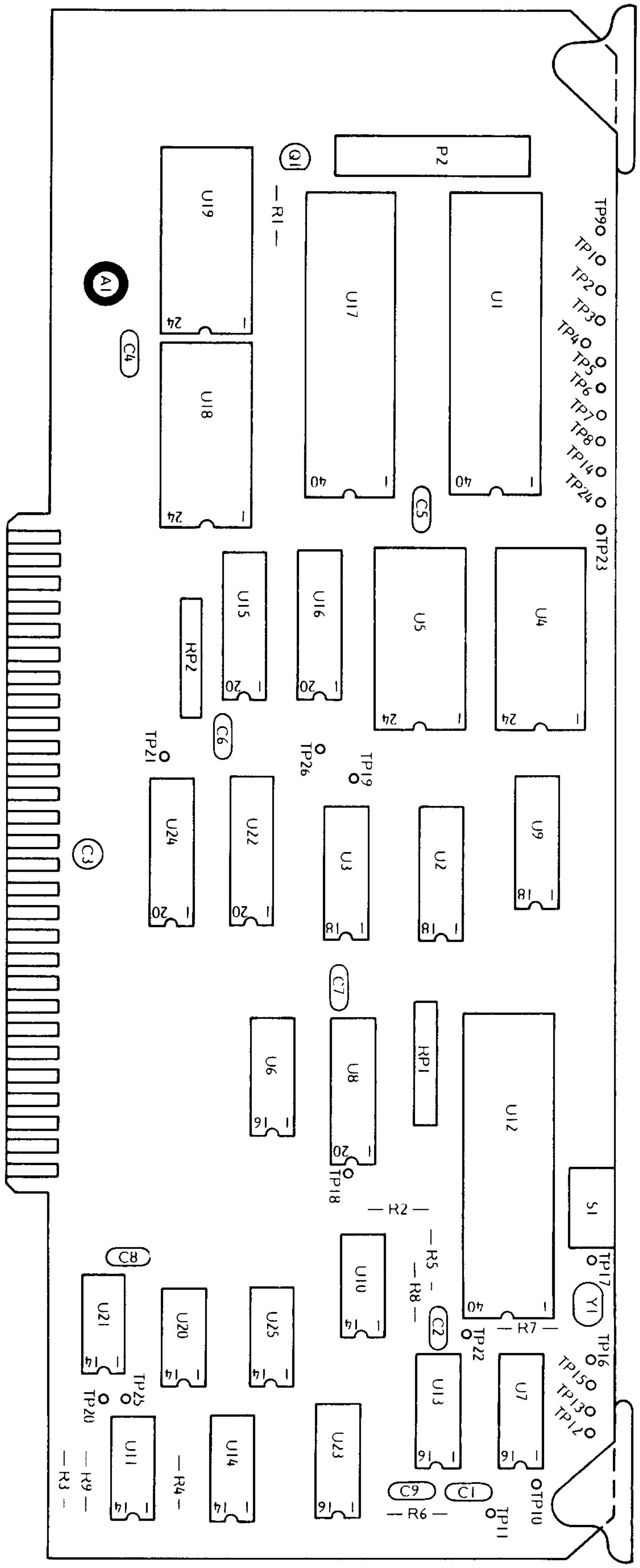


Figure 7-21. A1 PCB, AC Power-On Operational Flowchart



A1 PCB Parts Locator Diagram

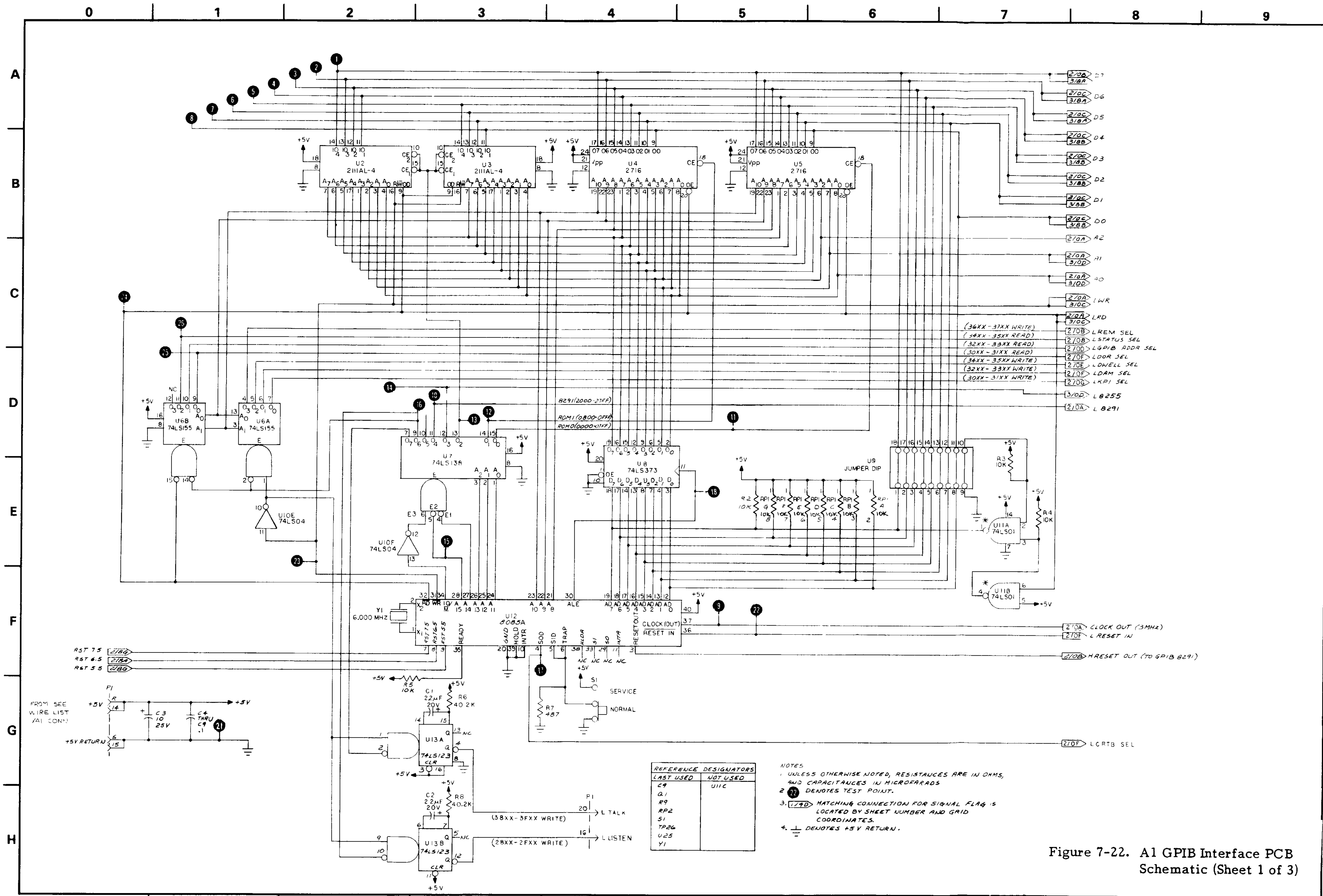


Figure 7-22. A1 GPIB Interface PCB Schematic (Sheet 1 of 3)

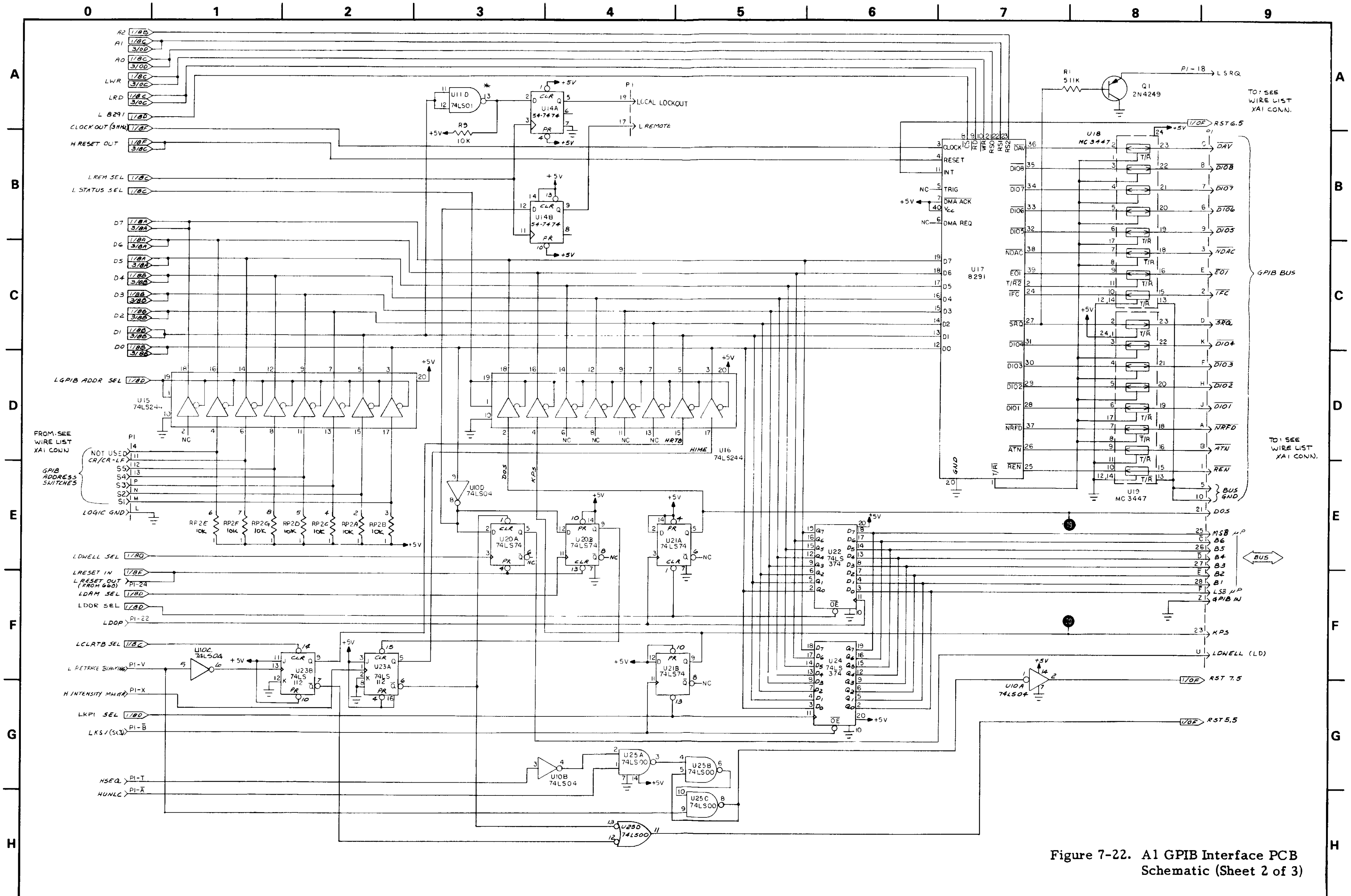
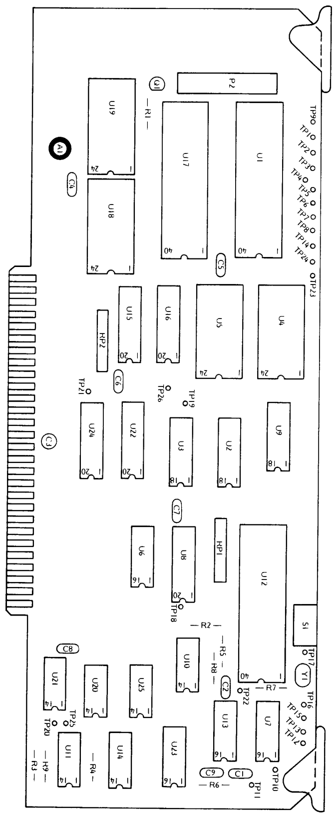


Figure 7-22. A1 GPIB Interface PCB Schematic (Sheet 2 of 3)



A1 PCB Parts Locator Diagram

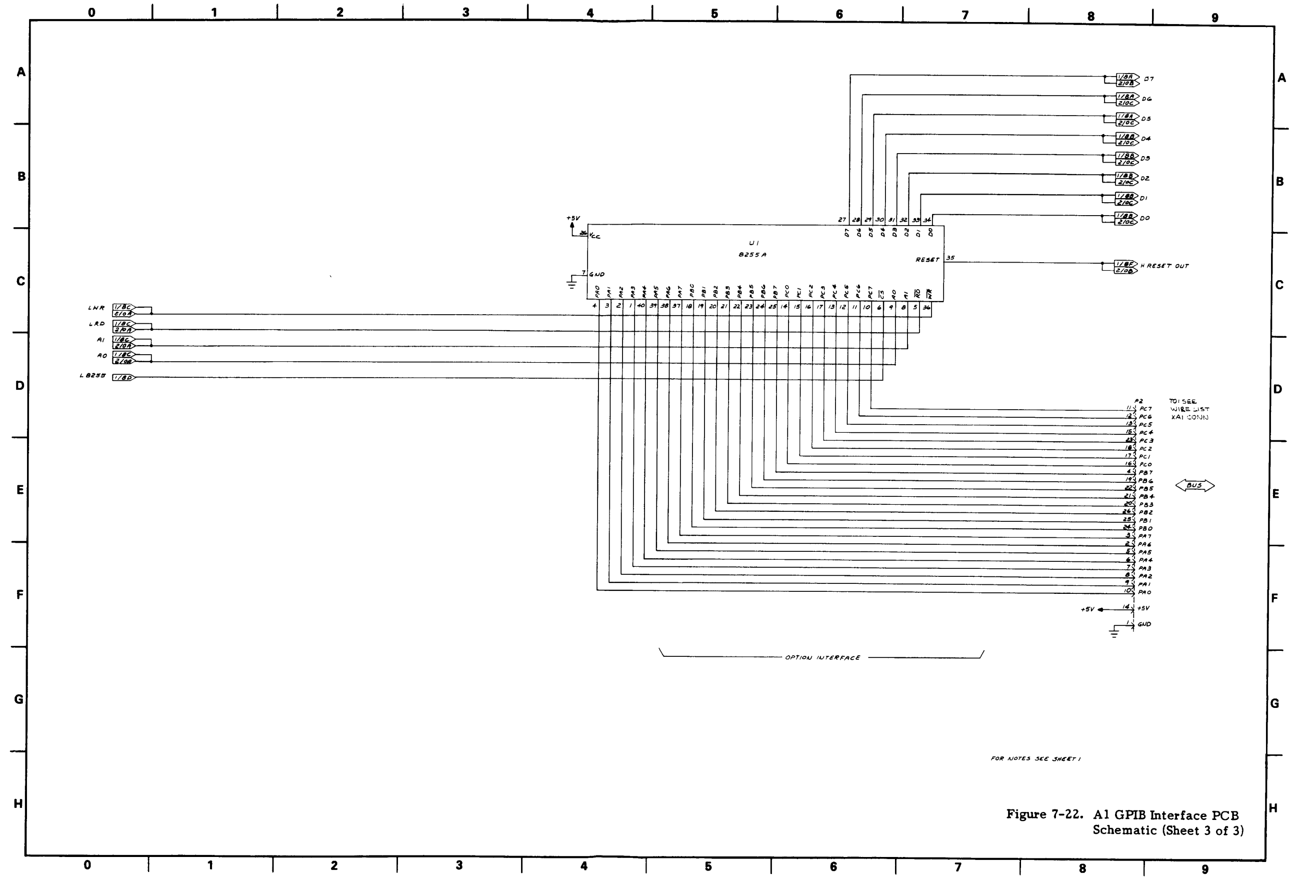


Figure 7-22. A1 GPIB Interface PCB Schematic (Sheet 3 of 3)

parts locator

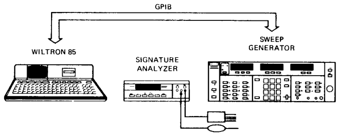


Figure 7-23. Test Equipment Setup for Troubleshooting Error Code 24

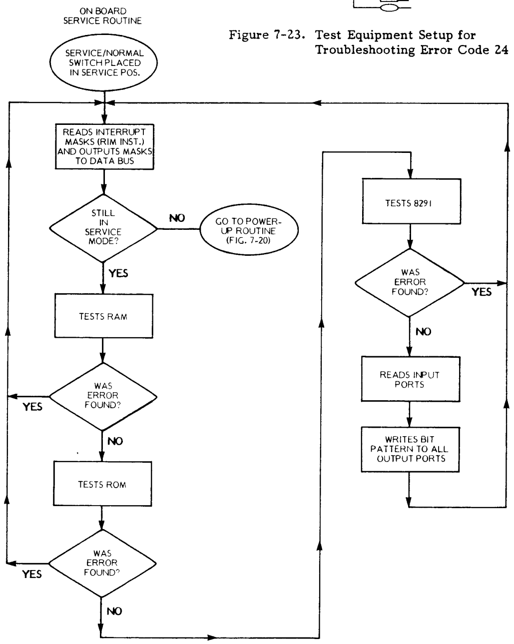


Figure 7-24. A1 PCB On-Board Service Routine

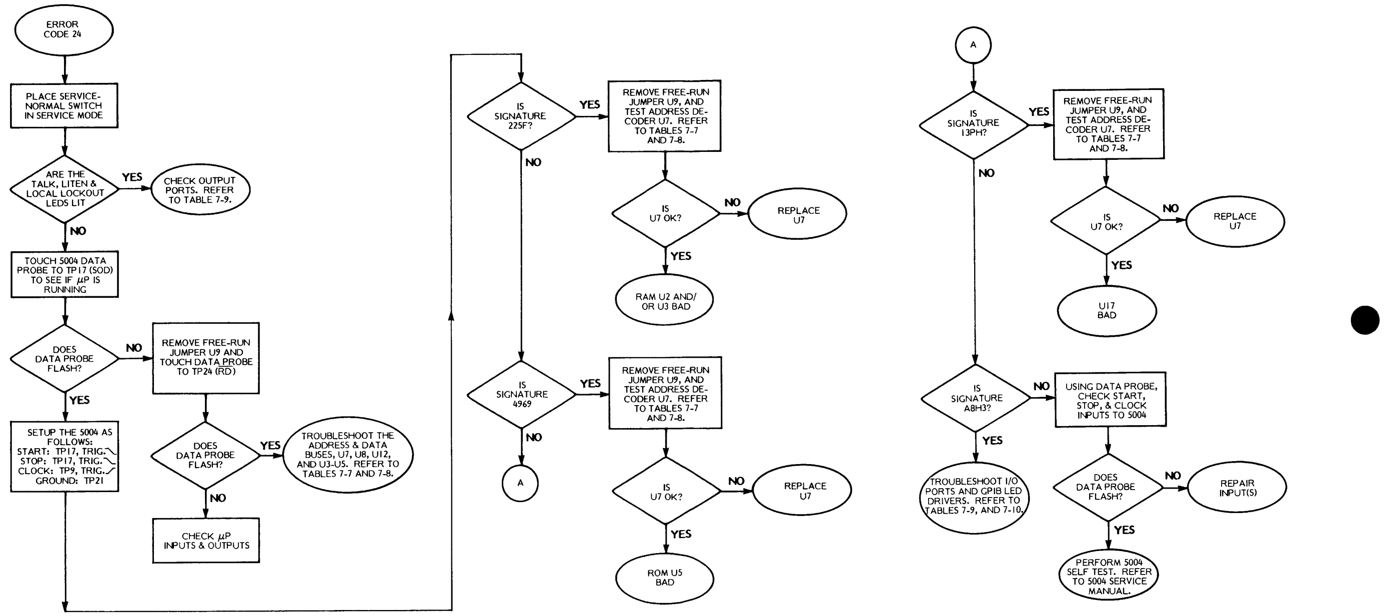


Figure 7-25. Error Code 24 Troubleshooting Flowchart

Fig. 7-23 & 7-24

7-8.2 A1 GPIB Interface PCB Troubleshooting Information and Data

Error Code 24 reports on the status of the A1 GPIB Interface PCB. The microprocessor routine associated with this error code initiates a subroutine (Figure 7-26) that tests the A1 RAM, ROM, and 8291 circuits. The test equipment setup for troubleshooting Error Code 24 is provided in Figure 7-23 (facing page); the troubleshooting flowchart is provided in Figure 7-25.

Signature analysis is the recommended method for troubleshooting A1 circuits. In addition to a free-run mode (explained in HP Application Note 222-2), the A1 PCB also has a service mode. In this mode, routines stored in ROM U5 provide two methods for isolating to faulty components. The first uses a "loop-on-fail" technique (Figure 7-24) that allows the signature analyzer to quickly isolate a malfunctioning RAM, ROM, or 8291 GPIB Interface IC circuit. In this method, the signature analyzer will display one of four characteristic (Vcc) signatures, depending on which loop is being executed. If no faults are found, a specific signature is displayed. A fault in either the RAM, ROM, or 8291 provides a signature that is different for each.

The second service-mode method, a routine which writes to the output ports, input ports and retrace-blanking flip flop, provides for signature analysis of these components. These tests are contained in Tables 7-9 thru 7-11 respectively. Note that the Table 7-9 and 7-11 signatures are dependent on the software version contained in ROM. The software-version number appears on a label affixed to ROM U5.

For free-run signature analysis two tables of signatures are provided. Tables 7-7 and 7-8 respectively provide signatures for the microprocessor's read and write spaces. Both of these tables provide test and signature analyzer setup conditions. When these conditions are met, a characteristic (Vcc) signature will be displayed; the microprocessor circuit may then be accurately tested.

In addition to signatures, the 5004A Signature Analyzer data probe may be used like a logic probe. When a circuit node is touched, the probe tip will either flash, light steadily, or

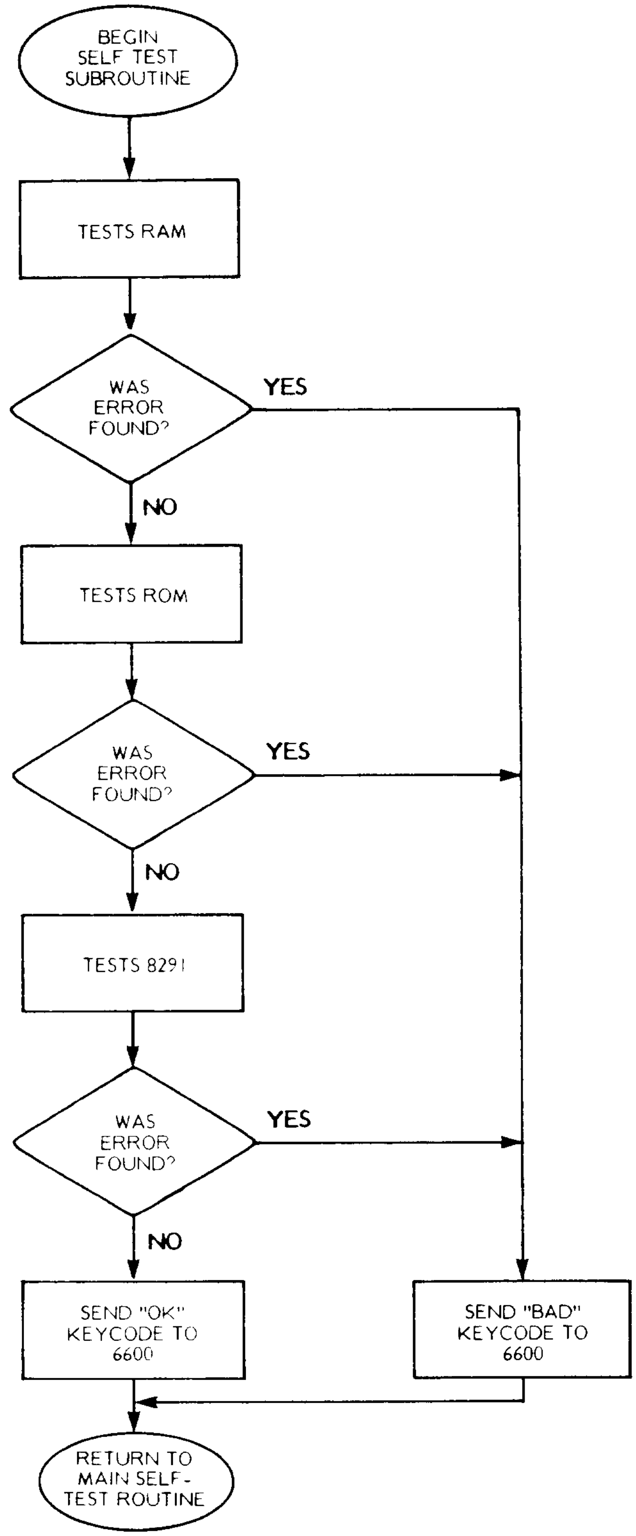


Figure 7-26. A1 PCB Self-Test Subroutine

not be lit. A steadily-lit probe indicates a logic 1 or Vcc. An unlit probe indicates a logic 0 or ground. And a flashing probe usually indicates pulses; however, it can also indicate noise. A noise indication sometimes occurs when the probe is touched to an open node, or when it is touched to a tri-state-buffer node where the buffer is in its off state. When testing such nodes, the 5004A will read the Vcc signature when its RESET button is pressed. To help minimize probe noise pickup, ground the probe at the same point the test pod is grounded.

Table 7-7. A1 PCB Free-run Mode Signatures – Read Space Test

GENERAL:

Test Conditions: SERVICE-NORMAL switch in NORMAL.
Free-run jumper U9 removed.

Signature Analyzer Setup:

START: Bit A15 (TP15), Trigger ↘ (Button In)

STOP: Bit A15 (TP15), Trigger ↗ (Button Out)

CLOCK: $\overline{RD}$ (TP24), Trigger ↗ (Button Out)

GROUND: TP21 (Test Pod and Probe)

Vcc Signature: 755U

NOTE

[1] Test probe flashes.
[2] Signature may be unstable.
[3] May have to press RESET on probe.

IC	PIN NO.	SIGNATURE
U2	1	0772
	2	7050
	3	C113
	4	H335
	5	AA08
	6	7211
	7	A3C1
	8	0000
	9	0000
	10	P352
	15	P352
	16	755U
	17	C4C3
	18	755U
U3	1	0772
	2	7050
	3	C113
	4	H335
	5	AA08
	6	7211
	7	A3C1
	8	0000
	9	0000
	10	P352
	15	P352
	16	755U
	17	C4C3
	18	755U
U5	1	A3C1
	2	7211
	3	AA08
	4	C4C3
	5	0772
	6	7050
	7	C113

IC	PIN NO.	SIGNATURE
U5	8	H335
	12	0000
	18	4CP2
	19	HH86
	20	0000[1]
	21	755U
	22	577A
	23	7707
	24	755U
U6	1	0000
	2	F615
	3	HH86
	4	755U
	5	755U
	6	755U
	7	755U
	8	755U
	9	2HU0
	10	CF3F
	11	9181
	12	C307
	13	577A
	14	F615
	15	0000[1]
	16	755U
U7	1	89F1
	2	AC99
	3	PCF3
	4	1180
	5	0000[1]
	6	755U
	7	6F7P
	8	0000
	9	F615
	10	2F25

IC	PIN NO.	SIGNATURE
U7	11	8UH9
	12	340A
	13	P352
	14	U1U2
	15	4CP2
	16	755U
U8	1	0000
	2	H335
	3	755U[1]
	4	755U[1]
	5	C113
	6	7050
	7	755U[1]
	8	755U[1]
	9	0772
	10	0000
	11	0000[1]
	12	C4C3
	13	755U[1]
	14	755U[1]
	15	AA08
	16	7211
	17	755U[1]
	18	0000[1]
	19	A3C1
	20	755U
U12	1	755U[1]
	2	0000[1]
	3	0000
	4	755U
	5	0000
	6	0000
	7	0000
	8	0000
	9	0000

IC	PIN NO.	SIGNATURE
U12	10	0000
	11	755U
	12	755U[1]
	13	755U[1]
	14	755U[1]
	15	755U[1]
	16	755U[1]
	17	755U[1]
	18	755U[1]
	19	0000[1]
	20	0000
	21	7707
	22	577A
	23	HH86
	24	89F1
	25	AC99
	26	PCF3
	27	1180
	28	0000[1]
	29	755U
	30	0000[1]
	31	755U
	32	0000[1]
	33	755U
	34	0000
	35	755U
	36	755U
	37	755U[1]
	38	0000
	39	0000
	40	755U
U15	1	CF3F
	2	755U[1]
	4	755U
	6	755U
	8	755U

IC	PIN NO.	SIGNATURE
U15	10	0000
	11	755U
	13	755U
	15	755U
	17	755U
	19	CF3F
	20	755U
U16	1	9181
	2	0000
	4	755U
	6	755U[3]
	8	755U[1]
	10	0000
	11	755U
	13	755U
	15	0000
	17	0000
	19	9181
	20	755U
U17	1	755U
	2	755U
	3	755U[1]
	4	0000
	5	0000
	6	755U
	7	755U
	8	8UH9
	9	0000[1]
	10	755U
	11	0000[1]
	20	0000
	21	H335[2]
	22	C113[2]
	23	7050
	24	755U

Table 7-7. A1 PCB Free-run Mode Signatures – Read Space Test (continued)

IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE
U17	25	755U	U17	29	0000	U17	32	755U	U17	35	755U	U17	38	755U
	26	755U		30	0000		33	0000		36	755U		39	755U
	27	0000		31	755U		34	0000		37	755U		40	755U
	28	0000												

Table 7-8. A1 PCB Free-run Mode Signatures – Address Space Test

GENERAL:

Test Conditions: SERVICE-NORMAL switch in NORMAL.
Free-run jumper U9 removed.

Signature Analyzer Setup:

START: Bit A15 (TP15), Trigger ⌐_ (Button In)

STOP: Bit A15 (TP15), Trigger _/ (Button Out)

CLOCK: ALE (TP18), Trigger ⌐_ (Button In)

GROUND: TP21 (Test Pod and Probe)

Vcc Signature: 755U

NOTE

[1] Test probe flashes.
[2] Signature may be unstable.
[3] May have to press RESET on probe.

IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE
U2	1	0772	U5	1	A3C1	U6	13	577A	U8	16	7211	U12	32	755U[1]
	2	7050		2	7211		14	F615		17	7211		33	755U
	3	C113		3	AA08		15	755U[1]		18	A3C1		34	0000
	4	H335		4	C4C3		16	755U		19	A3C1		35	755U
	5	AA08		5	0772					20	755U		36	755U
	6	7211		6	7050	U7	1	89F1					37	755U[1]
	7	A3C1		7	C113		2	AC99	U12	1	755U[1]		38	0000
	8	0000		8	H335		3	PCF3		2	0000[1]		39	0000
	9	755U[1]		9	755U[1]		4	1180		3	0000		40	755U
	10	P352		10	755U[1]		5	0000[1]		4	755U			
	11	755U[2]		11	755U[1]		6	755U		5	0000	U15	1	755U[1]
	12	755U[2]		12	0000		7	6F7P		6	0000		2	755U[1]
	13	755U[2]		13	755U[2]		8	0000		7	0000		3	755U[2]
	14	Unstable		14	755U[2]		9	F615		8	0000		4	755U
	15	P352		15	755U[2]		10	2F25		9	0000		5	755U[2]
	16	755U		16	Unstable		11	8UH9		10	0000		6	755U
	17	C4C3		17	Unstable		12	340A		11	755U		7	755U[2]
	18	755U		18	4CP2		13	P352		12	H335		8	755U
				19	HH86		14	U1U2		13	C113		9	Unstable
U3	1	0772		20	755U[1]		15	4CP2		14	7050		10	0000
	2	7050		21	755U		16	755U		15	0772		11	755U
	3	C113		22	577A					16	C4C3		12	755U[1]
	4	H335		23	7707	U8	1	0000		17	AA08		13	755U
	5	AA08		24	755U		2	H335		18	7211		14	755U[1]
	6	7211					3	H335		19	A3C1		15	755U
	7	A3C1	U6	1	0000		4	C113		20	0000		16	755U[1]
	8	0000		2	F615		5	C113		21	7707		17	755U
	9	755U[1]		3	HH86		6	7050		22	577A		18	Unstable
	10	P352		4	755U		7	7050		23	HH86		19	755U[1]
	11	755U[2]		5	755U		8	0772		24	89F1		20	755U
	12	755U[2]		6	755U		9	0772		25	AC99			
	13	755U[2]		7	755U		10	0000		26	PCF3	U16	1	755U[1]
	14	Unstable		8	0000		11	755U[1]		27	1180		2	0000
	15	P352		9	755U[1]		12	C4C3		28	0000[1]		3	755U[2]
	16	755U		10	755U[1]		13	C4C3		29	755U		4	755U
	17	C4C3		11	755U[1]		14	AA08		30	755U[1]		5	755U[2]
	18	755U		12	755U[1]		15	AA08		31	755U		6	755U

Table 7-8. A1 PCB Free-run Mode Signatures – Address Space Test (continued)

IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE
U16	7	755U[2]	U16	18	Unstable	U17	8	8UH9	U17	19	Unstable	U17	30	0000
	8	755U[1]		19	755U[1]		9	755U[1]		20	0000		31	755U
	9	Unstable		20	755U		10	755U		21	H335		32	0000
	10	0000					11	0000		22	C113		33	0000
	11	755U	U17	1	755U		12	755U[2]		23	7050		34	0000
	12	755U		2	755U		13	755U[2]		24	755U		35	755U
	13	755U		3	755U[1]		14	755U[2]		25	755U		36	755U
	14	755U		4	0000		15	Unstable		26	755U		37	755U
	15	0000		5	0000		16	755U[2]		27	0000		38	755U
	16	755U		6	0000		17	755U[2]		28	0000		39	755U
	17	0000		7	755U		18	755U[2]		29	0000		40	755U

Table 7-9. A1 PCB Output-Port Test (Software Version 3)

Purpose: This test verifies whether the A1 PCB is outputting data to the A12 Microprocessor.

Test Conditions: SERVICE-NORMAL switch in SERVICE mode.
Free-run jumper U9 installed.

Signature Analyzer Setup:

START: U7, Pin 9 (TP16), Trigger _/¯ (Button Out)

STOP: SOD (TP17), Trigger _/¯ (Button Out)

CLOCK: $\overline{WR}$ (TP23), Trigger _/¯ (Button Out)

GROUND: TP21 (Test Pod and Probe)

Vcc Signature: C637

NOTE

If the 5004 reads identical signatures (other than Vcc) on successive IC pins, or if the probe does not flash when a signature (other than Vcc) is read, check the front panel GPIB indicators. Correct status is: TALK, LISTEN, and LOCAL LOCKOUT brightly lit; SRQ and REMOTE dimly lit. If this is not the case, recycle both the A1 and A12 SERVICE-NORMAL switches.

IC	PIN NO.	SIGNATURE	IC	PIN NO.	SIGNATURE
U22	1	C637*	U24	1	C637*
	2	9UU5		2	C637*
	3	C637*		3	9UU5
	4	C637*		4	29F1
	5	29F1		5	C637*
	6	9UU5		6	C637*
	7	C637*		7	9UU5
	8	C637*		8	29F0
	9	29F0		9	0000*
	10	0000		10	0000
	11	C637*		11	51P2
	12	9UU4		12	C637
	13	0000		13	9UU4
	14	C637*		14	29F0
	15	29F0		15	C637
	16	9UU4		16	C637
	17	0000*		17	9UU4
	18	C637*		18	29F1
	19	29F1		19	C637*
	20	C637		20	C637

* Logic Probe flashes.

Table 7-10. A1 PCB Input Port Test

Purpose: This test can be used to check whether the A1 PCB is responding to inputs from the GPIB.

Test Conditions: SERVICE-NORMAL switch in SERVICE mode.
Free-run jumper U9 installed.

Signature Analyzer Setup:

START: LDOR SEL (TP25), Trigger ⌐_ (Button In)

STOP: L STATUS SEL (TP26), Trigger _/‾ (Button Out)

CLOCK: $\overline{RD}$ (TP24), Trigger _/‾ (Button Out)

GROUND: TP21 (Test Pod and Probe)

Vcc Signature: 72A2

NOTE

If the 5004 reads identical signatures (other than Vcc) on successive IC pins, or if the probe does not flash when a signature (other than Vcc) is read, check the front panel GPIB indicators. Correct status is: TALK, LISTEN, and LOCAL LOCKOUT brightly lit; SRQ and REMOTE dimly lit. If this is not the case, recycle both the A1 and A12 SERVICE-NORMAL switches.

Procedure:

1. Set up test equipment as shown in Figure 7-23.
2. Sequentially touch the data probe to TP1 thru TP7; verify that each test point exhibits a stable signature.
3. Using controller, send the following statements over the bus:

```
10 OUTPUT 705 ;"FUL"
20 GOTO 10
30 END
```

4. Recheck the above test points and verify that TP2 thru TP7 exhibit unstable signatures.

Table 7-11. A1 PCB Retrace Blanking Flip-Flop Test (Software Version 3)

Purpose: This test verifies whether the Retrace Blanking FF (U23) is working properly.

Test Conditions: SERVICE-NORMAL switch in SERVICE mode.
Free-run jumper U9 installed.

Signature Analyzer Setup:

START: SOD (TP17), Trigger ⎺\⎽ (Button In)

STOP: SOD (TP17), Trigger ⎺\⎽ (Button In)

CLOCK: CLOCK (OUT) (TP9), Trigger ⎽/⎺ (Button Out)

GROUND: TP21 (Test Pod and Probe)

Vcc Signature: A8H3

IC	PIN NO	SIGNATURE	IC	PIN NO.	SIGNATURE
U23	1	0000	U23	9	6725
	2	0000		10	A8H3
	3	A8H3		11	A8H3
	4	A8H3		12	0000
	5	0000		13	A8H3
	6	0000		14	OFHP
	7	FU56		15	89C8
	8	0000		16	A8H3

* Logic Probe LED flashes.

7-9 A2 RAMP GENERATOR PCB

7-9.1 A2 Ramp Generator PCB Circuit Description

The A2 Ramp Generator PCB generates one of the voltage tuning signals used to produce the sweep generator's sweep-frequency output. The PCB also generates the **RETRACE BLANKING** (+), (-), **BANDSWITCH BLANKING** (+), (-), and **SEQ SYNC** signals that are output to the respective rear panel connectors. A functional block diagram of this PCB is shown in Figure 7-28; the schematic diagram (3 sheets) is shown in Figure 7-29. The A2 PCB consists of three functional blocks (Figure 7-28), which are described below.

a. Ramp Generator. This functional block produces the PCB sweep ramp output signal and the two retrace blanking pulses that are supplied to the RETRACE BLANKING (+) and (-) rear panel connectors. The block also provides control for the relay connected to the rear panel PENLIFT OUTPUT connector. The input to this functional block is the front panel SWEEP TIME control group from the A12 Microprocessor PCB. Eight bits of this nine-bit group are latched into the digital-to-analog converter (DAC) circuit (U15) when the microprocessor clocks **SP13** HIGH. The DAC output is a negative voltage that causes the Sweep Ramp Integrator (U20B) to integrate in the positive direction. When the sweep ramp reaches 10 volts, the 10V Compare circuit (U25B, U25C) causes the Sweep Direction and Dwell Gating circuit (U24A, U24B, U2A, U2B, U17C) to open Switch A and close Switch B. This switching action causes the integrator to integrate in the negative direction (retrace) at a fixed rate (10 ms for sweep speeds between .010 and 1 second, 1 second for sweep speeds between 1 and 99 seconds). When 0 volts is reached, the 0V Compare circuit then causes Switch B to open and Switch A to close. This Switch A/Switch B arrangement reconfigures the integrator to again integrate in the positive direction. A typical sweep ramp waveform is shown in Figure 7-27.

The **1 SECOND CONTROL** bit (the ninth bit in the SWEEP TIME group) is a >1-or a <1-second flag bit. For sweep speeds between 1 and 99 seconds, this bit is HIGH. This HIGH causes the Sweep Ramp Integrator to integrate at the slower sweep-time rate.

The Retrace Blanking Logic circuit (Q2, U10C) causes both a plus (+) and a minus (-) 5 volt pulse to be generated during sweep retrace. The same signal that opens Switch A initiates these retrace blanking pulses.

The **H SWP** bit goes TRUE (high) to indicate when a forward sweep is in progress. This bit is supplied to the A12 Microprocessor, where it causes the front panel SWEEPING indicator to light.

The Activate Relay Logic circuit (Q3) controls relay A14K1, which is the relay that connects to the rear panel PENLIFT OUTPUT connector. This circuit holds the relay deactivated (that is, the normally-open (NO) contacts open and the normally-closed (NC) contacts closed) when any of the following occur:

1. The 1 **SECOND CONTROL** bit is LOW (sweep speeds between 10 ms and 1 s).
2. The **H SWP** bit is false (forward sweep not in progress).
3. The **H RESET** bit is TRUE (single-sweep is reset, subparagraph c below).
4. THE TRIGGER **EXT OR SINGLE SWEEP** control-word bit is not HIGH (subparagraph c below).

b. Sweep Dwell and Related Circuits. The sweep dwell circuit causes the sweep ramp to dwell when:

1. The end of an oscillator band (EOB) is reached (bandswitch point).
2. An intensity marker command is received.

3. The top of the sweep ramp (10V) is reached.

4. The bottom of the sweep ramp (0V) is reached.

When any one of the above dwell conditions is detected, the Initiate Dwell circuit (U16B, U17A, U22A, U22B, U23A) sets the **DWELL** line HIGH. This HIGH causes the following to occur. It causes the Sweep Direction and Dwell Gating circuit to open Switch A and Switch B and halt voltage integration. It causes the Level Dip flip-flop (U1A) to output a logic-low that causes the A4 PCB to "dip" the RF output power (except on an intensity marker). And it enables the clock in the Dwell Timing circuit (U3) to run at approximately 288 kHz, which causes a timing sequence to be initiated. This timing sequence consists of three timing pulses: **TP2, TP5,** and **TP6.** The first occurring pulse, **TP2,** loads the dwell word (described below) into the Down Counter (U9, U13). The second occurring pulse, **TP5,** resets the Level Dip circuit. And the third occurring pulse, **TP6,** causes both the U3 clock to slow to approximately 7 kHz and the Down Counter to become enabled. When enabled, the Down Counter sequentially counts down each time it is clocked. When a zero count is reached, the **U11 CLOCK** line is gated

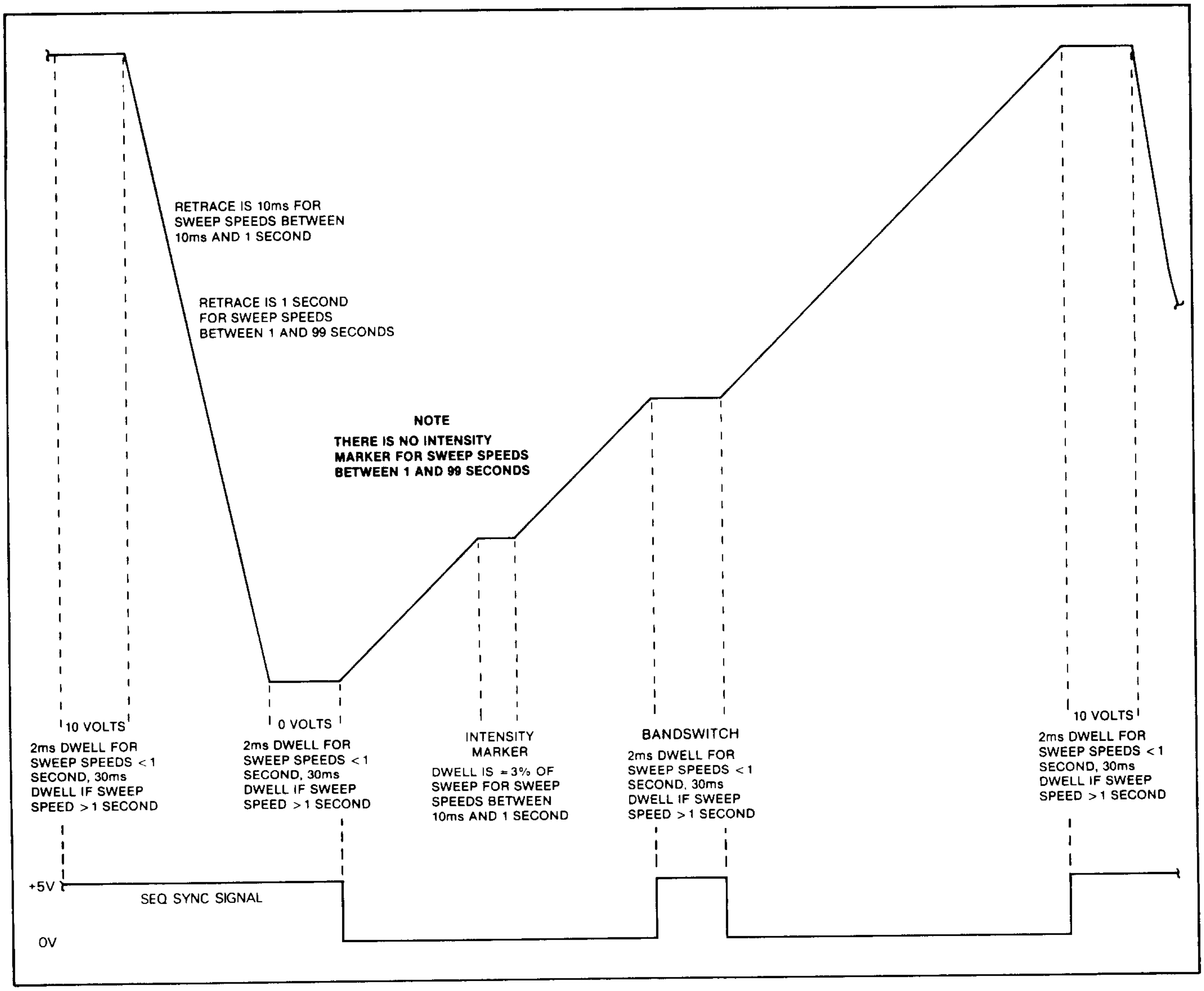


Figure 7-27. A2 PCB Sweep Ramp and Sequential Sync Pulse

HIGH. If the A2 INT-EXT switch (S1) is in INT, the **U11 CLOCK** line clocks the **L STRB** output from the Ext Sweep Logic circuit (U11A) TRUE (low). This **L STRB** output is applied to the Sweep Trigger Control Decoder circuit (U19) (subparagraph c below).

The dwell word that TP2 loads into the Down Counter may be any of three words, depending on why dwell was commanded. If the dwell command was intensity marker and the sweep time is less than 1 second, the dwell word is the SWEEP TIME group previously loaded into the Latch (U7). If the dwell command was EOB, 10V, or 0V, the dwell word is either a 2 ms or a 30 ms word. The dwell word is 2 ms if the **1 SECOND CONTROL** bit is a 0, and 30 ms if the bit is a 1.

The related circuits in this block are the Seq Sync Logic (U23B, U5D, Q4) and the Bandswitch Blanking (Q5, Q6) circuits. The Seq Sync Logic circuit outputs a +5V pulse (Figure 7-27) during an oscillator bandswitch, 0-and 10-volt dwell periods, and sweep ramp retrace. This pulse goes to the A1 PCB (**H SEQ**) and to the rear panel SEQ SYNC connector.

The Retrace Blanking circuit outputs plus and minus (+, -) 5V pulses during sweep ramp retrace. These pulses go to the respective rear panel connectors.

c. Sweep Trigger Control. This functional block controls the recurrence of the A2 PCB sweep ramp. The input to this block is an 8-bit control group from the A12 Microprocessor PCB. This word is latched into the Control Word Latch and Logic circuit (U14, U2C, U5F) when the microprocessor clocks **SP14** HIGH. Of these eight bits, five comprise the TRIGGER group (AUTO, LINE, or EXT OR SINGLE SWEEP), one is the **1 SECOND CONTROL** bit (subparagraph b above), one is the **SEQ SYNC DISABLE** bit, and one is the **EXT FM DISABLE** bit. The **EXT FM DISABLE** bit is not used on this PCB; it is decoded here and sent to the A10 PCB. The **SEQ SYNC DISABLE** bit is used to activate the Seq Sync Disable Logic circuit (Q7). Three bits of the 5-bit control group go to the Decoder (U19), where they are used to control the trigger source. These 3 control-group bits are decoded by U19 when the **L STRB** line goes TRUE (low) (subparagraph b above). Once enabled by the **L STRB** line, U19 is controlled by the **H RAMP IS TEN** line. This line signals when the sweep ramp has reached its top end (10 volts). When the line is TRUE (high), the ramp is at 10 volts. A chart showing the logic state of the **RAMP NOT DWELL** line for the various input signal logic states is given in Table 7-12.

The remaining signal in this block is **H RESET.** This signal line pulses HIGH (true) when the EXT OR SINGLE SWEEP pushbutton is pressed while a sweep is in progress. When TRUE, **H RESET** initiates a dwell and, when the dwell period is finished, causes Switch A to close. When Switch A closes, the sweep ramp starts climbing toward 10 volts at a fast rate. When the ramp reaches 10 volts, the **L RAMP IS TEN** line enables a new sweep to be initiated when the EXT OR SINGLE SWEEP pushbutton is again pressed.

Table 7-12. L RAMP NOT DWELL Logic States

STROBE U19-7	RAMP IS TEN U19-9	AUTO U19-15	LINE U19-10	EXT OR SINGLE SWEEP U19-A	RAMP NOT DWELL U19-6
1	X*	X	X	X	1
0	0	X	X	X	0
0	1	1	0	0	0
0	1	X	1	0	0 Only when triggered by Line Trigger Pulse Generator. (U19-13 = 1)
0	1	X	0	1	0 Only when Single Sweep Logic circuit (U17D) has detected one of the following: a. An external trigger pulse from the rear panel. (U17D-12 = 0) b. An activate single-sweep logic level from the front panel, via the microprocessor. (U17D-13 = 0)

* = Don't Care

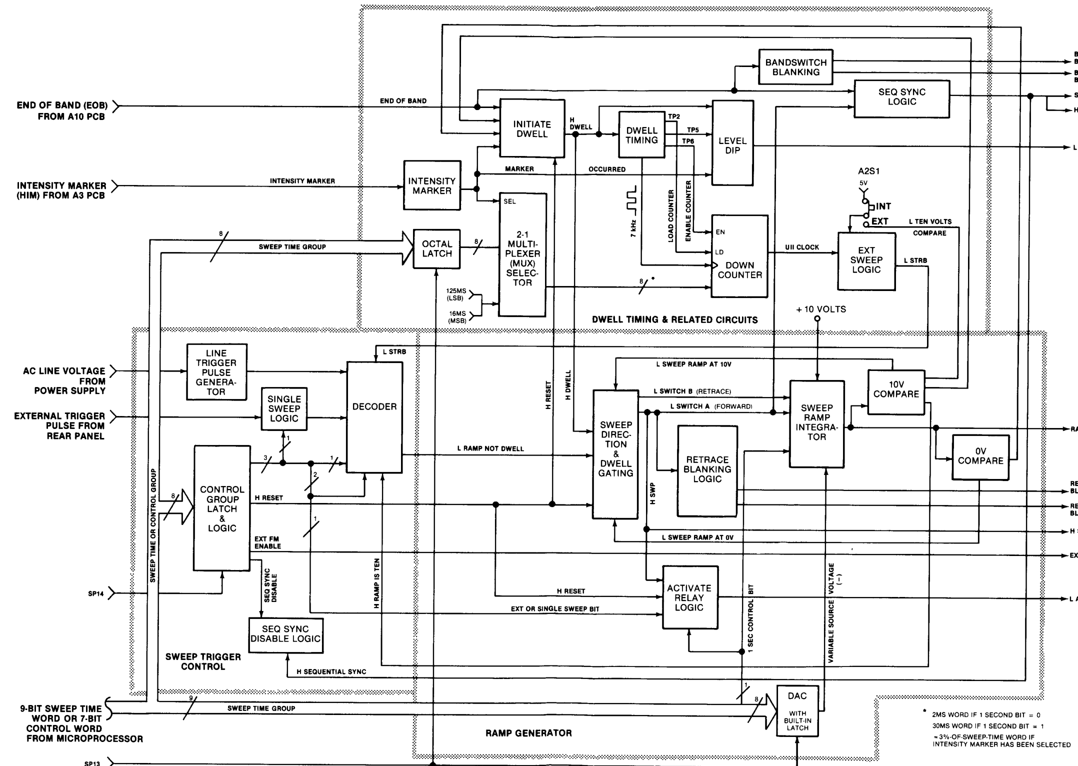


Figure 7-28. A2 Ramp Generator Functional Block Diagram

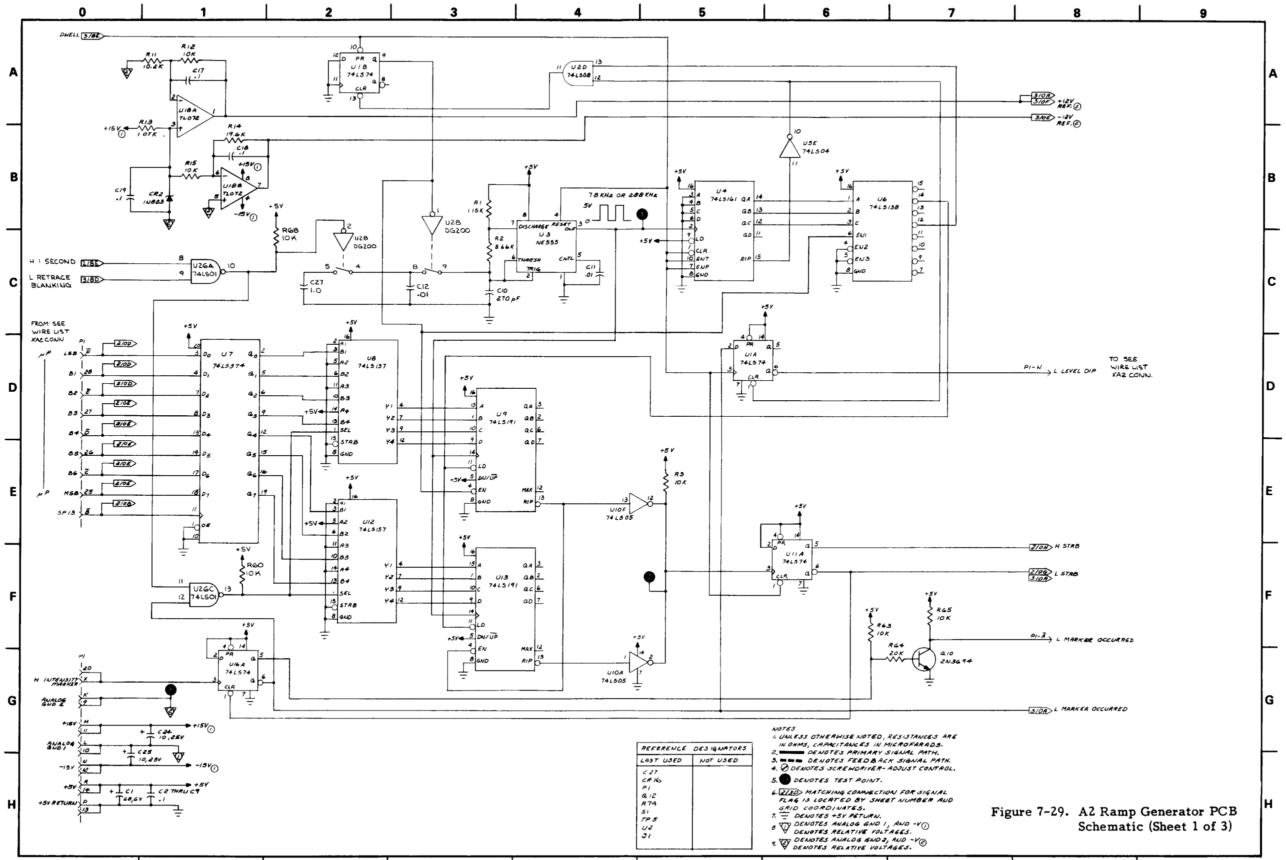
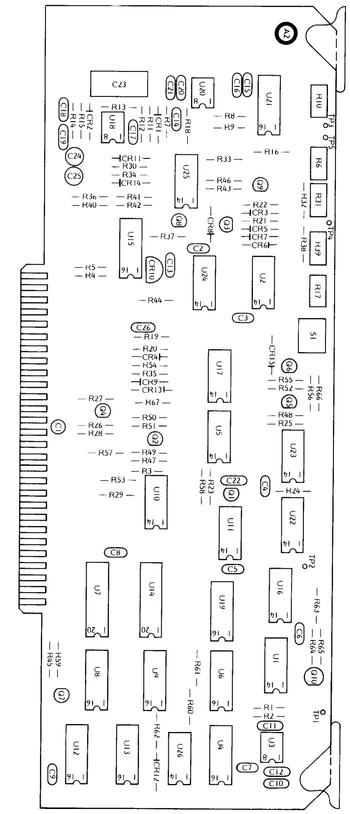


Figure 7-29. A2 Ramp Generator PCB Schematic (Sheet 1 of 3)



A2 PCB Parts Locator

Figure 7-29. (Sheet 1)

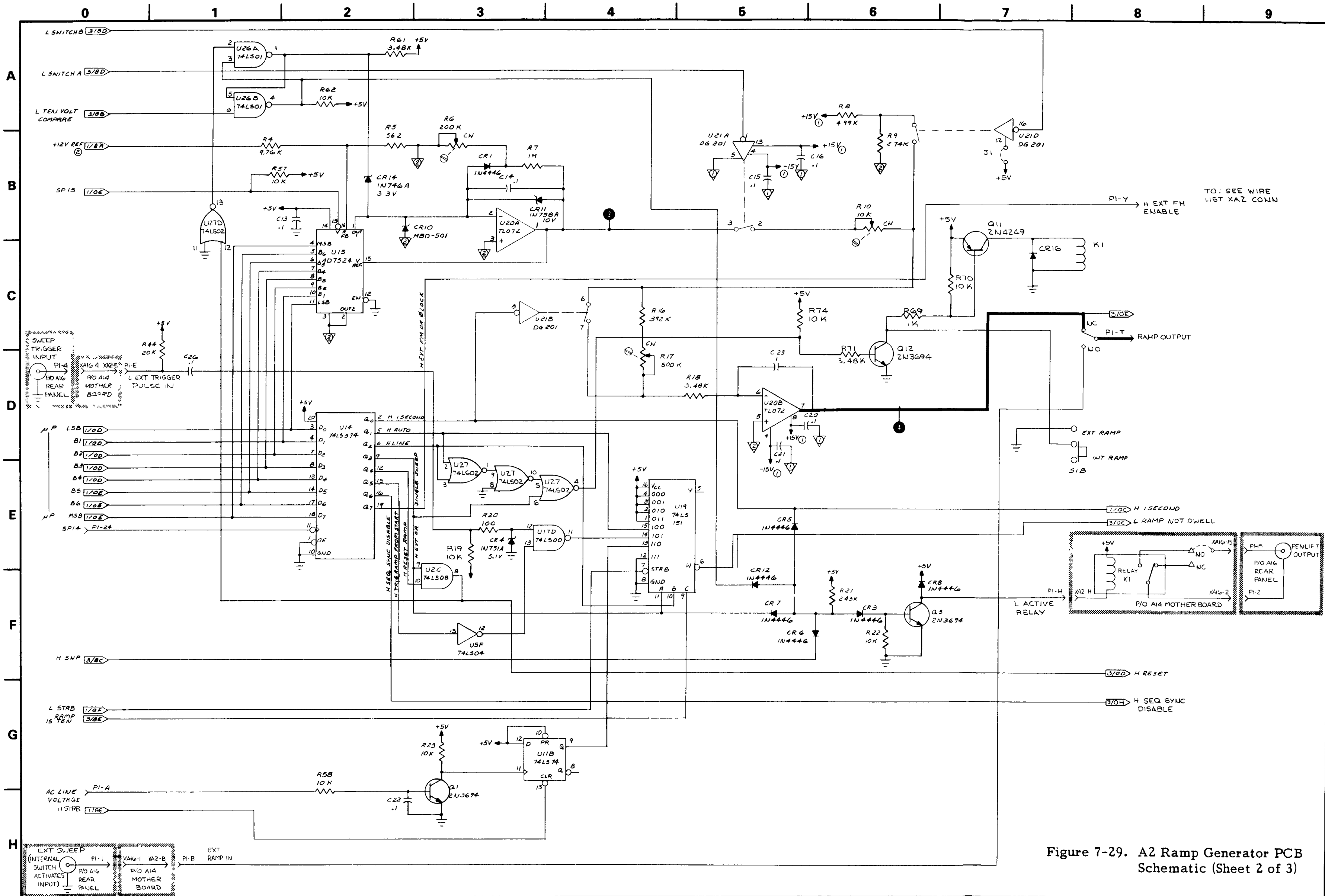


Figure 7-29. A2 Ramp Generator PCB Schematic (Sheet 2 of 3)

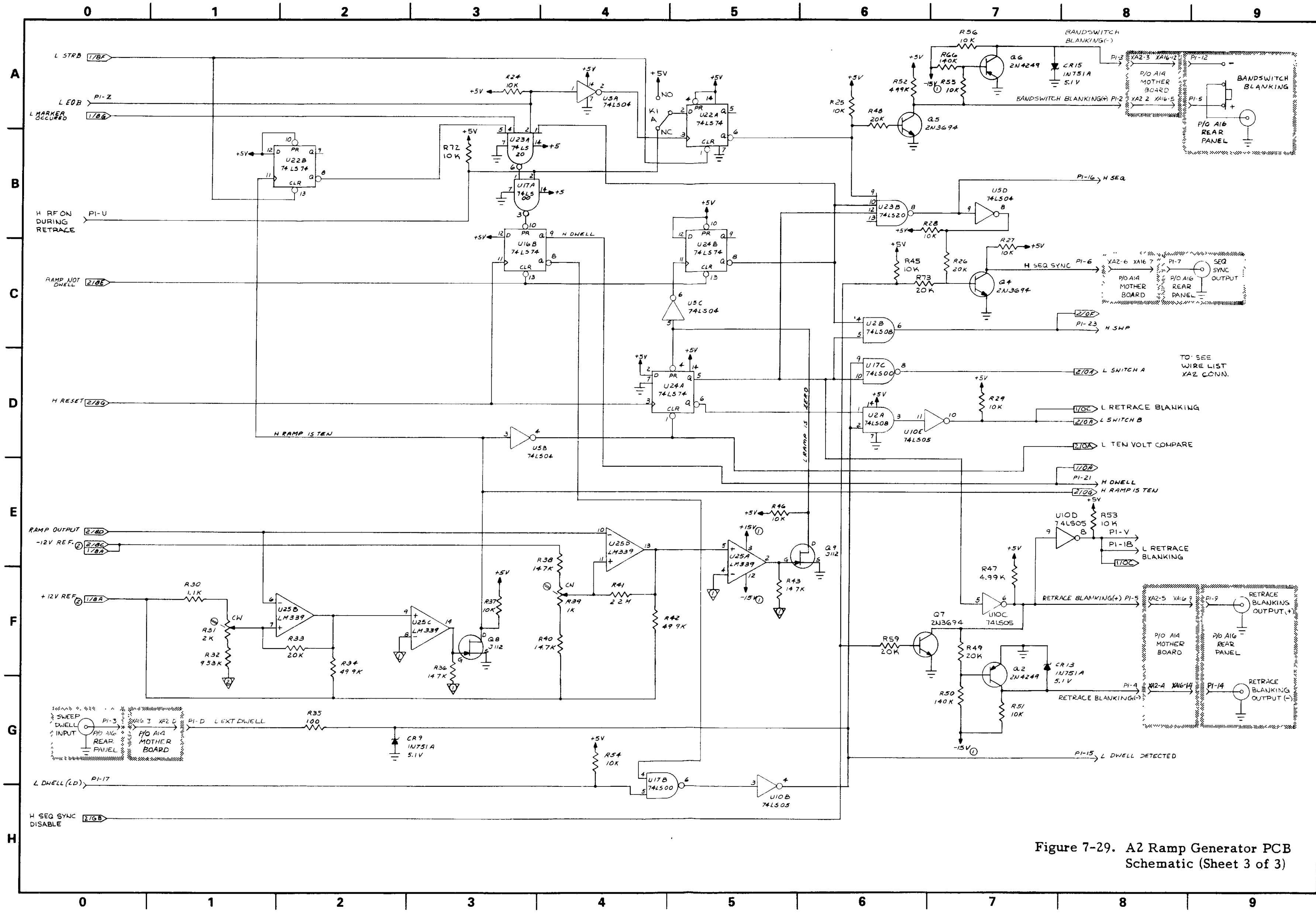
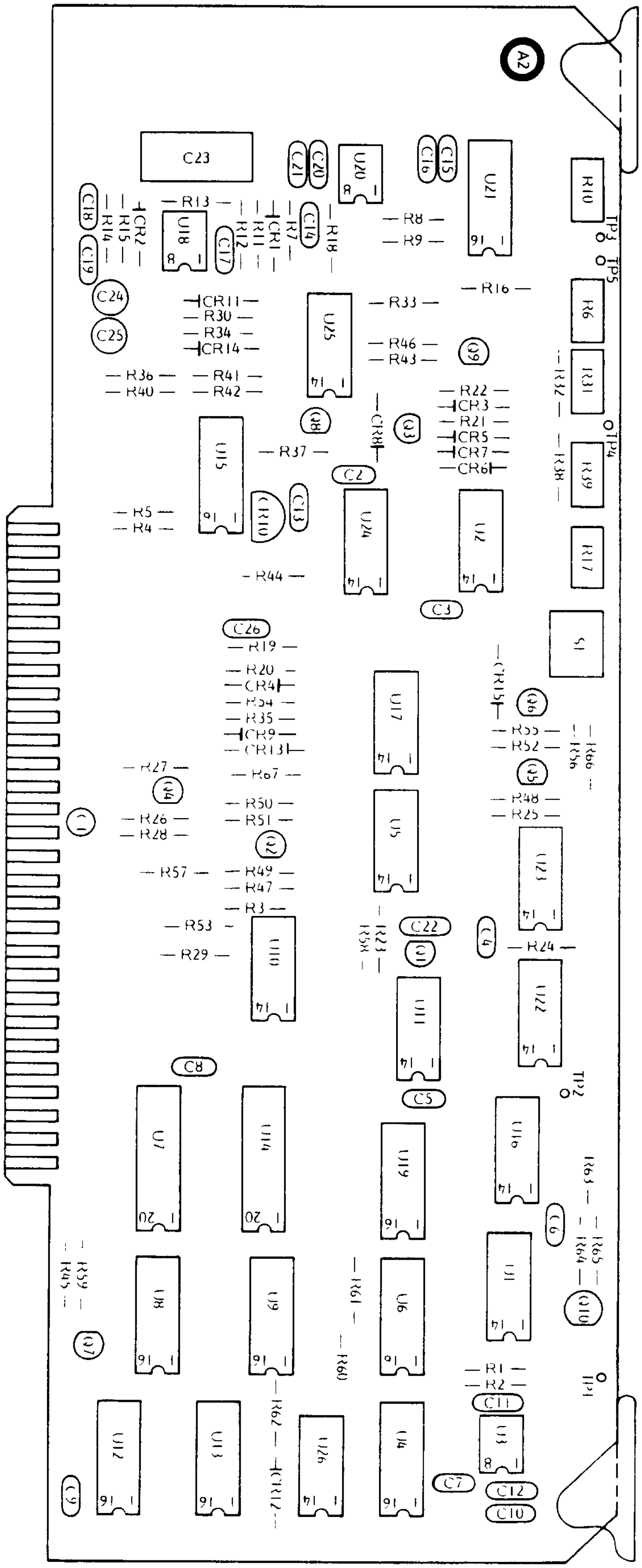


Figure 7-29. A2 Ramp Generator PCB Schematic (Sheet 3 of 3)

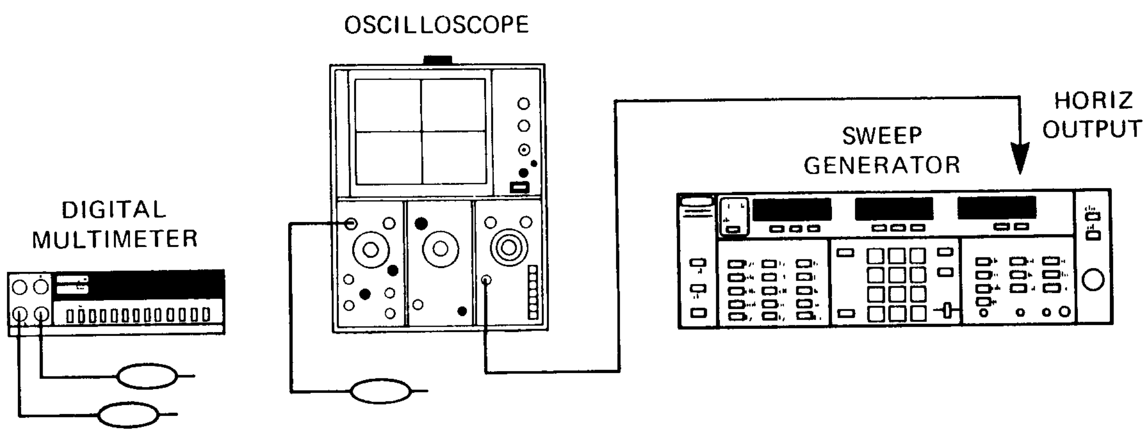


A2 PCB Parts Locator Diagram

7-9.2 A2 Ramp Generator PCB Troubleshooting Information and Data

Error code 21 reports on the status of the A2 Ramp Generator PCB. The microprocessor routine associated with this error code starts a sweep ramp, and then verifies that the ramp has occurred. The routine accomplishes this by starting an 8-ms ramp, and then – after a reasonable time – checking the **H SWP** and **L DWELL DETECTED** control lines. If the **H SWP** line has toggled from HIGH to LOW, a forward sweep has occurred. And if the **L DWELL DETECTED** line has toggled from LOW to HIGH, a retrace sweep has occurred.

The test setup for troubleshooting Error Code 21 is provided in Figure 7-30; the troubleshooting flowchart (2 sheets) is provided in Figure 7-31.



SWEEP GENERATOR CONTROL SETTINGS

FREQUENCY RANGE: FULL
TRIGGER: AUTO
MARKERS: VIDEO
LEVELING: INTERNAL
RETRACE RF: ON
RF: ON

RF SLOPE: OFF
LEVEL: 0 dBm
SWEEP TIME: 10 ms

Figure 7-30. Test Equipment Setup for Troubleshooting Error Code 21

GENERAL INSTRUCTIONS:

1. Check the following voltages before starting the flowchart:
   a. +5V - check at connector P1, pins R(+) and P(-).
   b. +15V - check at connector P1, pin M (reference measurement to pin L).
   c. -15V - check at connector P1, pin N (reference measurement to pin L).
2. Insure that the PCB-mounted INT-EXT switch (A2S1) is in INT.
3. Logic levels are TTL.

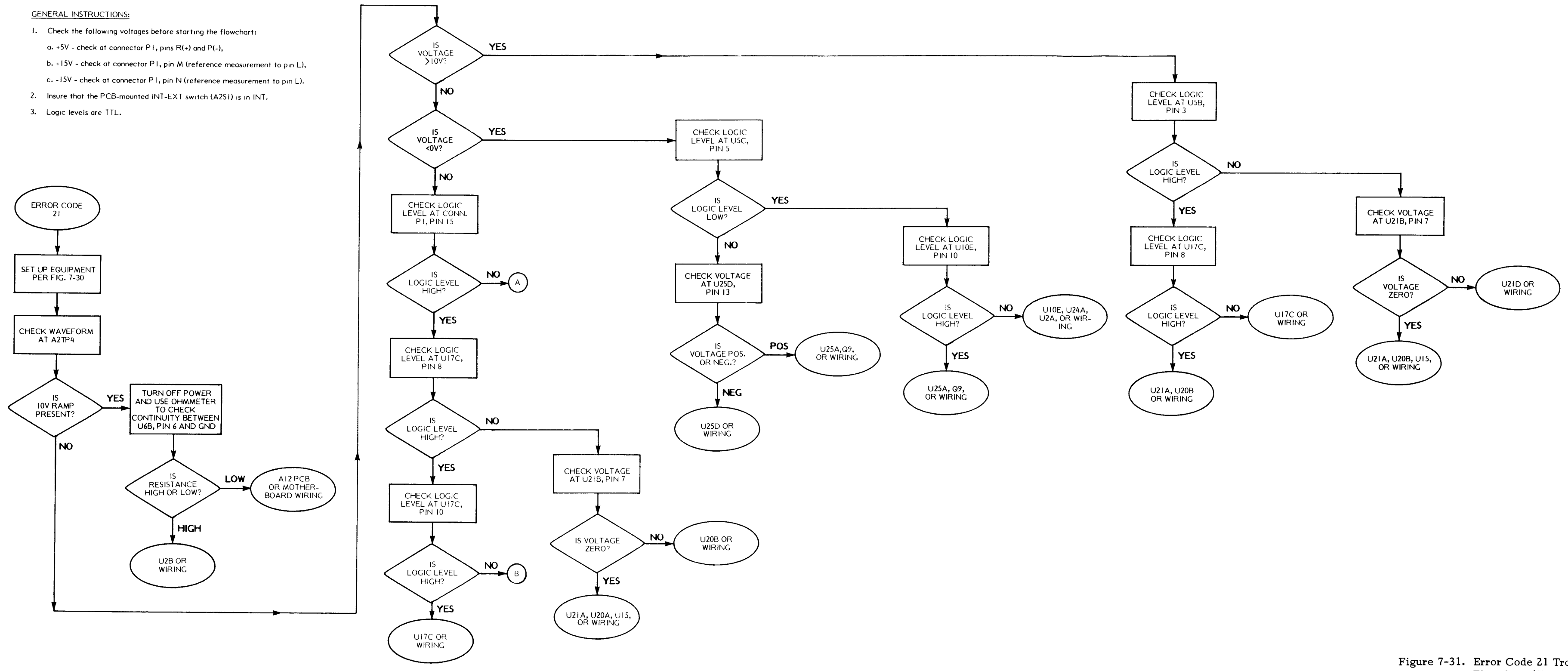


Figure 7-31. Error Code 21 Troubleshooting Flowchart (Sheet 1 of 3)

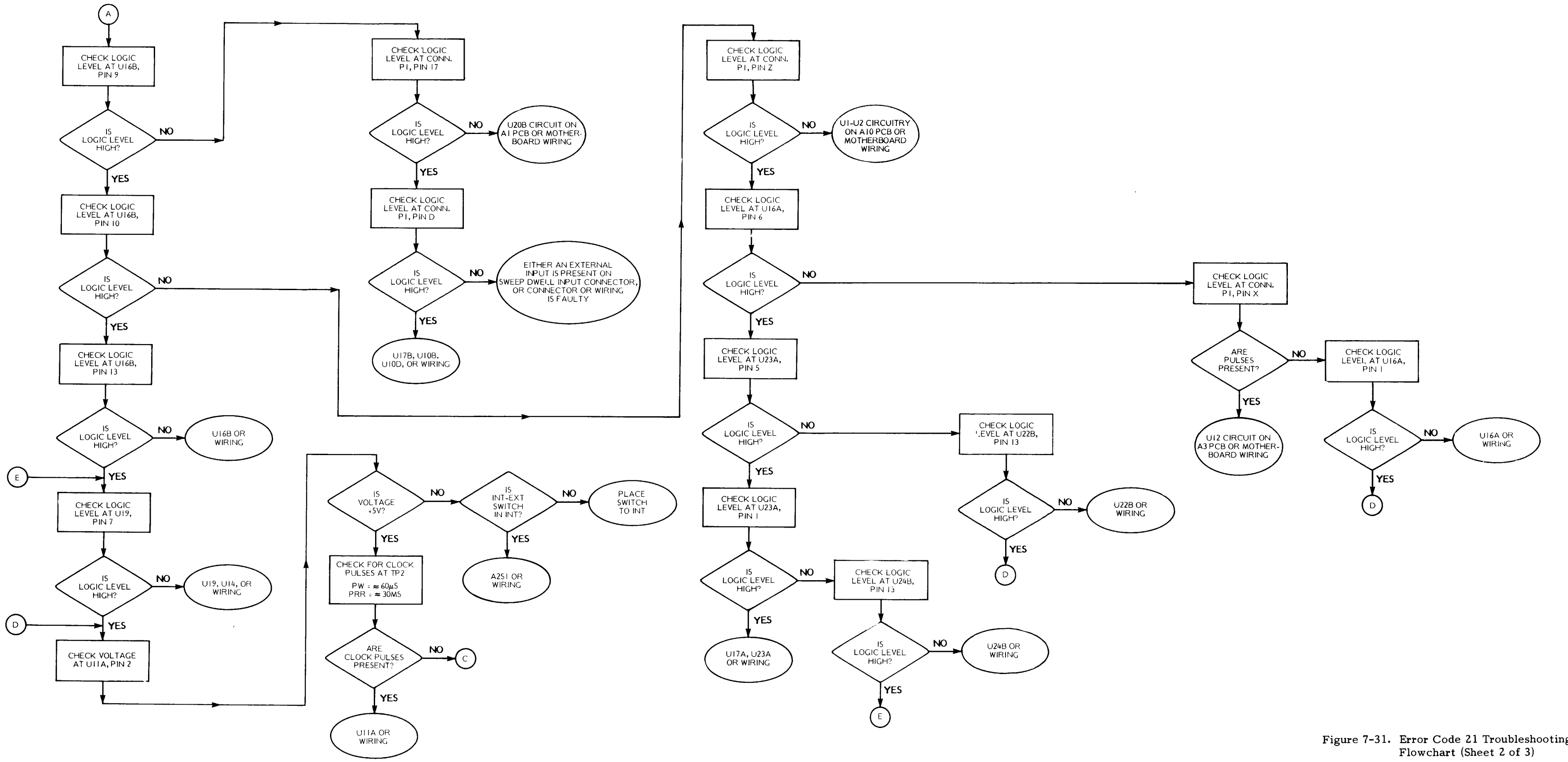


Figure 7-31. Error Code 21 Troubleshooting Flowchart (Sheet 2 of 3)

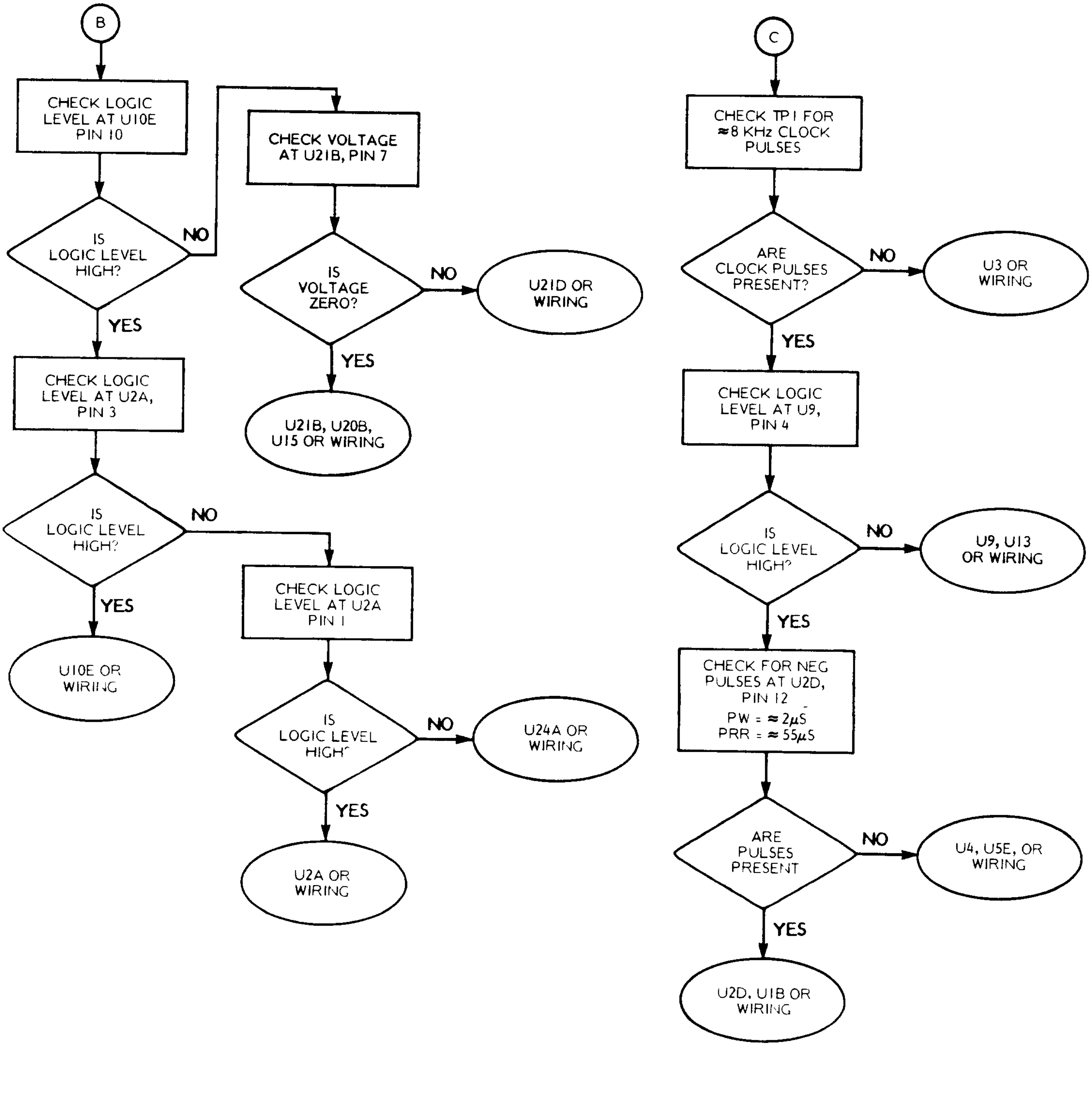


Figure 7-31. Error Code 21 Troubleshooting Flowchart (Sheet 3 of 3)

7-10 A3 MARKER GENERATOR PCB

7-10.1 A3 Marker Generator PCB Circuit Description

The A3 Marker Generator PCB generates the RF, Video, and Intensity markers. In addition, the PCB also contains the logic circuitry associated with the front panel INCREASE-DECREASE lever. A functional diagram of the marker generator circuitry is shown in Figure 7-32, and a similar diagram for the INCREASE-DECREASE lever logic circuitry is shown in Figure 7-33. The A3 PCB schematic diagram (4 sheets) is contained in Figure 7-34 and the circuits are described below.

a. Marker Generator Circuits. As shown in Figure 7-32, the inputs to the Marker Generator are a 0-10V sweep ramp from the A5 PCB and the retrace blanking control line from the A2 PCB, plus the data bus and several control lines from the A12 PCB. The 0-10V sweep ramp **(RAMP, 0-10V)** may be either the **RAMP OUT** signal from the A2 PCB, the **MAN SWEEP INPUT** from the front panel, or the Step Freq DAC signal (paragraph 3-7.2) from the A5 PCB. The inputs from the A12 PCB are as follows:

   1. three marker frequency (F0, M1, M2) 8-bit digital groups

   2. a 3-bit marker-mode and a 3-bit marker frequency disable control group

   3. four latch-clock control bits (SP9, SP10, SP11, SP12)

   4. three marker-identify control bits.

   The three marker-frequency digital groups represent either the preset marker frequencies (paragraph 3-2.7) or the marker frequencies selected using the front panel controls (paragraph 3-2.4).

   The three digital groups provide the inputs for the three digital-to-analog converter circuits (DACs) (U5-U8A, U6-U9A, U7-U10A). These DAC circuits have built-in latches. When the microprocessor clocks these DAC latches HIGH, the marker-frequency words are loaded and subsequently converted to discrete voltages between 0 and 10 volts. These voltages represent the marker's relative position within the band of frequencies being swept. For example, 3 volts would indicate the marker frequency is located approximately 1/3 of the way between the low and high ends of the band; 5 volts would indicate the marker frequency is located at the middle of the band; and 10 volts would indicate the marker frequency is located at the high end of the band. These marker frequency voltages are applied to the Marker Comparator circuits.

   The Marker Comparator circuits (U8D, U9D, U10D) effectively compare the marker-frequency voltages with the **RAMP, 0-10V**, signal. The output of each comparator is a steeply-sloping ramp with voltage excursions between -13.5 and +13.5 volts. The midpoints (0V) on these ramps are the comparison points, that is, the points at which the instantaneous voltages of the sweep ramps equal the marker-frequency voltages from the DACs. The **F0**, **M1**, and **M2** ramps are applied to the Absolute Value circuits.

   The Absolute Value circuits (U10C, U9B, U10B) change the **F0**, **M1**, and **M2** ramps into triangular waveforms, on which the apexes represent the respective marker's location. The usable portion of these waveforms, after being offset, varies between 0 and +5 volts. The 0-5V signals are applied to the marker output circuits, via the marker-frequency disable logic circuits (Q4, Q5, Q6).

   The marker-frequency disable-logic circuits are controlled respectively by the **H F0 DISABLE, H M1 DISABLE**, and **H M2 DISABLE** control lines. These control lines come from the Marker Select and Control latch and logic circuits (U1, U2D, U2C, U2B). If the microprocessor disables a marker or if a marker-frequency front panel pushbutton (F0, M1, M2) is pressed, the respective marker disable

7-10.1 cont.

control line is set TRUE (high). When TRUE, these lines cause their respective marker's Absolute Value circuit output to be shunted to ground.

The 0-5V signals from the Absolute Value circuits are applied, via the MARKER AMPLITUDE control to the RF and Video Marker Output circuits. The control inputs to these output circuits are the **H RF MARKER ENABLE** and the **H VIDEO MARKER ENABLE** lines from the Mode Enable Logic circuits (U11C, U11D). If the MARKERS - RF pushbutton is engaged and a forward frequency sweep is in progress (**L RETRACE BLANKING** is FALSE), the **H RF MARKER ENABLE** line will be TRUE (high). When this line is TRUE, the output of the RF Marker Output circuit (U8B) will be a 0-5V analog signal. The actual amplitude of this signal will depend on the MARKER AMPLITUDE control setting. This 0-5V signal is applied to the A4 Automatic Level Control PCB, where it causes a "dip" in the RF output power level. If the MARKERS -VIDEO push-button is engaged, the Video Marker Output circuit (U9C) operation is the same as described for RF. The output of the video marker circuit is applied to the rear panel MARKER OUTPUT connector.

The 0-5V signals from the Absolute Value circuits are also applied directly to the Intensity Marker Output circuit (U12). The operation of the Intensity Marker Output circuit is similar to that described for the RF marker circuit, above. If MARKERS - INTENSITY is engaged and a forward sweep is in progress, the output of the intensity marker circuit will go HIGH when a marker is encountered. This HIGH is applied to the A2 Ramp Generator PCB, where it causes the A2-generated sweep ramp to dwell.

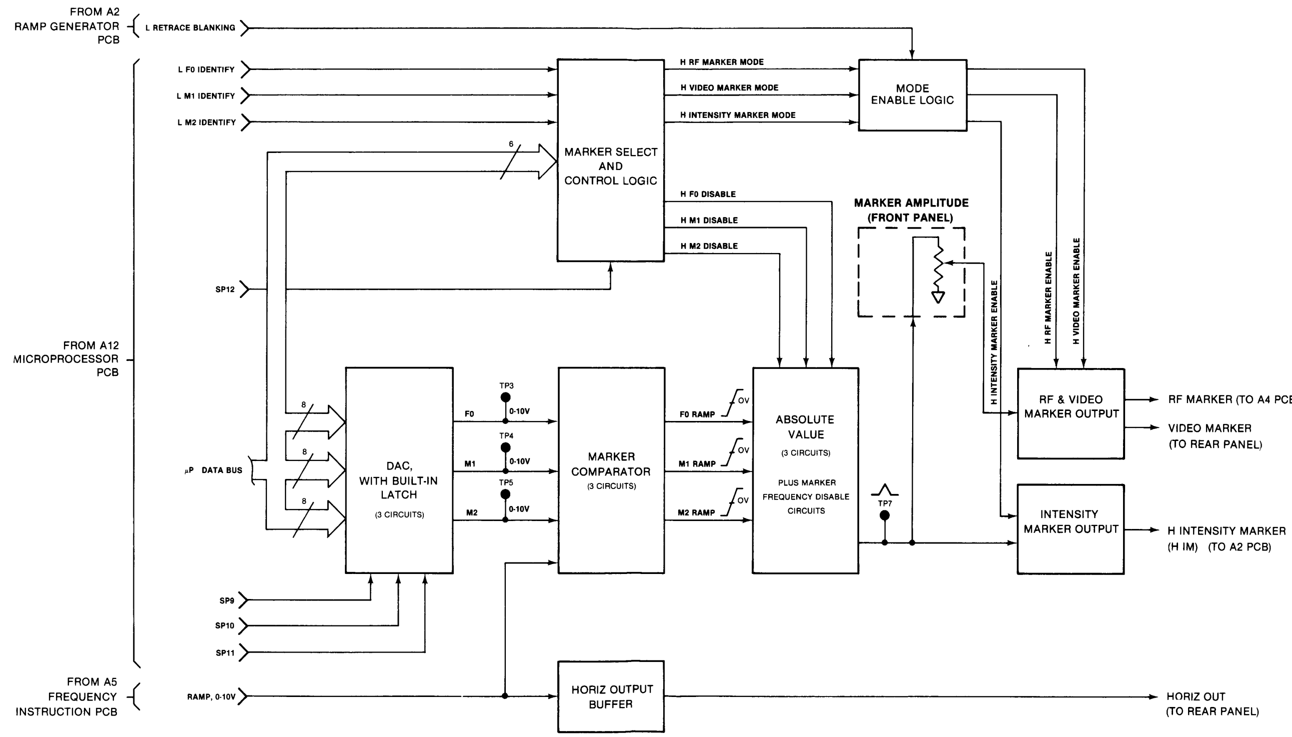


Figure 7-32. A3 PCB Marker Generator Functional Block Diagram

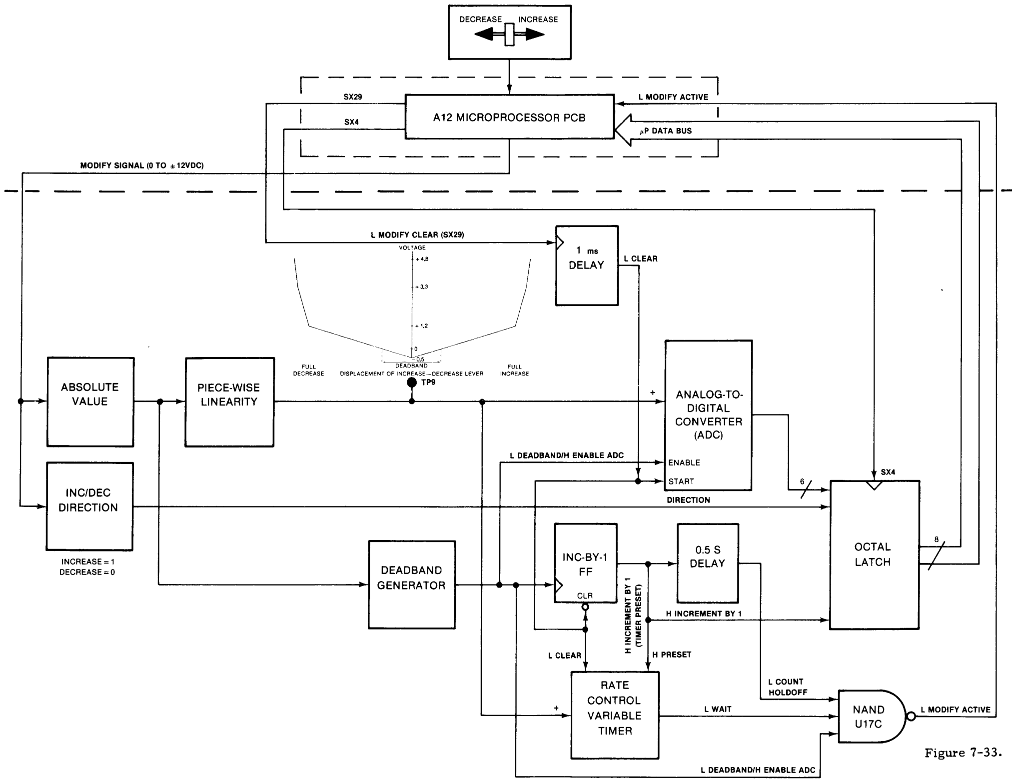


Figure 7-33. A3 PCB INCREASE-DECREASE Logic Circuit Functional Block Diagram

b. INCREASE-DECREASE Lever Logic Circuitry. This circuitry performs two distinct functions, as follows:

1. When the INCREASE-DECREASE lever is "tapped", the circuit causes the microprocessor to increase or decrease the value of the selected parameter (paragraph 3-2.1a) in one-increment steps.

2. When the INCREASE-DECREASE lever is moved to either side from center, the circuit causes the microprocessor to increase or decrease the value of the selected parameter at a variable rate. This rate depends upon lever displacement.

The first function the circuit performs is to increase or decrease the selected parameter's value in one increment steps. As shown in Figure 7-33, the INCREASE-DECREASE lever logic circuitry is connected in a control loop with the A12 Microprocessor PCB. The INCREASE-DECREASE lever itself is connected to the A12 PCB. This lever controls, via circuitry on the A12 PCB, the voltage level of the **MODIFY SIGNAL** input line to the A3 PCB. When the lever is moved from its center position, the **MODIFY SIGNAL** line's voltage value is between either 0 and -12 Vdc or 0 and +12 Vdc. The voltage's polarity and value depend on the direction and length of INCREASE-DECREASE lever displacement. Displacement in the DECREASE direction yields a positive voltage, and displacement in the INCREASE direction yields a negative voltage. This 0 to ±12 Vdc voltage goes to two places on the A3 PCB: the Absolute Value and the Inc/Dec Direction circuits.

At the Inc/Dec Direction circuit (U14B, Q2), the 0 to ±12 Vdc signal is translated into either a logic 1 or a logic 0, depending upon the voltage's polarity. If its polarity is negative, the logic level is a 1; conversely, if positive, the logic level is a 0. The output of this circuit (**DIRECTION** signal line) is applied to the Octal Latch (U19), where it waits to be clocked out to the microprocessor.

At the Absolute Value circuit (U13A), the 0 to ±12 Vdc signal is changed to a positive voltage when the INCREASE-DECREASE lever is moved either direction from center. (The circuit-output voltage is slightly negative when the lever is at its center (rest) position.) One portion of this signal goes to the Piece-wise Linearity circuit; the other goes to the Deadband Generator circuit.

The purpose of the Deadband Generator circuit (U14A, Q1) is to keep the logic circuitry inactive when the INCREASE-DECREASE lever is in its center position. When the lever is moved from center, the positive output of the Absolute Value circuit causes the **L DEADBAND/H ENABLE ADC** control line to go HIGH. This control line serves the following purposes:

(a) When the **L DEADBAND/H ENABLE ADC** line transitions from LOW to HIGH, it clocks the **H INCREMENT BY 1 (TIMER PRESET)** control line HIGH. When HIGH, this line presets the Rate Control Variable Timer circuit (U13B, U14D, U14C, Q3), which sets the **L WAIT** control line HIGH. Also, the HIGH state of the **H INCREMENT BY 1** control line provides the logic input for the most-significant bit (MSB) of the Octal Latch.

(b) When the **L DEADBAND/H ENABLE ADC** line goes HIGH, it provides an enabling logic level to the Analog-to-Digital Converter (ADC) circuit (U18, U17A, U17B); it also enables one "leg" of NAND gate U17C.

The U17C NAND gate has three inputs: **L WAIT, L DEADBAND/H ENABLE ADC,** and **L COUNT HOLDOFF**. As already described, the first two inputs have been set HIGH; the third input, **L COUNT HOLDOFF**, is normally HIGH. Now, with all three U17C inputs HIGH, the **L MODIFY ACTIVE** line goes LOW (true). When the microprocessor senses that L

Figure 7-33.

MODIFY ACTIVE is LOW, it uses **SX4** to clock the Octal Latch. When clocked, the Octal Latch outputs an 8-bit digital word. If the MSB of this word is a 1, the microprocessor increases or decreases (depending on the **DIRECTION** bit) the selected parameter by 1 increment. After performing this incremental function, the microprocessor uses **SX29** to clear the logic circuitry by clocking the 1 ms Delay circuit.

The 1 ms Delay circuit (U16B) generates the 1 ms **L CLEAR** pulse. This pulse goes several places. At the ADC circuit, the **L CLEAR** pulse is inverted and then ANDed with the **L DEADBAND/H ENABLE ADC** logic level. The signal resulting from this ANDing process starts the ADC voltage conversion cycle. Once a conversion is done, U18 pin 5 goes LOW and triggers another conversion cycle. This repetitive triggering process keeps the ADC free-running as long as the **L DEADBAND/H ENABLE ADC** line stays HIGH. And this line will stay HIGH until the INCREASE-DECREASE lever is returned to its center position.

In addition to getting an ADC conversion started, the **L CLEAR** pulse has two other functions: it resets the Inc-by-1 FF, and it clears the Rate Control Variable Timer circuit.

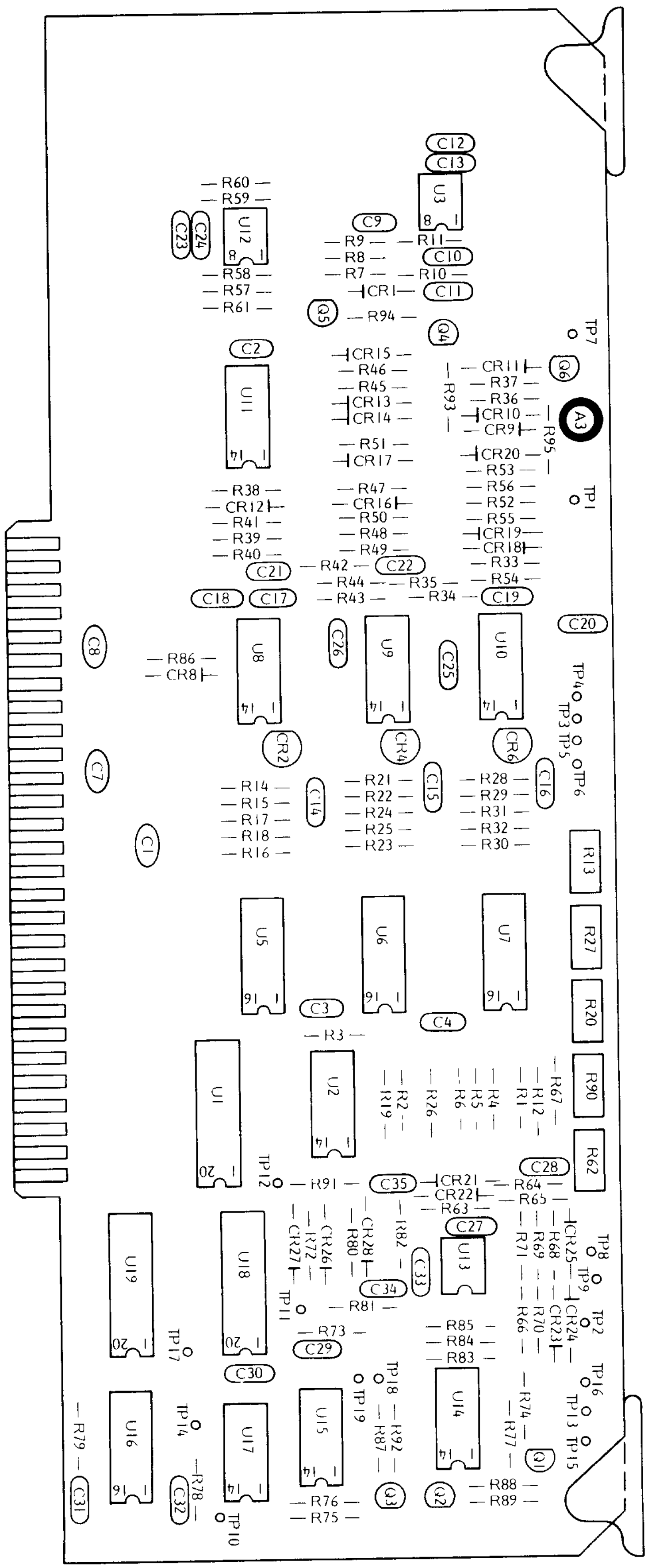
When reset, the HIGH to LOW transition of the Inc-By-1 FF Q-output clocks the **L COUNT HOLDOFF** control line TRUE. The TRUE state of this line causes the **L MODIFY ACTIVE** line to go FALSE and stay that way for about 0.5 seconds.

When cleared, the Rate Control Variable Timer circuit returns the **L WAIT** control line to its TRUE state. The increment-by-1 function is thus completed. Now, if the INCREASE-DECREASE lever has been moved and held rather than just "tapped", the circuit is primed for its second (variable rate) function.

To begin the discussion of the second function, go back to the Absolute Value circuit. As mentioned earlier, a portion of this circuit's output voltage goes to the Piece-wise Linearity circuit (R70, CR24-CR25-R69, CR23-R68, R71). This circuit is a three-piece voltage divider. The circuit provides the velocity breakpoints that can be observed as the lever is moved. These breakpoints (+1.2, +3.3, and +4.8 volts) are shown in the voltage/lever-displacement diagram above TP9. Although not drawn to scale horizontally, this diagram suggests the relationship that exists between the displacement of the lever and the speed with which the selected parameter increases or decreases.

The voltage at TP9 provides both the input for the ADC circuit, and the input for the Rate Control Variable Timer circuit.

The purpose of the Rate Control Variable Timer circuit is to slow down the count when the INCREASE-DECREASE lever is moved by only a small amount. The timer circuit uses a voltage-integrator RC (resistor-capacitor) network to form a timing ramp. When the velocity voltage at TP9 is low, the RC network capacitor takes a long time to charge; hence, the circuit produces a long time-delay. As the voltage at TP9 increases, the capacitor charges more quickly and the timer-circuit delay time becomes shorter.



A3 PCB Parts Locator Diagram PCB

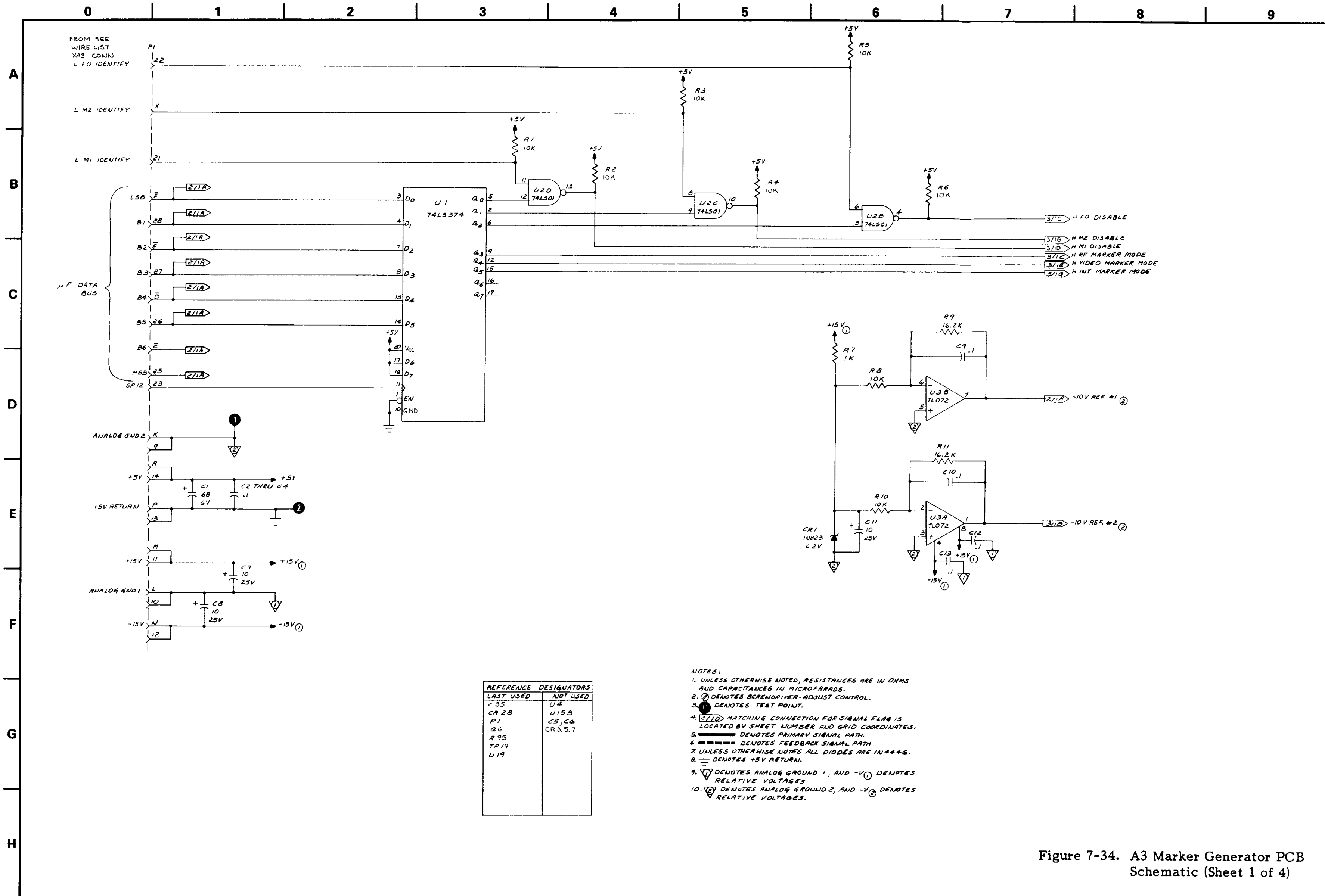


Figure 7-34. A3 Marker Generator PCB Schematic (Sheet 1 of 4)

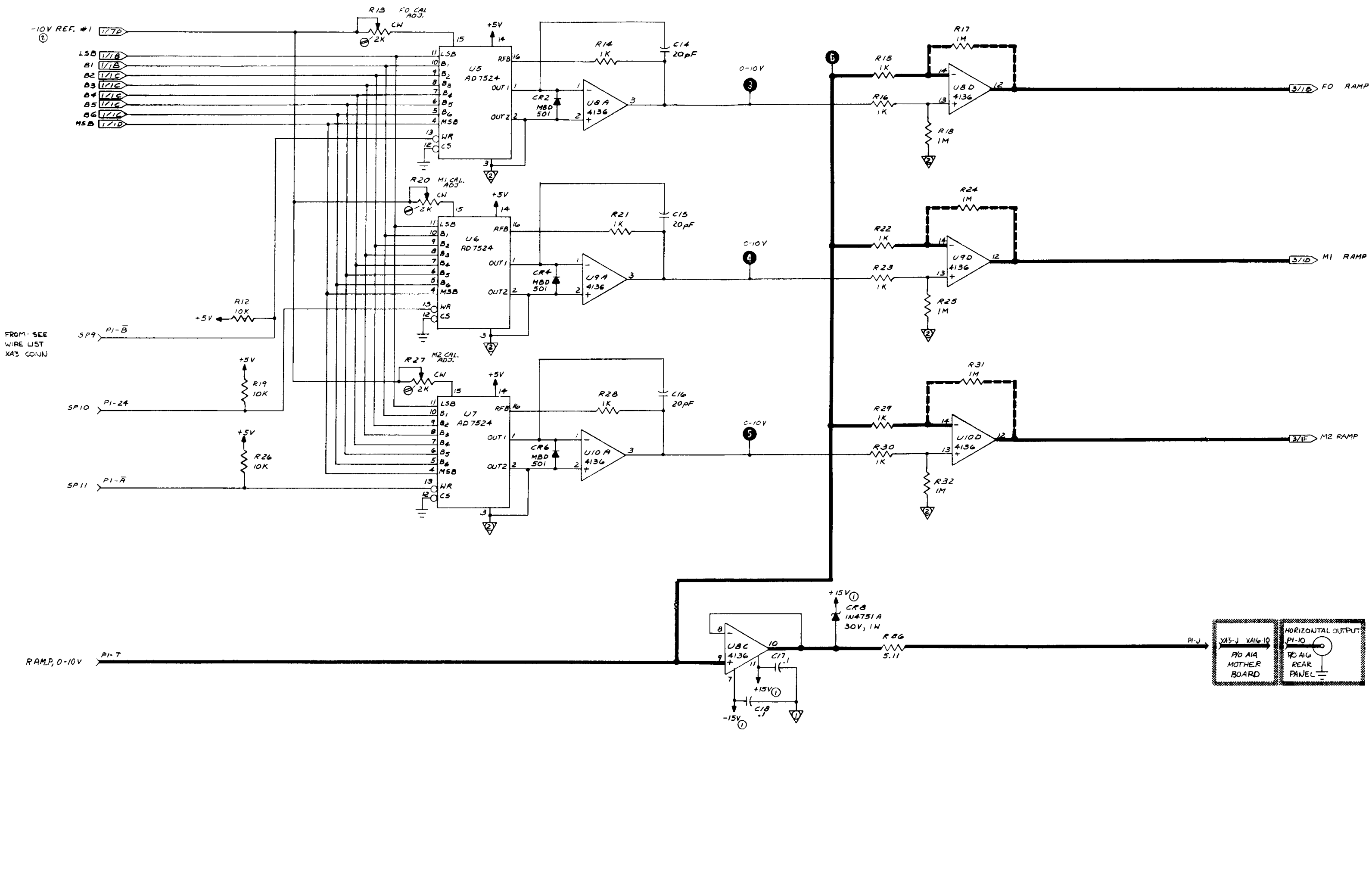


Figure 7-34. A3 Marker Generator PCB Schematic (Sheet 2 of 4)

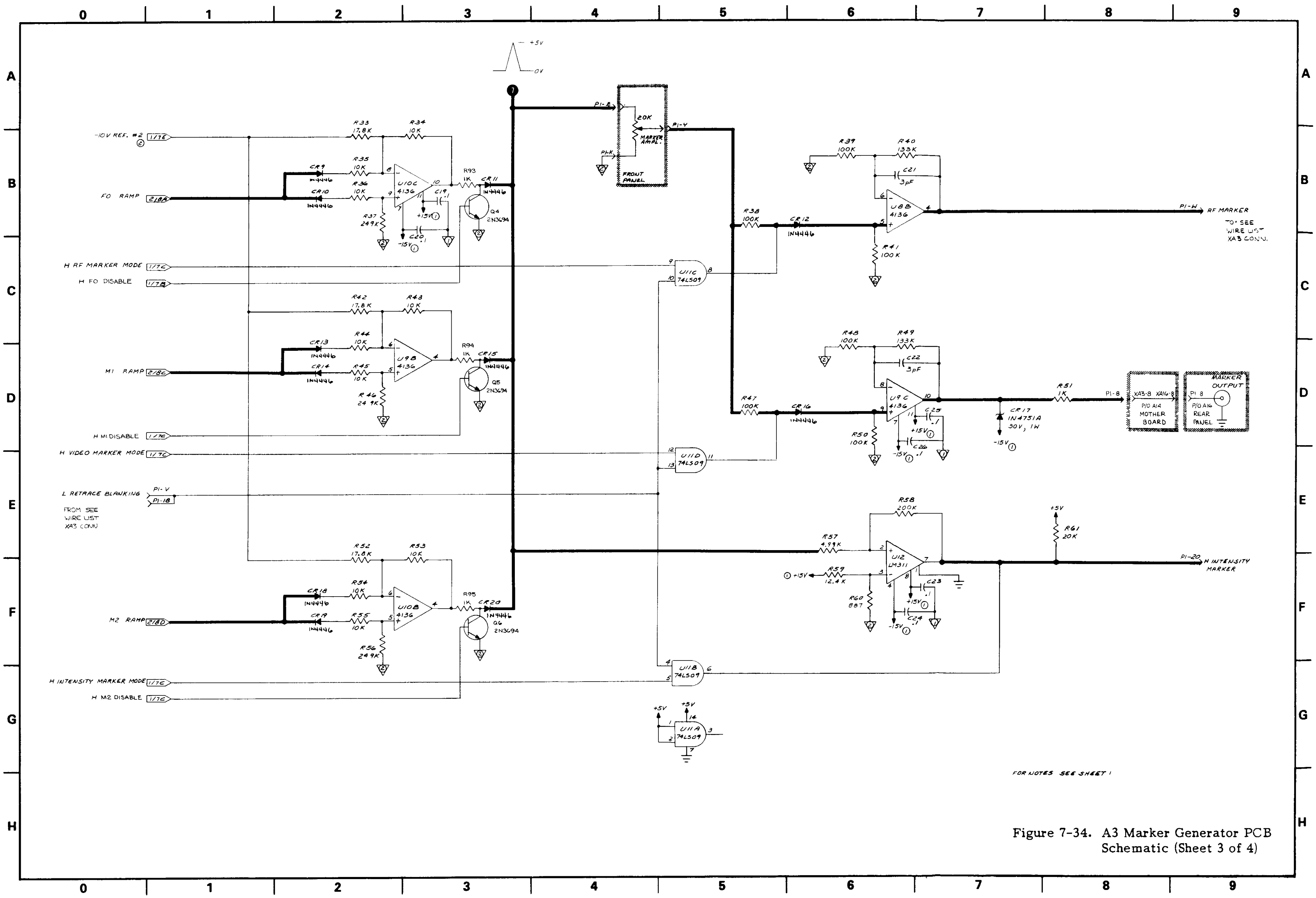


Figure 7-34. A3 Marker Generator PCB Schematic (Sheet 3 of 4)

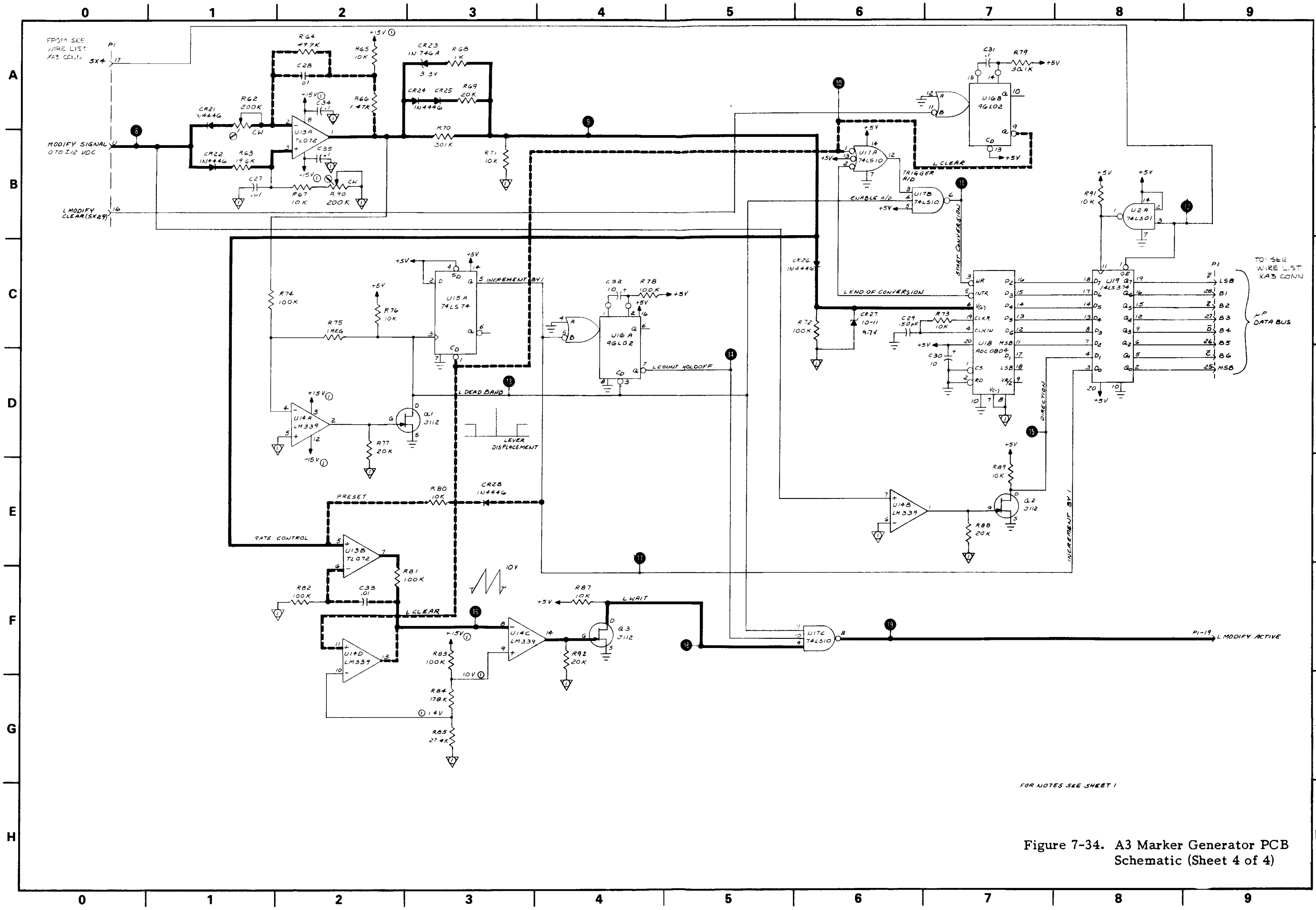


Figure 7-34. A3 Marker Generator PCB Schematic (Sheet 4 of 4)

7-10.2 A3 Marker Generator PCB Troubleshooting Information and Data

Error Code 22 reports on the status of the A3 Marker Generator PCB. The microprocessor routine associated with this error code performs the A3 PCB test in the following manner:

a. It positions the A3 marker frequencies as follows:

   1. M1 to a frequency point equal to 25% of the sweep width.

   2. F0 to a frequency point equal to 50% of the sweep width.

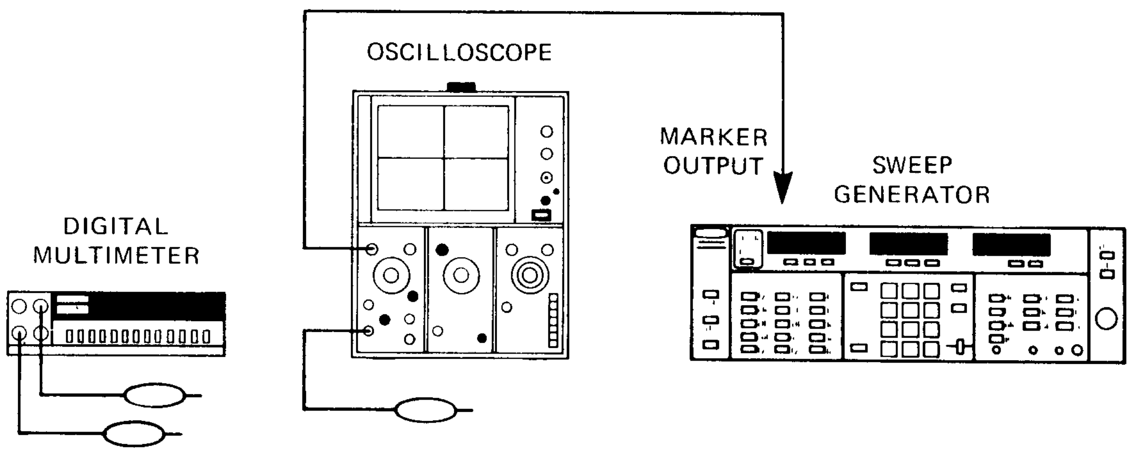
   3. M2 to a frequency point equal to 75% of the sweep width.

b. It selects the Intensity Markers on A3, the A2 Sweep Ramp on A5, and CW Filter Out on A5.

c. It sets the A2 sweep ramp for a 8-ms sweep and selects AUTO triggering.

d. It counts the markers during the forward sweep period; if three markers are not counted, the routine causes "Error 22" to be displayed.

The test setup for troubleshooting Error Code 22 is provided in Figure 7-35, the troubleshooting flowchart is in Figure 7-36, and the troubleshooting block diagram is in Figure 7-37.

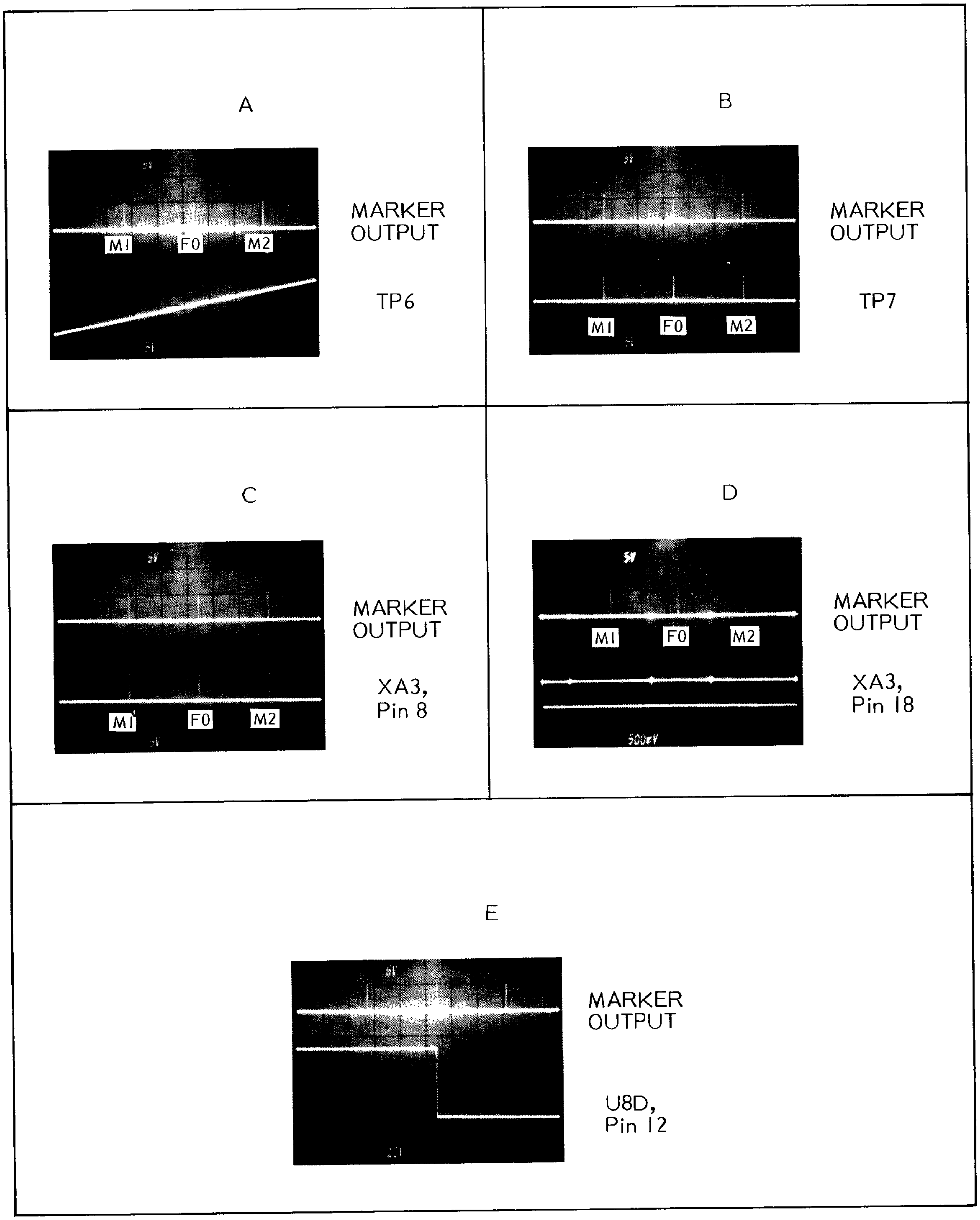


SWEEP GENERATOR CONTROL SETTINGS

FREQUENCY RANGE: FULL
TRIGGER: AUTO
MARKERS: VIDEO
LEVELING: INTERNAL
MARKER AMPLITUDE: Fully CW
LEVEL: 0 dBm
SWEEP TIME: 10 ms

RETRACE RF: ON
RF ON: ON
RF SLOPE: OFF
M1: 5 GHz
F0: 10 GHz
M2: 15 GHz

Figure 7-35. Test Equipment Setup for Troubleshooting Error Code 22



A3 Marker Generator PCB Waveforms (part of Figure 7-36)

GENERAL INSTRUCTIONS

1. Check the following dc voltages before starting the flowchart:
   a. +5V - P1, pins R(+) and P(-)
   b. +15V - P1, pin M (reference measurement to pin L)
   c. -15V - P1, pin N (reference measurement to pin L)
2. Logic levels are TTL.

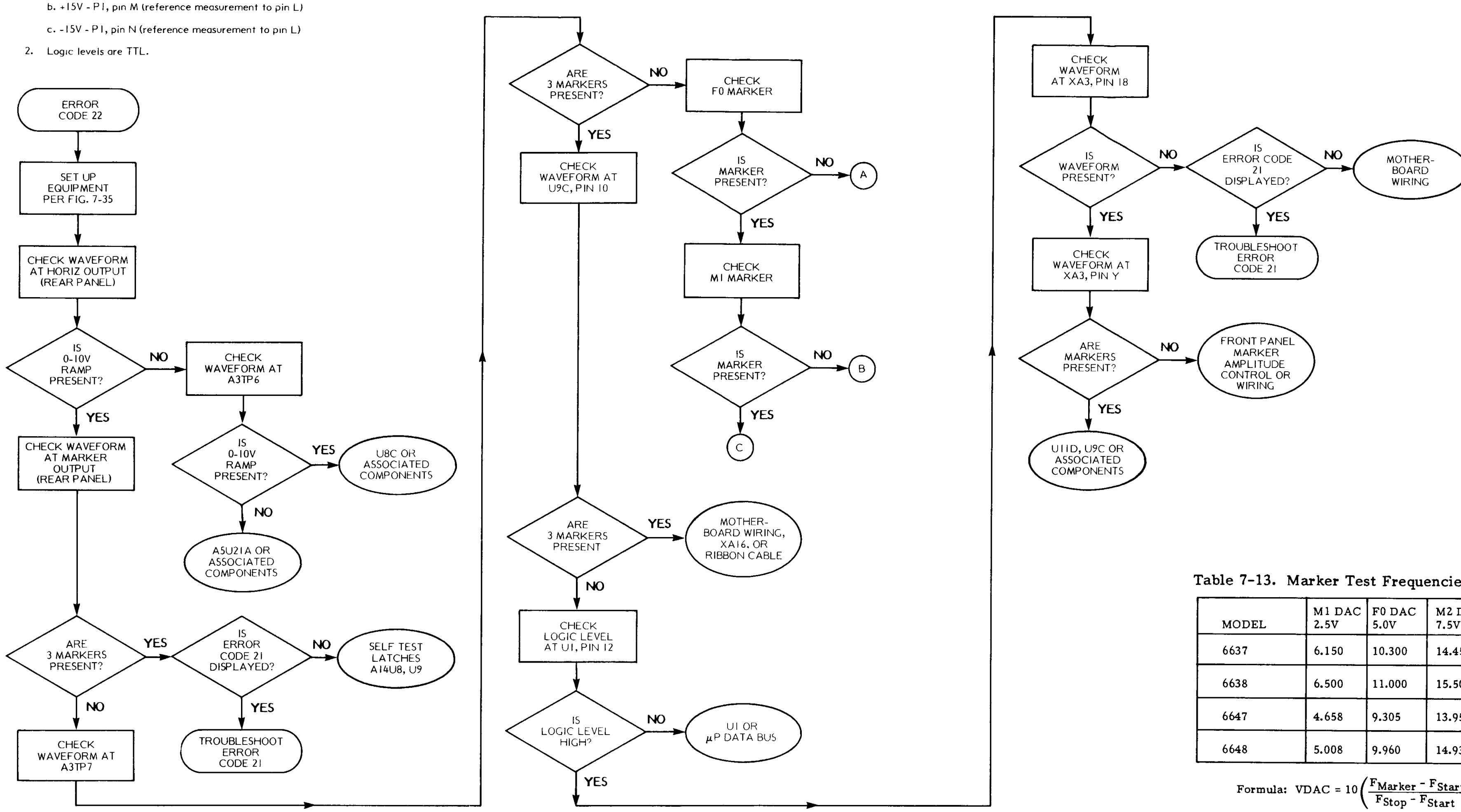


Table 7-13. Marker Test Frequencies (GHz)

MODEL	M1 DAC 2.5V	F0 DAC 5.0V	M2 DAC 7.5V
6637	6.150	10.300	14.450
6638	6.500	11.000	15.500
6647	4.658	9.305	13.953
6648	5.008	9.960	14.935

Formula: $VDAC = 10\left(\frac{F_{Marker} - F_{Start}}{F_{Stop} - F_{Start}}\right)$

Figure 7-36. Error Code 22 Troubleshooting Flowchart (Sheet 1 of 3)

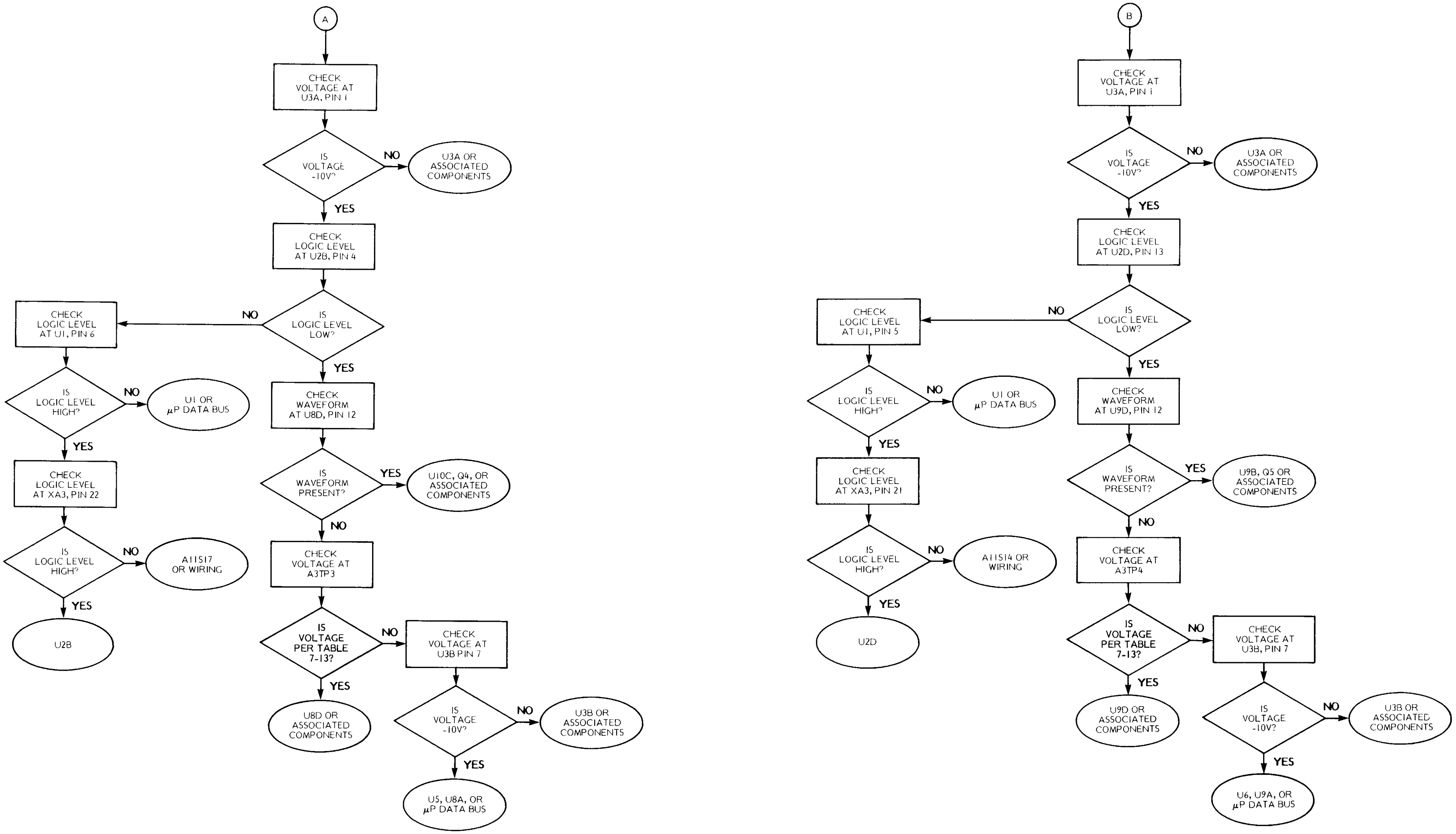


Figure 7-36. Error Code 22 Troubleshooting Flowchart (Sheet 2 of 3)

Figure 7-36(A).

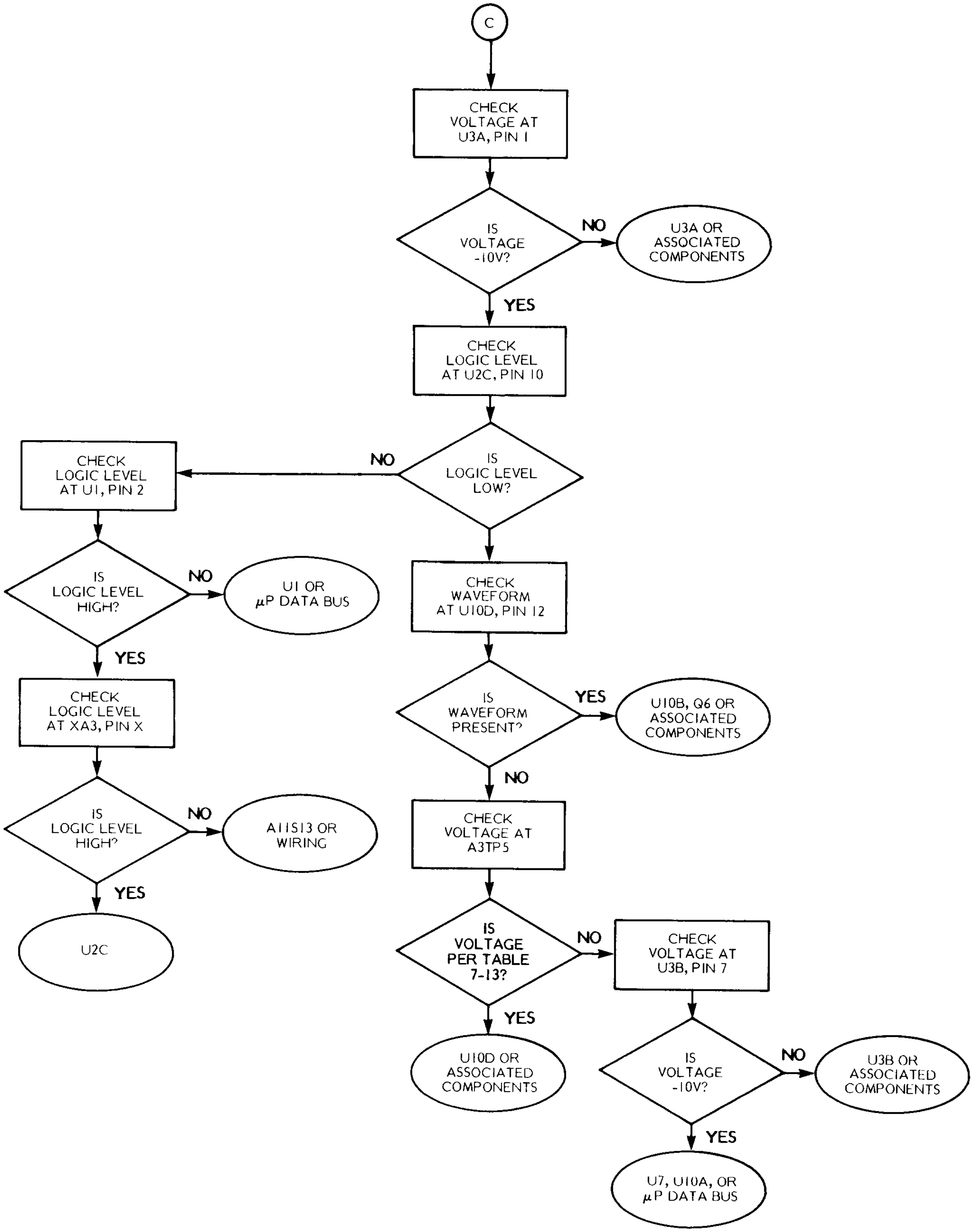


Figure 7-36. Error Code 22 Troubleshooting Flowchart (Sheet 3 of 3)

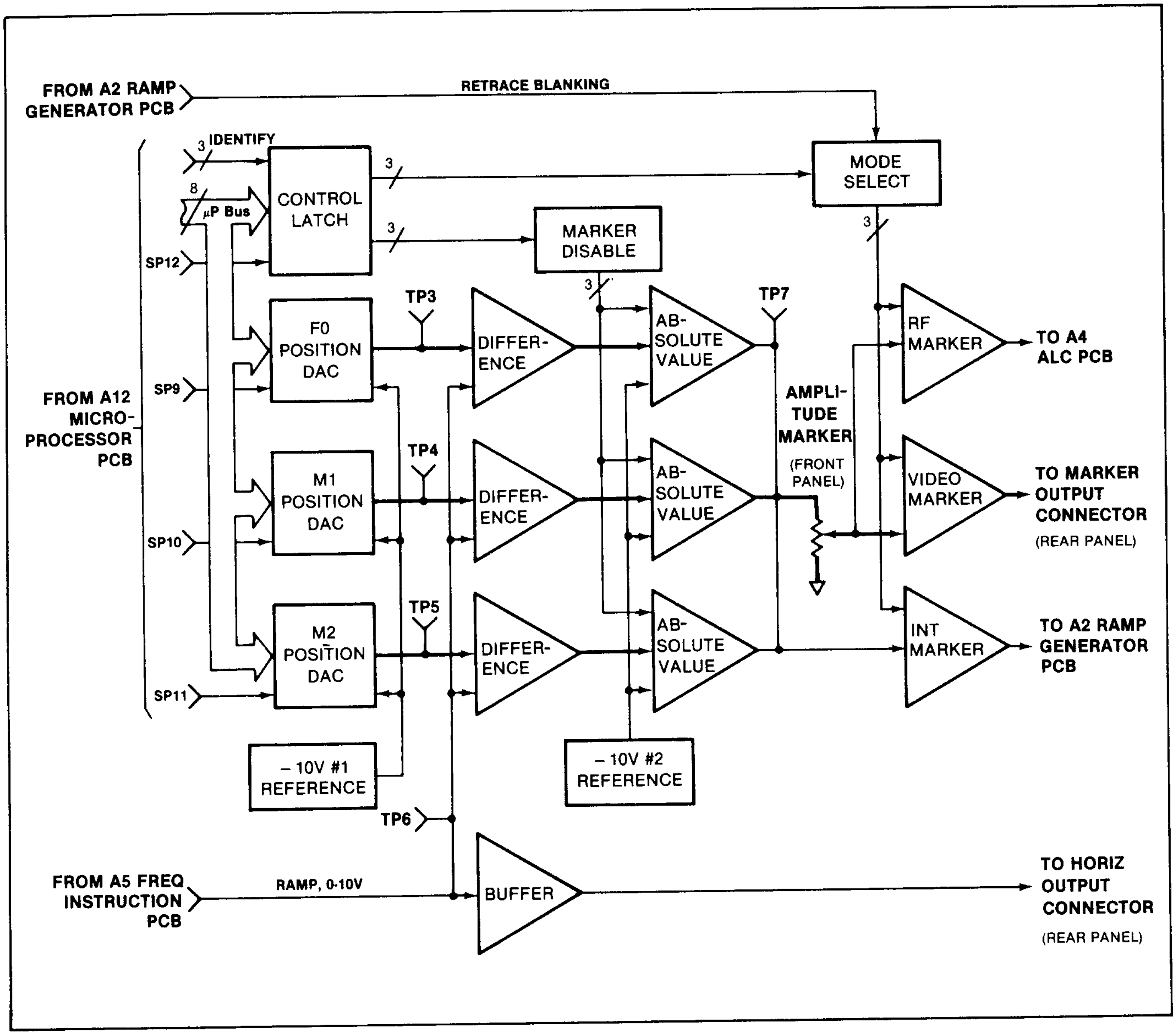


Figure 7-37. Error Code 22 Troubleshooting Diagram

7-11 A4 AUTOMATIC LEVEL CONTROL (ALC) PCB

7-11.1 A4 Automatic Level Control (ALC) PCB Circuit Description

The A4 Automatic Level Control (ALC) PCB, along with circuitry on the RF Component Deck and the YIG Driver PCB (A6, A7, or A8), provides for the automatic leveling of the RF output power. The A4 PCB also receives the ATTN 1 thru ATTN 4 control bits from the microprocessor and routes these bits to the Option 2 Step Attenuator current-driver circuits on the A10 PCB. The schematic diagram for the A4 PCB (3 sheets) is contained in Figure 7-40.

The sweep generator ALC loop (Figure 7-38) consists of the following circuits and components:

a. PIN Switch and RF Coupler/Detector. These components are on the RF Component Deck.

b. PIN Driver/Linearizer circuits. These circuits are on the individual A6, A7, and A8 YIG Driver PCBs.

c. Preamp (3), Absolute Value, Ext Gain Compare, Log Amp/Shaper, Latch/DAC, Level Amp, Compensation, and Unlevel Compare circuits. These circuits are on the A4 PCB.

As shown in Figure 7-38, the output from the RF Oscillator is applied to the RF Coupler/Detector via the PIN Switch. A sample of the RF power signal, which is attenuated by approximately 16 dB, is coupled to the RF detector. If internal leveling has been selected, the detector

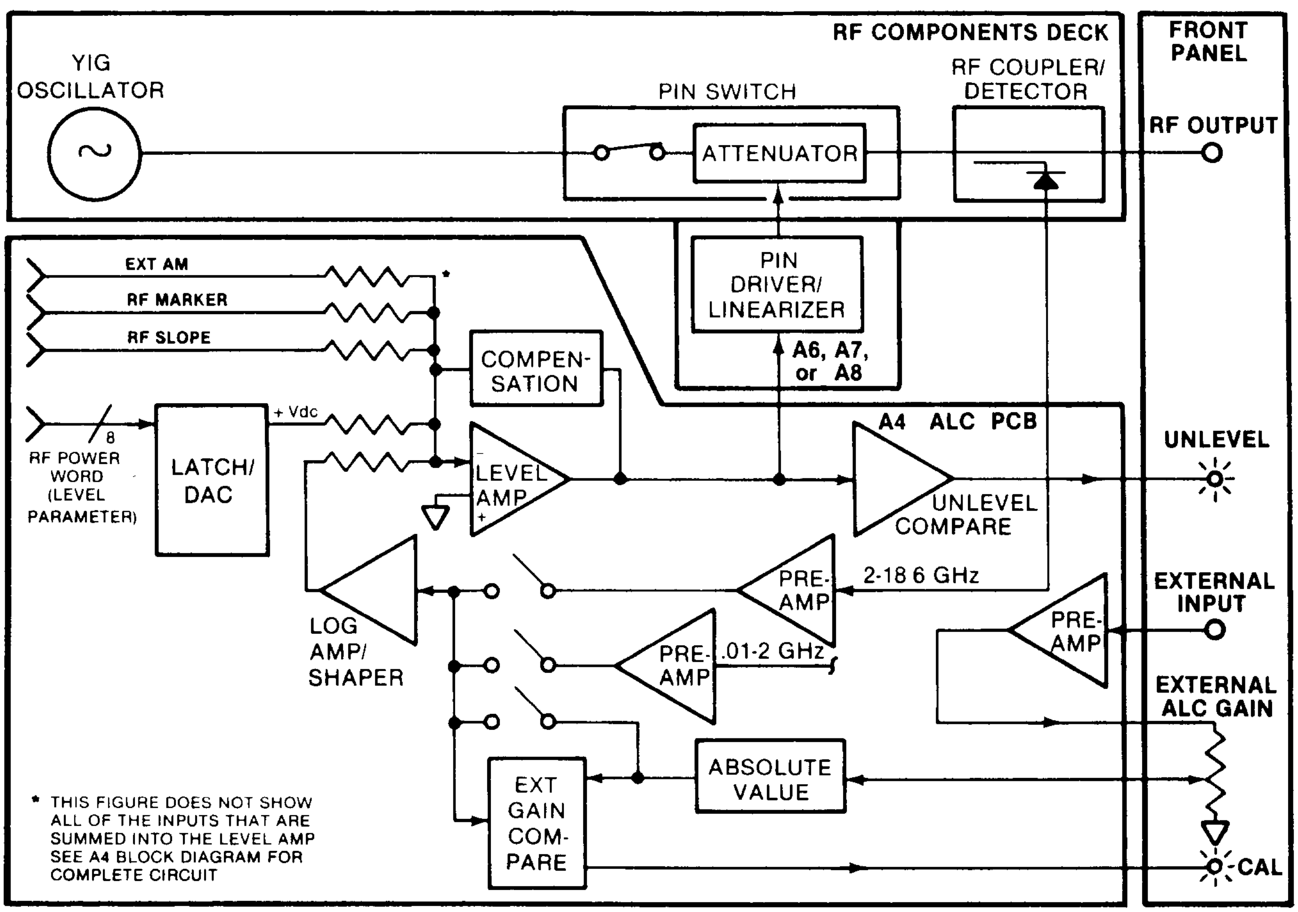


Figure 7-38. Sweep Generator Overall Leveling Loop

output signal is applied to the Log Amp/Shaper via the appropriate Preamp circuit. If external leveling has been selected, the external detector output signal is applied to the Log Amp/Shaper via the Absolute Value circuit.

At the Log Amp/Shaper, the detector output signal is amplified and shaped and its relationship to the main power signal is changed from logarithmic to linear. The linear-change-with-power-level-change output from the Log Amp/Shaper is summed at the Level Amp with the voltage output from the Reference DAC. The output from the DAC is the analog voltage representation of the digital power word that was selected using the front panel LEVEL pushbutton. Another reason for including a log amplifier in the ALC loop is to provide the loop with the means for setting output power in dBm.

The output of the Level Amp is applied to either the A6, A7, or A8 PCB PIN Driver/Linearizer circuit (depending on which YIG oscillator band is supplying the output power). The A6, A7, and A8 PIN Driver/Linearizer circuits provide an adjustment for customizing the loop gain for each YIG oscillator band.

The A4 PCB leveling circuit (Figure 7-39) provides overall control of the RF output power. The A4 PCB has two preamplifiers for internal leveling: a .01-2 GHz circuit (U4) and a 2-18.6 (or 20) GHz circuit (U6).

For external leveling, both a preamplifier (U7) and an Absolute Value circuit (U8) are provided. The Absolute Value circuit provides a positive output for either a positive or a negative input. This circuit allows either a positive or a negative detector to be used for external leveling. If POWER METER leveling has been selected, the **L POWER METER** control line is TRUE. When TRUE, this line causes the circuit gain to be reduced to accommodate the larger voltage supplied by the power meter video output.

The Ext Gain Comparator circuit (U11A, U11B), in conjunction with the front panel EXTERNAL ALC GAIN control, provides for calibrating the gain of the external leveling loop. When the EXTERNAL ALC GAIN control is pushed in, the microprocessor causes either the **L <2 GHz** or the **L >2 GHz** line to go TRUE (depending upon the frequency range that has been selected). Either of these lines going TRUE places its associated detector signal on the Ext Gain Comparator's comparison input. With this signal in place, the EXTERNAL ALC GAIN control is adjusted until the voltage of the external detector is equal to the voltage of the internal detector. When these two voltages are equal, the **L EGD** (External Gain Detected) line will go TRUE and light the CAL indicator LED. The CAL indicator will remain lit until the EXTERNAL ALC GAIN control is released and control is restored to the external signal path.

The output signal from the external or internal preamplifier circuit is applied to the Log Amp/Shaper circuit (Figure 7-40, Sheet 2). The Log Amp/Shaper, with its associated temperature compensation and voltage offset circuits, provides gain and shaping for the internal detector signal.

The Level Amp (U21) and its associated input circuitry gives the A4 PCB overall control over the level of the sweep generator output-power signal. In addition to the Log Amp, the Level Amp input circuitry consists of the following:

a. DAC Circuit. This circuit (U22, U19B) converts the 8-bit digital power level control group from the microprocessor into an analog reference voltage used to set the sweep generator output power level. The microprocessor digital word represents the dBm value that was set using the front panel LEVEL pushbutton.

b. Level-Dip Logic Circuit. This circuit (Q2) causes the PIN Switch Attenuator (Figure 7-38) to go to maximum attenuation ("dip" RF power) when any of the following occurs:

    1. The **L LEVEL DIP** line from the A2 PCB goes TRUE (Paragraph 7-9.lb).
    2. The **L RETRACE BLANKING** line from the A2 PCB goes TRUE (provided the front panel RETRACE RF switch is OFF).

7-11.1 cont.

3. The front panel RF OFF switch is switched off.

When any of the above three conditions occurs, the Level-Dip Logic circuit output goes HIGH and causes the PIN Switch Attenuator to go to maximum attenuation.

c. RF MARKER Signal Line. This input is the 0 to +5V triangular waveform from the A3 Marker Generator PCB (paragraph 7-10.1a). This waveform causes the output power to "dip" up to 5 dB at the marker frequency, depending on the setting of the MARKER AMPLITURE control.

d. RF SLOPE Control. This input is from the front panel RF SLOPE control. The purpose of this input is to provide a linear boost in output power as the RF oscillator sweeps across its frequency band. The RF SLOPE input is a negative-going voltage ramp that is proportional to frequency. This signal provides an increase in output power at higher frequencies.

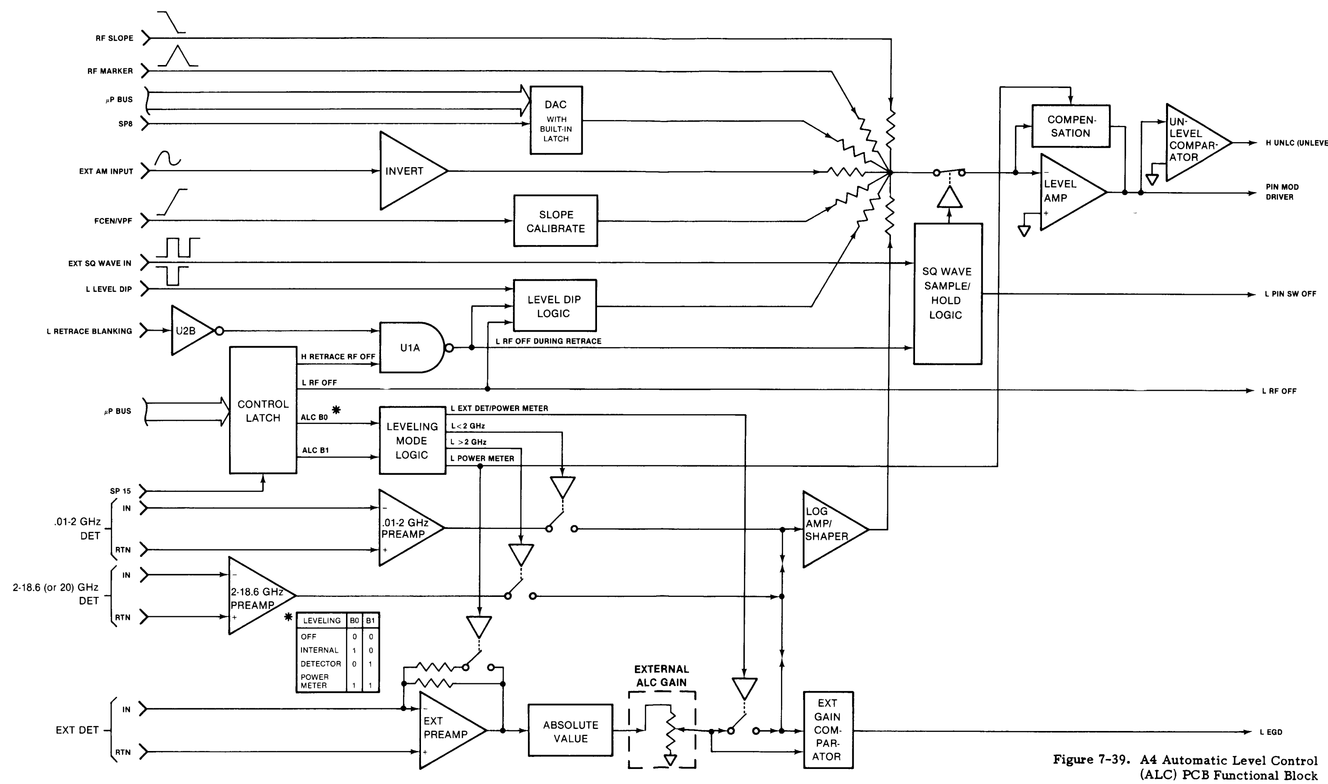
e. Slope Calibrate Circuit. This circuit (U19D) calibrates the sweep-frequency output to be optimally horizontal when the RF SLOPE control is OFF. The input to this circuit is a 0 to 10V ramp from the A5 PCB. The output of the Slope Calibrate circuit can be either a positive or a negative analog voltage, of which the value is proportional to frequency.

f. EXT AM INPUT Connector. This input is from the EXT AM INPUT rear panel connector. This modulation signal is inverted and summed into the Level Amp. The bandwidth of the modulation signal is rated from dc to 50 kHz; signal sensitivity is 1 dB/V.

g. Sq Wave Sample/Hold Logic Circuit. This circuit (Q3, U2C, U1D, U23A, U23B, U2F, U23C, U23D, U20B) provides for square wave modulation of the RF output signal, at rates up to 30 kHz. The inputs to this circuit are the **EXT SQ WAVE IN** signal from the rear panel connector and the **L RF OFF DURING RETRACE** control line from NAND gate U1A. When the **EXT SQ WAVE IN** signal goes negative or when the **L RF OFF DURING RETRACE** line goes TRUE, the **L PIN SW OFF** line goes TRUE and opens the PIN Switch (Figure 7-38). When open, the PIN Switch attenuates the RF output signal by ≈ 40 dB. When the EXT SQ WAVE IN signal again goes positive (or **L RF OFF DURING RETRACE** goes FALSE), the **L PIN SW OFF** line goes FALSE and closes the PIN switch. The ALC loop cannot respond fast enough to track the changes in RF output during square-wave modulation. Therefore, a sample-and-hold network is used to open the ALC loop and hold the previous PIN switch drive current when modulation is applied.

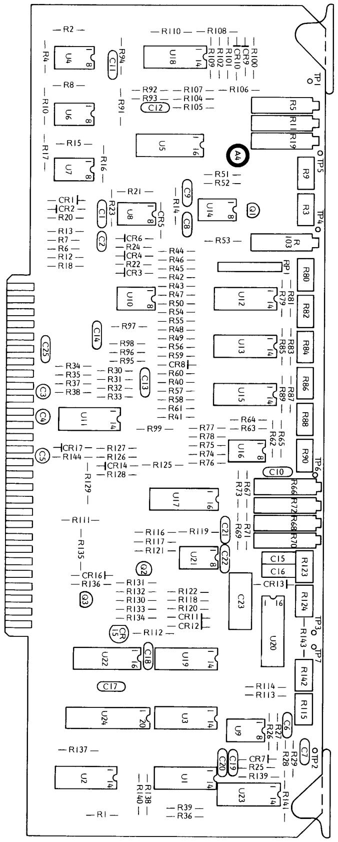
The two remaining blocks on this diagram are the Compensation and the Unlevel Comparator circuits. The Compensation circuit (C23, CR13) is used to stabilize the loop. The circuit also slows the response of the ALC loop when power meter leveling has been selected. Slowing the loop's response is necessary because a power meter's response to variations in output power is much slower than a detector's response.

The Unlevel Comparator circuit (U11D) provides drive for the front panel UNLEVEL indicator LED. If the output of the Level Amp goes positive, indicating more power has been called for than the YIG oscillator can deliver, the **H UNLC** line goes TRUE and lights the UNLEVEL indicator LED.



LEVELING	B0	B1
OFF	0	0
INTERNAL	1	0
DETECTOR	0	1
POWER METER	1	1

Figure 7-39. A4 Automatic Level Control (ALC) PCB Functional Block Diagram



A4 PCB Parts Locator Diagram

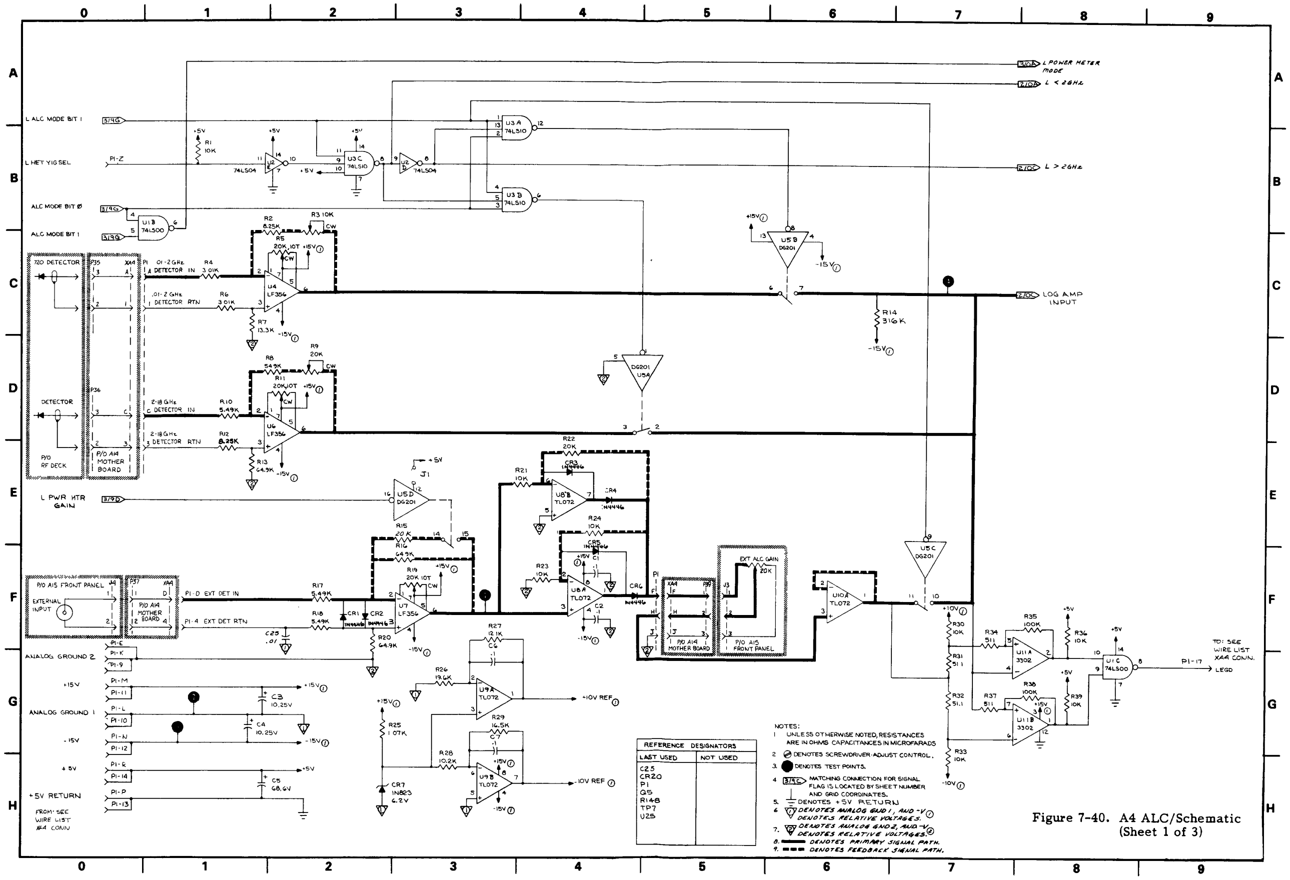


Figure 7-40. A4 ALC/Schematic (Sheet 1 of 3)

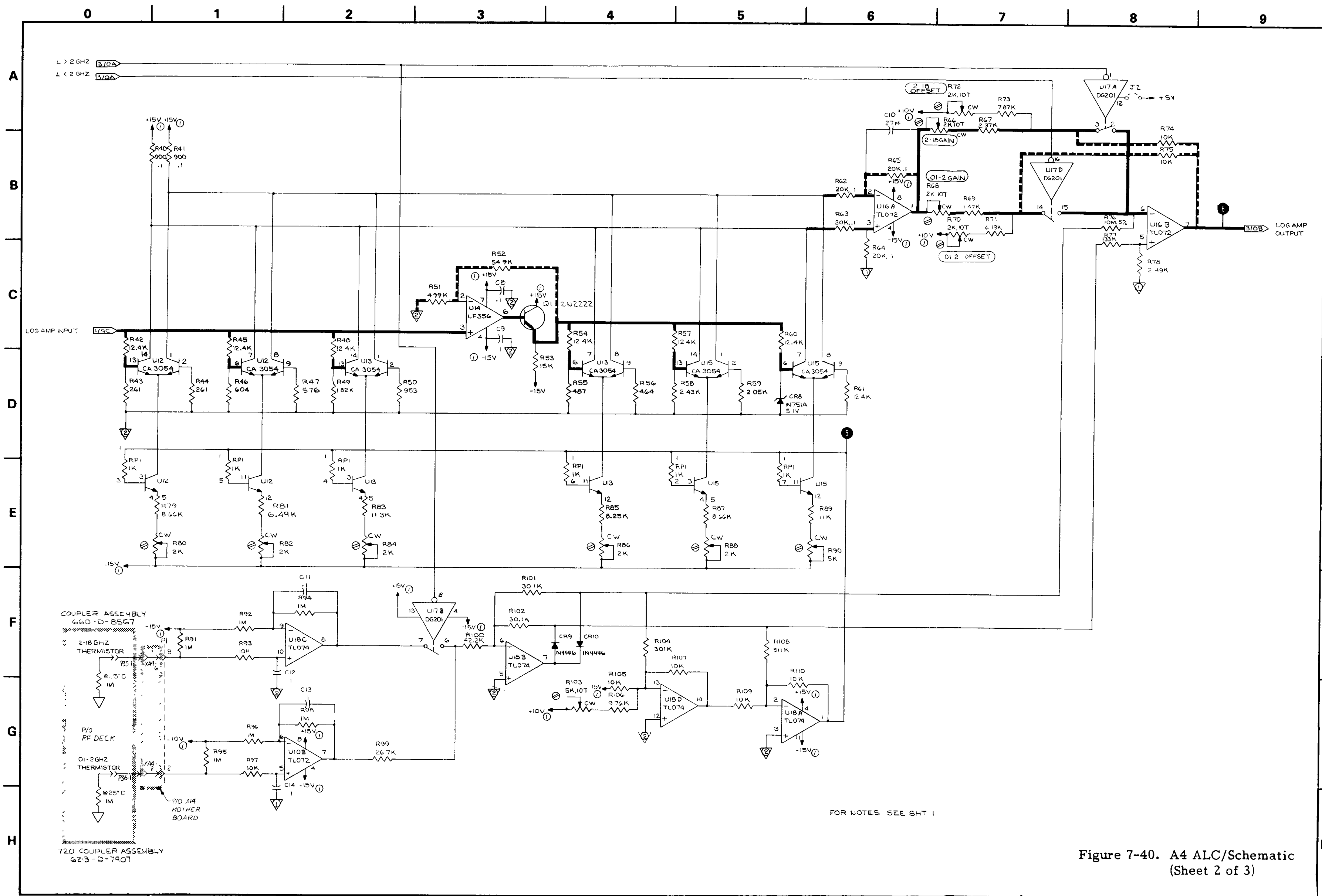


Figure 7-40. A4 ALC/Schematic (Sheet 2 of 3)

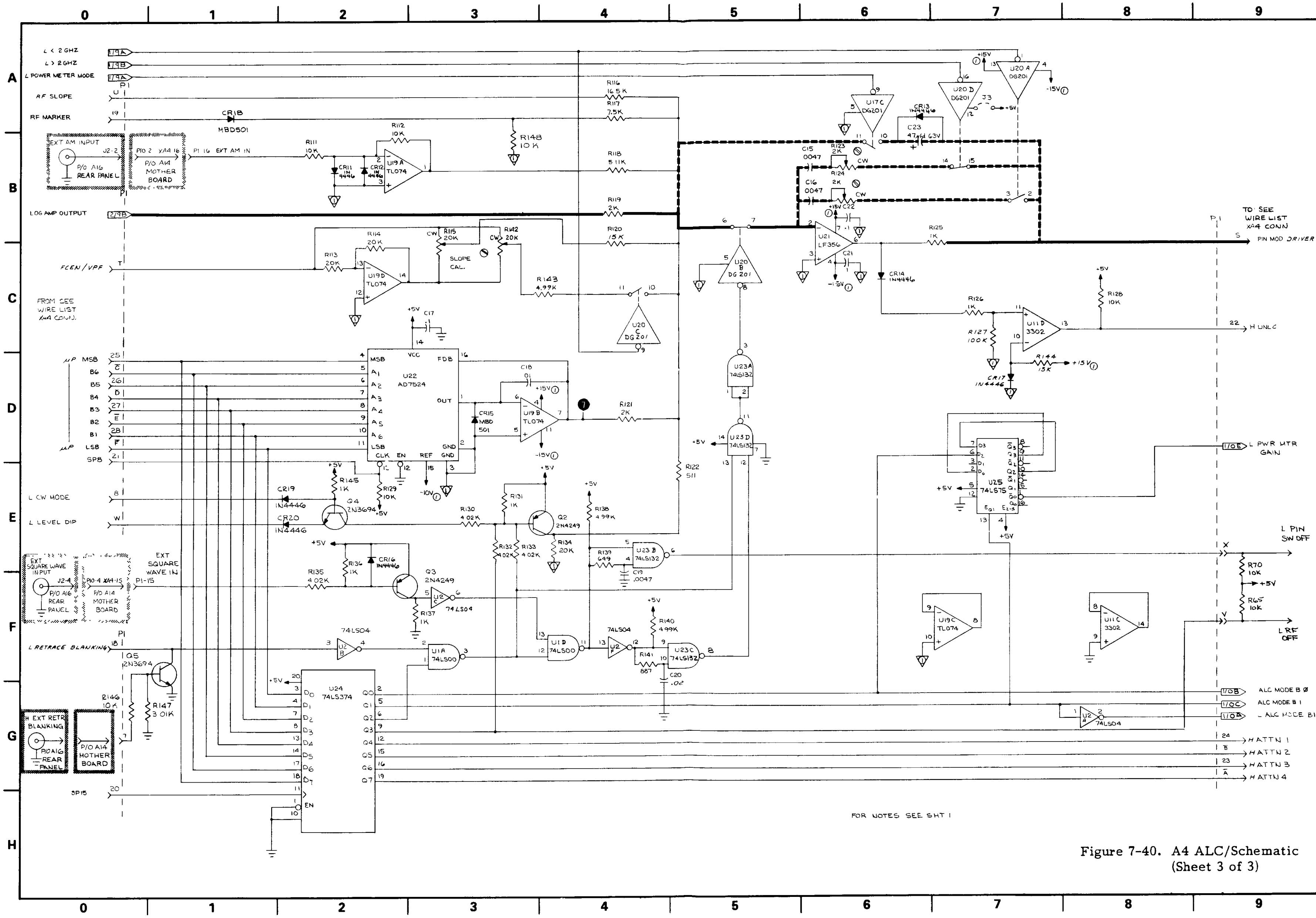


Figure 7-40. A4 ALC/Schematic
(Sheet 3 of 3)

7-11.2 Sweep Generator Automatic-Leveling-Control (ALC) Loop Troubleshooting Information and Data

Error Codes 15, 16, 17, 18, and 20 (Error Code 19 is not used) report on the status of the sweep generator automatic-leveling-control (ALC) loop. The microprocessor routines associated with error codes 15 through 18 verify that leveled power is available at the mid frequency in the HET (6647 and 6648), Osc 1-, Osc 2-, and Osc 3-YIG bands. The routine associated with Error Code 20 initiates an analog sweep and verifies that leveled power is available over 95% of the frequency band.

To accomplish the ALC error-code tests, the microprocessor configures the ALC loop circuits as follows:

a. Error Codes 15 through 18

1. The A5 PCB is set to CW operation, and the ALC loop output power is set to 10 dB below the guaranteed maximum output power.

2. The A5 F Center DAC (U7) is set as follows:

   (a) to 1 GHz for Error Code 15 (6647 and 6648),
   (b) to 5 GHz for Error Code 16,
   (c) to 10.2 GHz for Error Code 17,
   (d) to 15.5 GHz for Error Code 18 (6637 and 6647), and
   (e) to 16.2 GHz for Error Code 18 (6638 and 6648).

b. Error Code 20

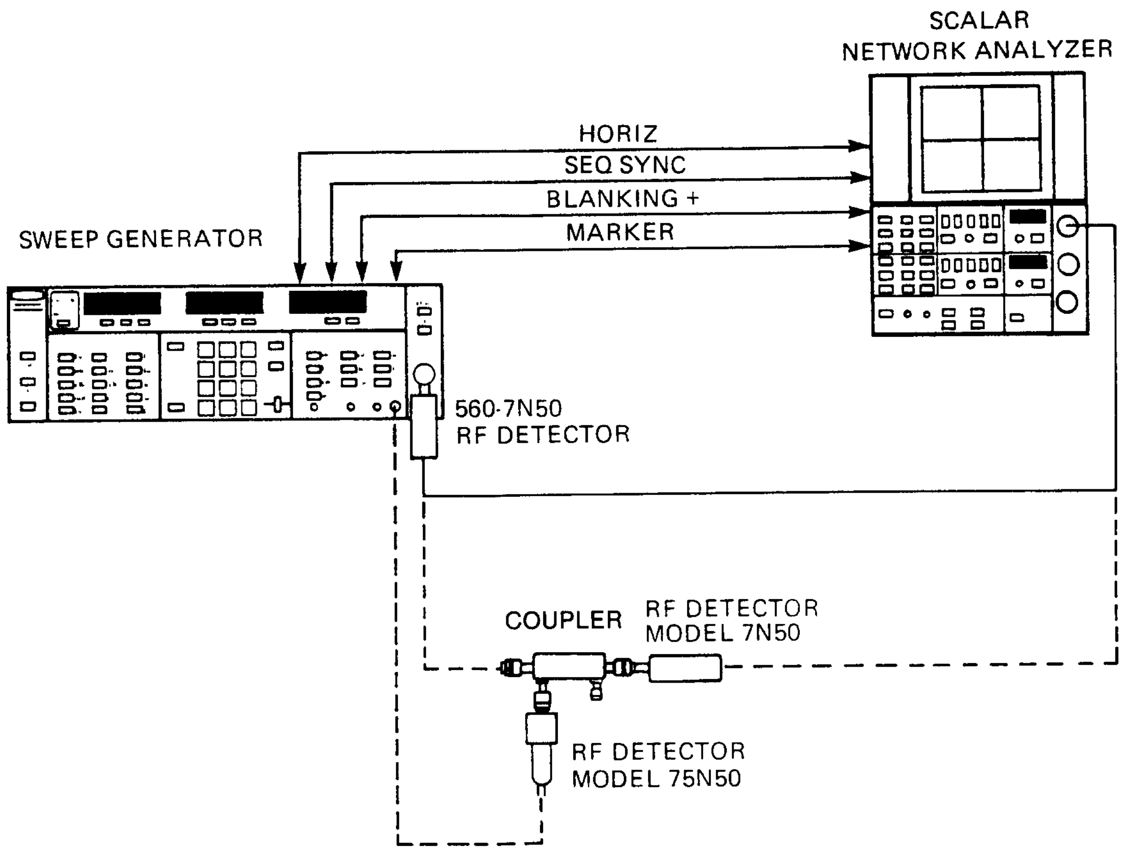
1. The A5 PCB is set for both CW and A2 sweep ramp operation. The **F Center DAC** is set for 9.3 GHz (6637 and 6647) or 10 GHZ (6638 and 6648). And the **Sweep Width DAC** (U24) is set to provide a ramp that will sweep 95% of the frequency band.

2. The A2 PCB is set to provide an 8-ms sweep ramp.

3. The ALC loop output power is set to 10 dB below the guaranteed maximum output power.

All of the ALC error-code routines monitor the **H UNLEVELED** line at the microprocessor input buffer. If this line goes LOW, the appropriate error code is displayed.

The test equipment setup for troubleshooting error codes 15-20 is provided in Figure 7-41; individual troubleshooting flowcharts are provided in Figure 7-42 through 7-46 respectively; individual troubleshooting block diagrams are provided in Figure 7-47 through 7-51 respectively; ALC loop waveforms are shown in Table 7-14; and a tabulation giving minimum output power (YIGs) and insertion loss values for the RF components is provided in Figure 7-52.



Initial Control Settings

Sweep Generator

FREQUENCY RANGE: F1-F2
TRIGGER: AUTO
MARKERS: INTENSITY
LEVELING: INTERNAL (DETECTOR*)
RETRACE RF: Off
RF ON: On
HORIZ OUTPUT DURING CW (Rear Panel): ON
RF SLOPE: OFF
LEVEL: 0 dBm
SWEEP TIME: 50 ms
F1: 10 MHz (Error Code 15)
2 GHz (Error Code 16)
8 GHz (Error Code 17)
12.4 GHz (Error Code 18)
10 MHz (Error Code 20)

F2: 2 GHz (Error Code 15)
8 GHz (Error Code 16)
12.4 GHz (Error Code 17)
18.6 (or 20) GHz (Error Code 18)
18.6 (or 20) GHz (Error Code 20)

Scalar Network Analyzer

CHANNEL A ON: On
INPUT: A
MEMORY: Off
dB PER DIVISION: 5
REFERENCE dB/dBm: dBm
SET (screwdriver pot): Midrange
OFFSET: -00.00
CHANNEL B: Not Used
MARKER THRESHOLD: Midrange
REAL TIME: On
SMOOTHING: Off
POWER: ON

* External leveling.

Figure 7-41. Test Equipment Setup for Troubleshooting Error Codes 15 thru 20

GENERAL INFORMATION

1. Check the following dc voltages before starting any of the flowcharts:
   a. +5V - check at P1, pins R (+) and P (-)
   b. +15V - check at P1, pin M (reference measurement to pin L)
   c. -15V - check at P1, pin N (reference measurement to pin L)
2. Logic voltages are TTL.

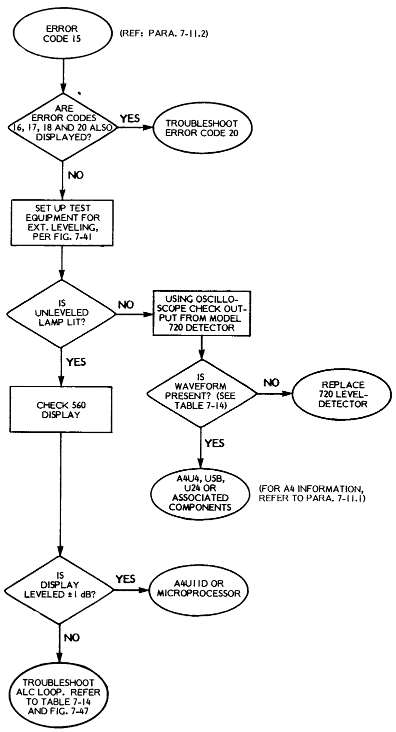


Figure 7-42. Error Code 15 Troubleshooting Flowchart

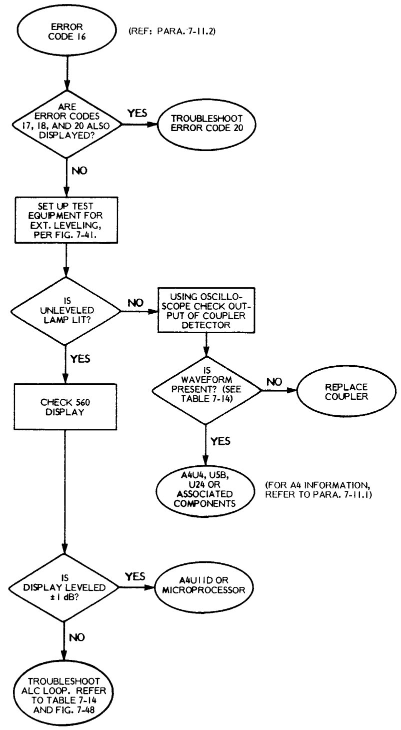


Figure 7-43. Error Code 16 Troubleshooting Flowchart

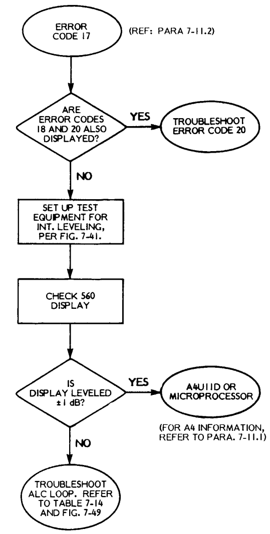


Figure 7-44. Error Code 17 Troubleshooting Flowchart

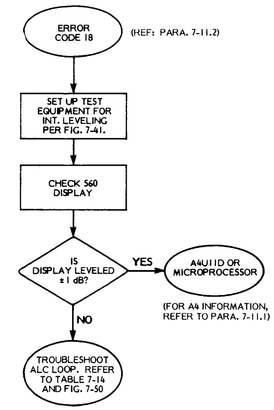


Figure 7-45. Error Code 18 Troubleshooting Flowchart

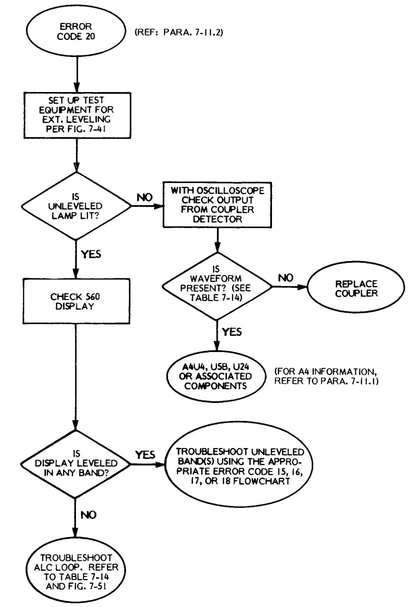


Figure 7-46. Error Code 20 Troubleshooting Flowchart

Fig. 7-42 7-43 & 7-44

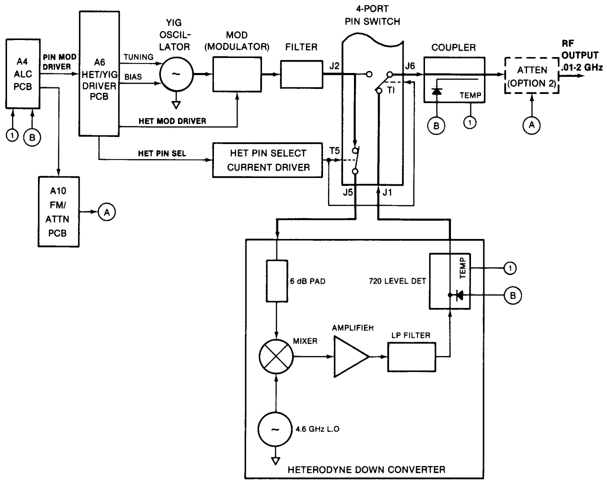


Figure 7-47. Error Code 15 Troubleshooting Block Diagram

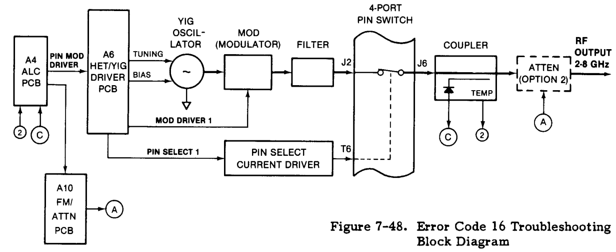


Figure 7-48. Error Code 16 Troubleshooting Block Diagram

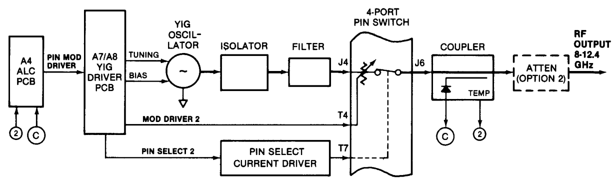


Figure 7-49. Error Code 17 Troubleshooting Block Diagram

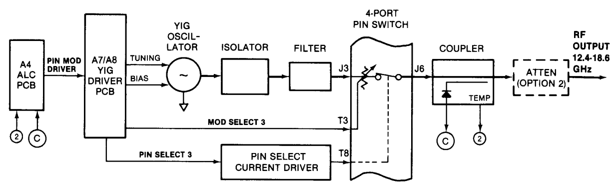


Figure 7-50. Error Code 18 Troubleshooting Block Diagram

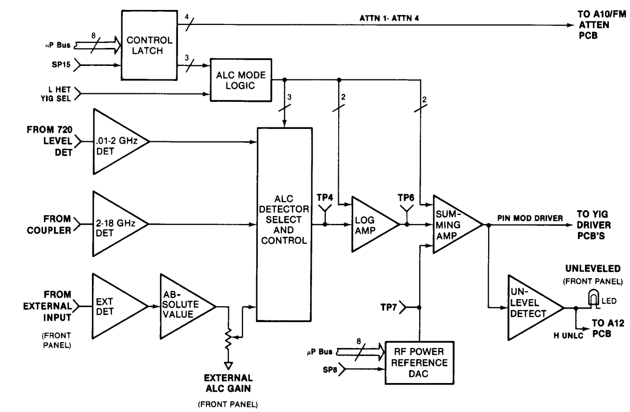
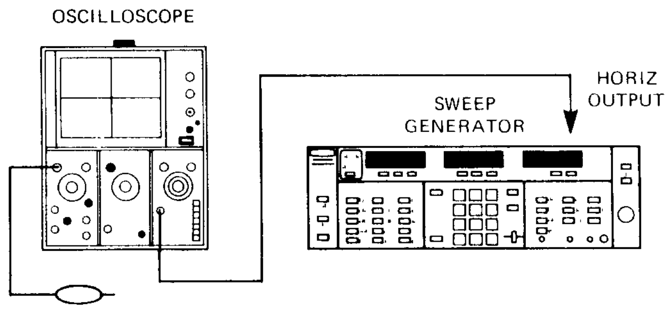


Figure 7-51. Error Code 20 Troubleshooting Block Diagram

Fig. 7-47, 7-48, 7-49 & 7-50

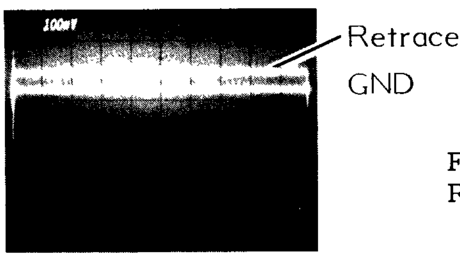
Table 7-17. ALC Loop Waveforms

TEST EQUIPMENT SETUP



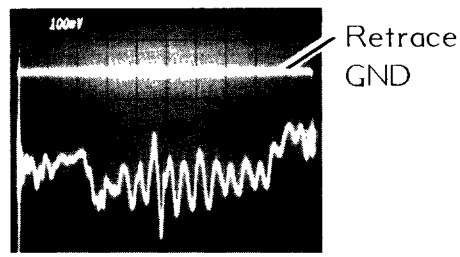
MODEL 720 DETECTOR OUTPUT

LEVELED



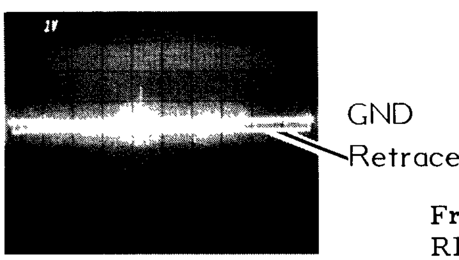
Frequency: .01 - 2 GHz
RF Power: 5 mW

UNLEVELED*



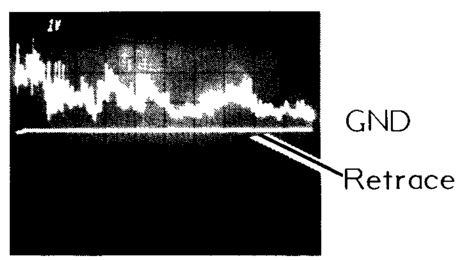
A4TP4

LEVELED



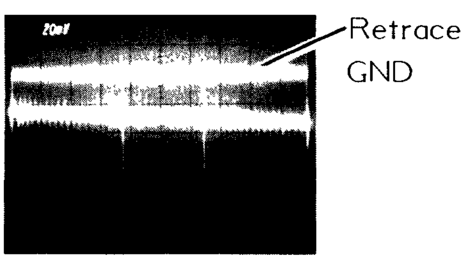
Frequency: .01 - 18.6 GHz
RF Power: 5 mW

UNLEVELED*



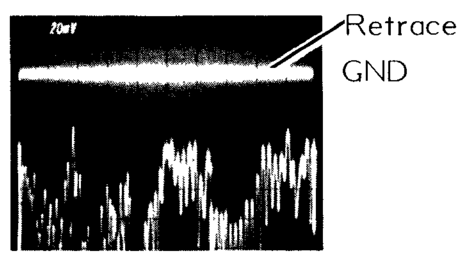
COUPLER OUTPUT

LEVELED



Frequency: 2 - 18 GHz
RF Power: 5 mW

UNLEVELED*

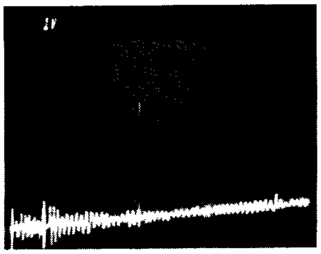


* Unleveled output simulated by disabling A4P1, pin S.

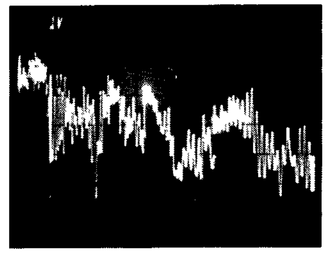
Table 7-17. ALC Loop Waveforms (continued)

A4TP6

LEVELED



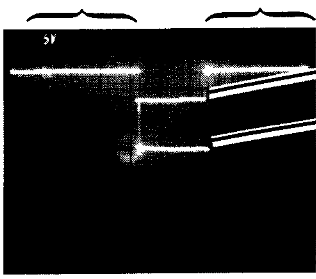
UNLEVELED*



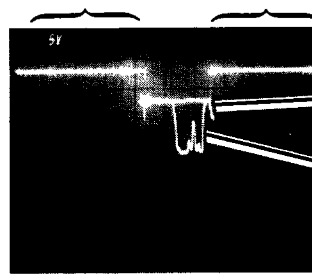
Frequency: .01 - 18.6 GHz
RF Power: 5 mW

A7P1, Pin K

LEVELED



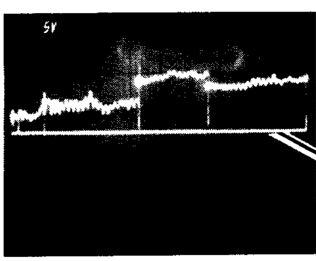
UNLEVELED**



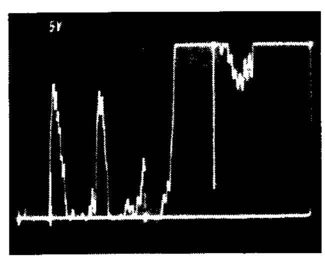
Frequency: .01 - 18.6 GHz
RF Power: 5 mW

A4P1, Pin S

LEVELED



UNLEVELED*



Frequency: .01 - 18.6 GHz
RF Power: 5 mW

NOTE

The unleveled waveform shown is an example of one that could appear at pin S - the Level Amplifier (U24) could also be latched at either rail; in which case the waveform could be a straight line (dc voltage), appearing at either +15V or -15V.

* Unleveled output simulated by disabling A4P1, pin S.
** Unleveled output simulated by disabling A7P1, pin K.

YIG-TUNED OSCILLATORS

WILTRON PART NO.	FREQUENCY (GHz)	MINIMUM POWER mW	dBm
1005-46	2-8 (WJ)	30.2	14.8
1005-47	2-8 (Avantek)	30.2	14.8
1005-51	12.4-18.6 (WJ)	30.2	14.8
1005-52	12.4-20 (WJ)	50, ≤18.5 GHz	17.0
		40, >18.5 GHz	16.0
1005-53	8-12.4 (Avantek)	45	16.5
1005-54	8-12.4 (WJ)	45	16.5

ISOLATORS

WILTRON PART NO.	FREQUENCY (GHz)	INSERTION LOSS (MAX.)
1000-20	12.4-18.5	0.5 dB
1000-21	7.0-12.4	0.5 dB
1000-35	12.4-20	0.5 dB

FILTERS

WILTRON PART NO.	FREQUENCY (GHz)	INSERTION LOSS (MAX.)
1030-26	2-8	0.5 dB
1030-29	7.9-13	0.55 dB
1030-31	2-18.7	0.55 dB
1030-32	12.4-20	0.6 dB

MISCELLANEOUS RF COMPONENTS

WILTRON PART NO.	COMPONENT	FREQUENCY (GHz)	SPECIFICATION (Max.)
660-C-8567	Coupler	2-18.6	Insertion Loss: 1 dB ± 0.2 dB Sensitivity: ±0.4 dB VSWR: 1.2 between 2-8 GHz 1.4 between 8-18.6 GHz
660-C-8821	4-Port PIN Switch	.01-18.6	Insertion Loss / Frequency Limits 1.5 dB / .01-2 GHz 2.5 dB / 2-12.4 GHz 3.0 dB / 12.4-18.6 GHz
660-C-9342	Modulator (MOD)	2-8	Insertion Loss: 1.5 dB at 0 mA modulator current
Model 720	Level Detector	.01-2	Insertion Loss: 2.5 dB Sensitivity: ±0.25 dB
660-C-8090	Heterodyne Down Converter	.01-2	Output Power: +13 dBm output power for -8 dBm input.

Figure 7-52. RF Components, Specification Data

7-12 A5 FREQUENCY INSTRUCTION AND A6-A8 YIG DRIVER PCB'S

7-12.1 A5 Frequency Instruction PCB Circuit Description

The A5 Frequency Instruction PCB provides YIG oscillator tuning voltages to the A6, A7, and A8 YIG Driver PCBs, plus a narrow (≤50 MHz) sweep tuning voltage ramp to the A10 FM/Attenuator PCB. The A5 PCB also supplies the YIG Driver PCBs with a regulated +10 Vdc, which is used as an oscillator-bandswitch reference voltage. A functional block diagram of the A5 PCB is shown in Figure 7-53, and the schematic (2 sheets) is shown in Figure 7-54.

The three main YIG tuning voltages supplied by the A5 PCB (Figure 7-53) are the **F CEN**, **ΔF >50 MHz**, and **F CORR** signals. These three signals are summed together at the YIG Driver PCBs and used to generate the YIG oscillator tuning current.

The **F CEN** signal is the output of the Center Frequency digital-to-analog converter (DAC) circuit (U7, U6). The input to this circuit is a 16-bit group from the microprocessor representing one of the following:

a. the center frequency in a FULL, F1-F2, or M1-M2 sweep,
b. the F0 frequency in a ΔF F0 sweep,
c. the F1 frequency in a ΔF F1 sweep, or
d. the selected CW F0, CW F1, CW F2, CW M1, or CW M2 frequency.

The center frequency group is loaded into the two F CEN Latches (U8, U9) when the microprocessor clocks **SP1** and **SP0** HIGH.

The **ΔF >50 MHz** signal is the output from the Sweep Width (ΔF) DAC (U24). The U24 circuit is a multiplier DAC that scales the analog REF input by a factor of N/4095. The circuit gain is from 0 to 1 and the resolution is $1 \div 2^{12}$ ($1 \div 4096$). The digital input to U24 is a 12-bit group from the microprocessor representing one of the following:

a. the sweep width in a FULL, F1-F2, or M1-M2 sweep,
b. the ΔF value in a ΔF F0 or ΔF F1 sweep, or
c. a zero value in any of the five CW frequency modes.

The input digital group is loaded into the two ΔF Latches (U17, U18) when the microprocessor clocks **SP6** and **SP7** HIGH.

The analog REF input to the Sweep Width (ΔF) DAC (U24) is a 10-volt signal (-5V to +5V) from the Sweep Sel Switch (U22A, U22B, U22C), via the -5V Offset circuit (U23). The inputs to the Sweep Sel Switch are a 0-10V manual tuning voltage from the front panel MANUAL SWEEP control, a 0-10V ramp from the A2 Ramp Generator PCB, or a 0-10V step-frequency tuning voltage from the Step Freq DAC (U19). The input to this DAC is a 12-bit group from the microprocessor that is generated in response to GPIB bus commands (paragraph 3-7.2). This 12-bit group is loaded into the two Step Freq Latches when the microprocessor clocks **SP3** and **SP4** HIGH.

The output of the Sweep Width DAC is applied to the W/M/N Switch (U28A, U28B, U28C, U28D). This switch is controlled by the microprocessor, via the ΔF Latch 2 circuit. The W/M/N switch is used to select a wide (>1000 MHz), medium (51 to 1000 MHz), or narrow (≤50 MHz) sweep width. If the microprocessor has selected a wide sweep width, the DAC output is applied to the output circuit via the Buffer (U26). If the medium sweep width was selected, the DAC output is scaled down by the ÷16 resistor (R37) before being applied to the output circuit. And if the narrow sweep width was selected, the DAC output is applied to the Diff Amp circuit (U10B). This circuit cancels any common mode signals that may exist between the analog ground on the A5 PCB and the analog ground on the A10 PCB. The output of the Diff Amp is applied to the A10 PCB via the **ΔF ≤50 MHz** signal line.

The **F CORR** signal is the output from the I/E (current to voltage) Converter circuit (U3). The input to this circuit is the sum of the current outputs from both the ROM Lin DAC and the Freq Ver DAC.

The ROM Lin DAC (U2) provides a linearity-correction frequency for the YIG oscillator.

7-12.1 cont.

The input to this DAC is from the linearizer ROMs on either the A6, A7, or A8 PCB, depending on which YIG oscillator band is presently being used. The purpose of these linearizing ROMs is to store data that will correct for nonlinear frequency characteristics in the YIG oscillator. The stored data provides the YIG oscillator with a frequency correction of up to ±64 MHz.

The Freq Ver DAC (U4) provides a vernier-correction frequency for the YIG oscillator. The input to this DAC is an 8-bit group from the microprocessor representing the front panel FREQUENCY VERNIER control-group output. This word is latched into the Freq Ver Latch (U5) when the microprocessor clocks **SP 2** HIGH. The Freq Ver DAC output provides the YIG oscillator with a frequency correction of up to ±12.7 MHz.

When no frequency correction is needed, the **F CORR** signal is 0 volts. If no linearity correction is required, the Lin ROM DAC input is 01111111 (0 = most significant bit). (There may be cases where a YIG oscillator requires no linearity correction. In such cases, no linearizing ROMs are supplied and the U2 input resistors (Figure 7-54) provide the 01111111 input.) If no frequency vernier correction has been programmed for the selected frequency parameter (paragraph 3-2.2c), 01111111 is also clocked into the Freq Ver Latch. When the output currents of the two frequency-correction DACs are summed with the equal-but-opposite current from R4, the I/E Converter outputs 0 volts.

The other signals generated on the A5 PCB are the **FCEN/VPF**, **V/GHz**, **RAMP OUT**, and **CW FILTER**.

The **FCEN/VPF** signal is from the FCEN/VPF switch. The inputs to this switch are **F CEN** and the sum of **F CEN** and either **ΔF >50 MHz** or **ΔF ≤50 MHz**. If the sweep width is ≤200 MHz, the **F CEN** signal is switched onto the **FCEN/VPF** line. This line is used on the A6, A7, and A8 YIG Driver PCBs to control oscillator bandswitching. If the sweep width is 200 MHz or less, bandswitch is inhibited. Control for the FCEN/VPF switch is from the microprocessor, via the ΔF Latch 2 circuit.

The **V/GHz** signal is the sum of the **F CEN** and either the **ΔF >50 MHz** or the **ΔF≤50MHz** signals. The two signals are summed at the FCEN/VPF Sum circuit (U14) and applied to the V/GHz Amp (U12). At U12, the output of the sum circuit is scaled so that the amplitude of the output ramp is 1 volt for each GHz of frequency tuning. This output is applied to the rear panel 1V/GHz OUTPUT connector.

The **RAMP OUT** signal is from the +5V Offset circuit (U21A). This circuit restores the frequency tuning voltage to its original 0 to 10V state. The **RAMP OUT** signal is applied to the A3 Marker Generator PCB, where it is buffered and applied to the rear panel HORIZ OUTPUT connector.

The **CW FILTER** signal is from the CW Filter Current Driver circuit (Q1). The input to this circuit is from the microprocessor, via the Step Freq Latch 2 circuit. The CW Filter Current Driver converts the latch-output voltage to a current that is used to drive the CW filter relay on the A6, A7, and A8 YIG Driver PCBs.

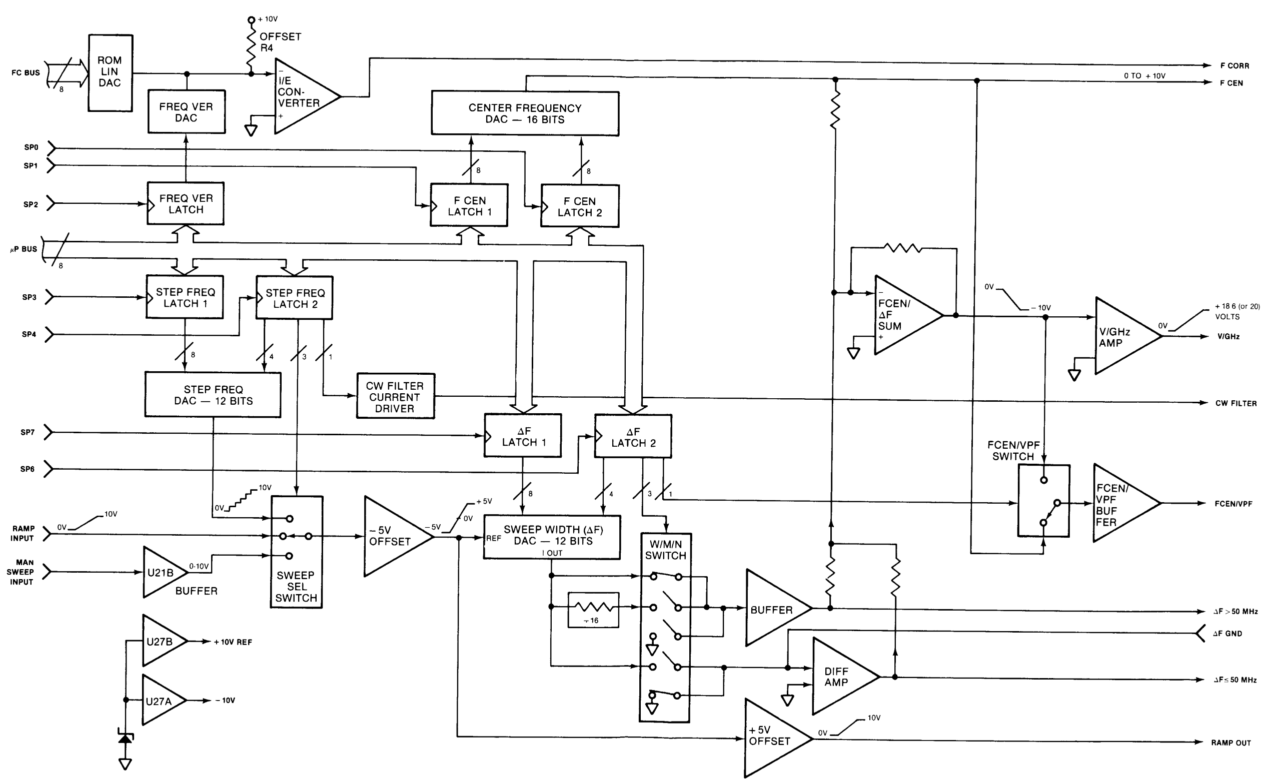


Figure 7-53. A5 Frequency Instruction PCB Functional Block Diagram

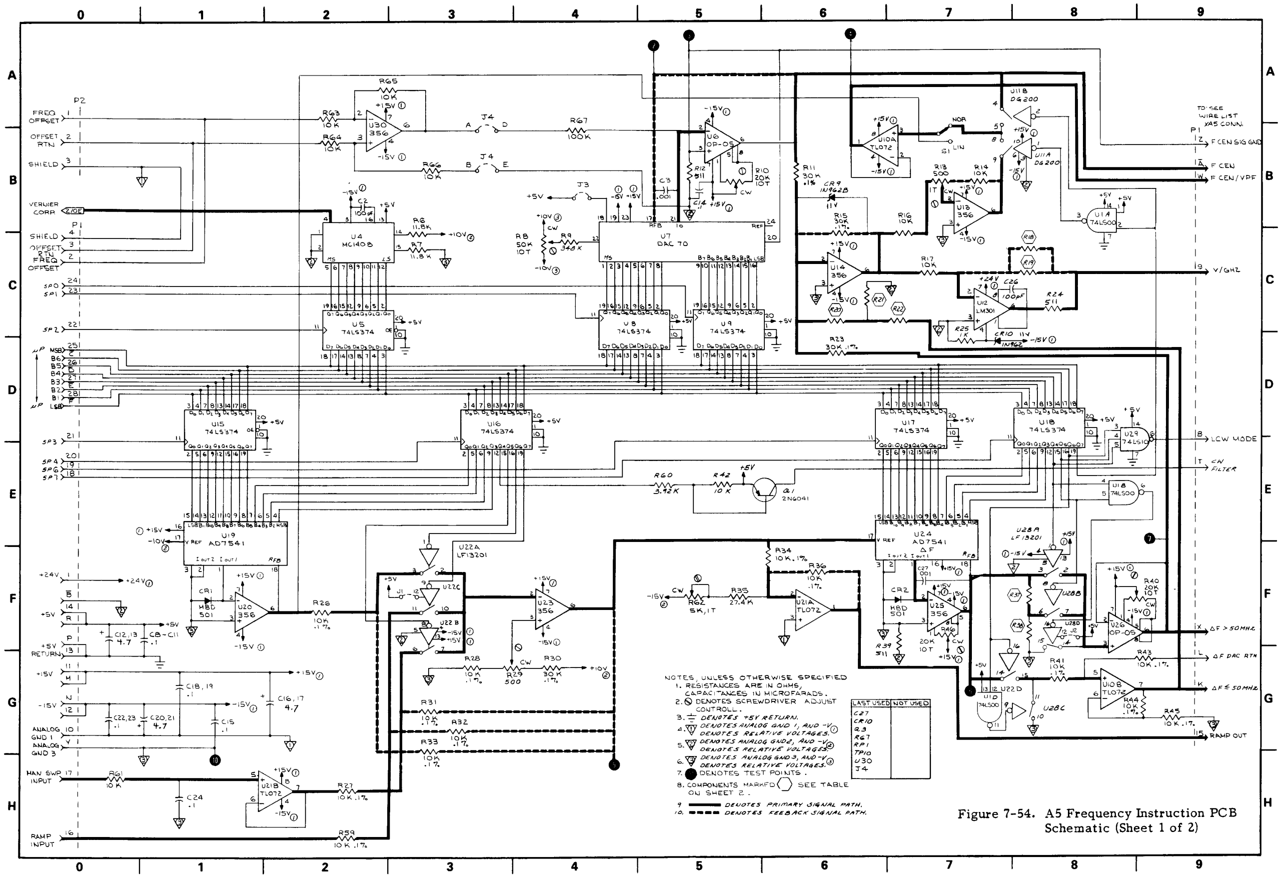
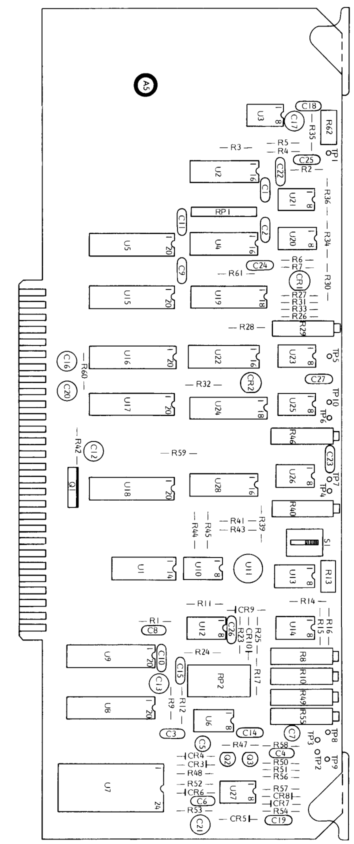
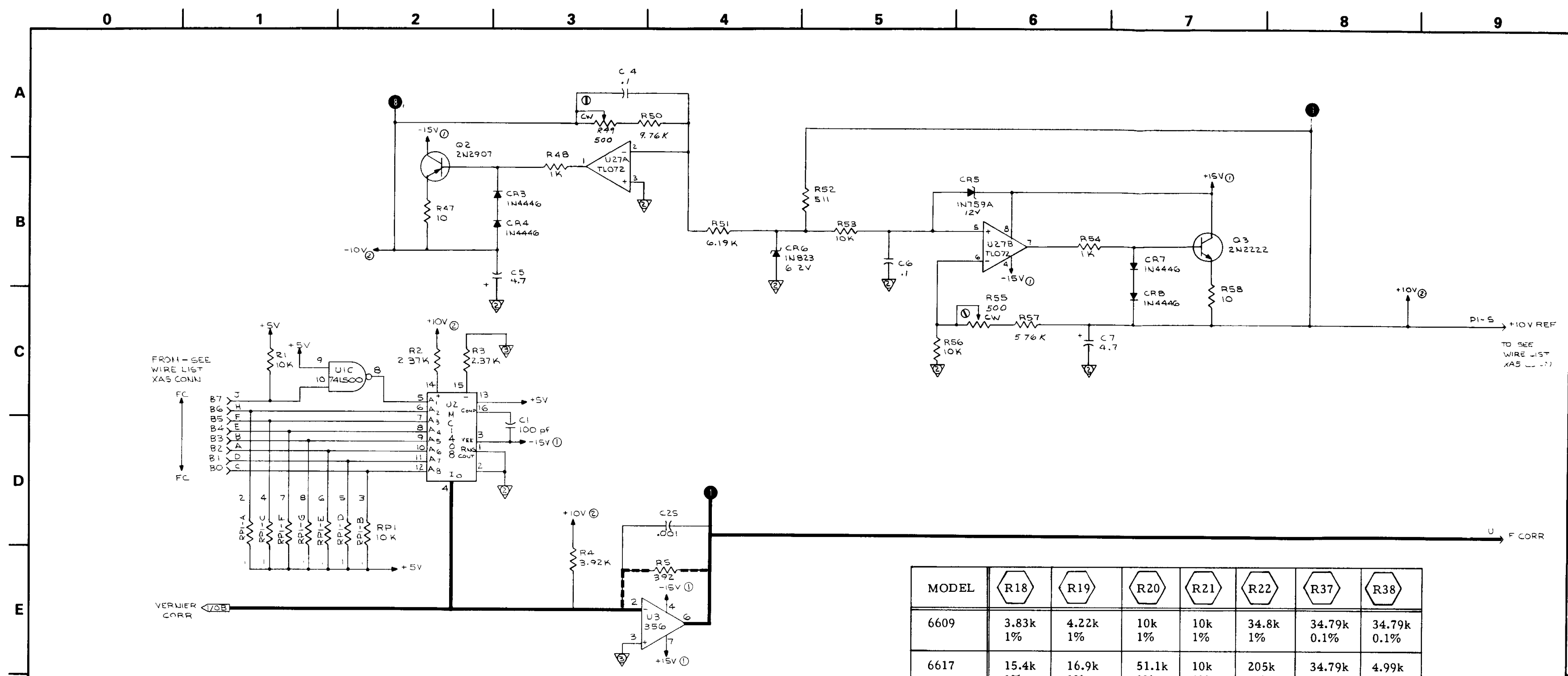


Figure 7-54. A5 Frequency Instruction PCB Schematic (Sheet 1 of 2)



A5 PCB Parts Locator Diagram

Figure 7-54. (Sheet 1)



MODEL	R18	R19	R20	R21	R22	R37	R38
6609	3.83k 1%	4.22k 1%	10k 1%	10k 1%	34.8k 1%	34.79k 0.1%	34.79k 0.1%
6617	15.4k 1%	16.9k 1%	51.1k 1%	10k 1%	205k 1%	34.79k 0.1%	4.99k 0.1%
6637/ 6647	115k 1%	22.1k 1%	619k 1%	10k 1%	110k 1%	34.79k 0.1%	2.32k 0.1%
6638/ 6648	38.3k 1%	42.2k 1%	100k 1%	4.64k 1%	348k 1%	34.79k 0.1%	2.32k 0.1%
6636	26.1k 1%	26.71k 1%	178k 1%	4.64k 1%	348k 1%	20.97k 0.1%	900Ω 0.1%
6640	38.3k 1%	42.2k 1%	42.2k 1%	4.64k 1%	348k 1%	20.97k 0.1%	900Ω 0.1%

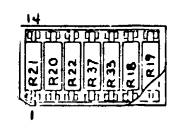


Figure 7-54. A5 Frequency Instruction PCB Schematic (Sheet 2 of 2)

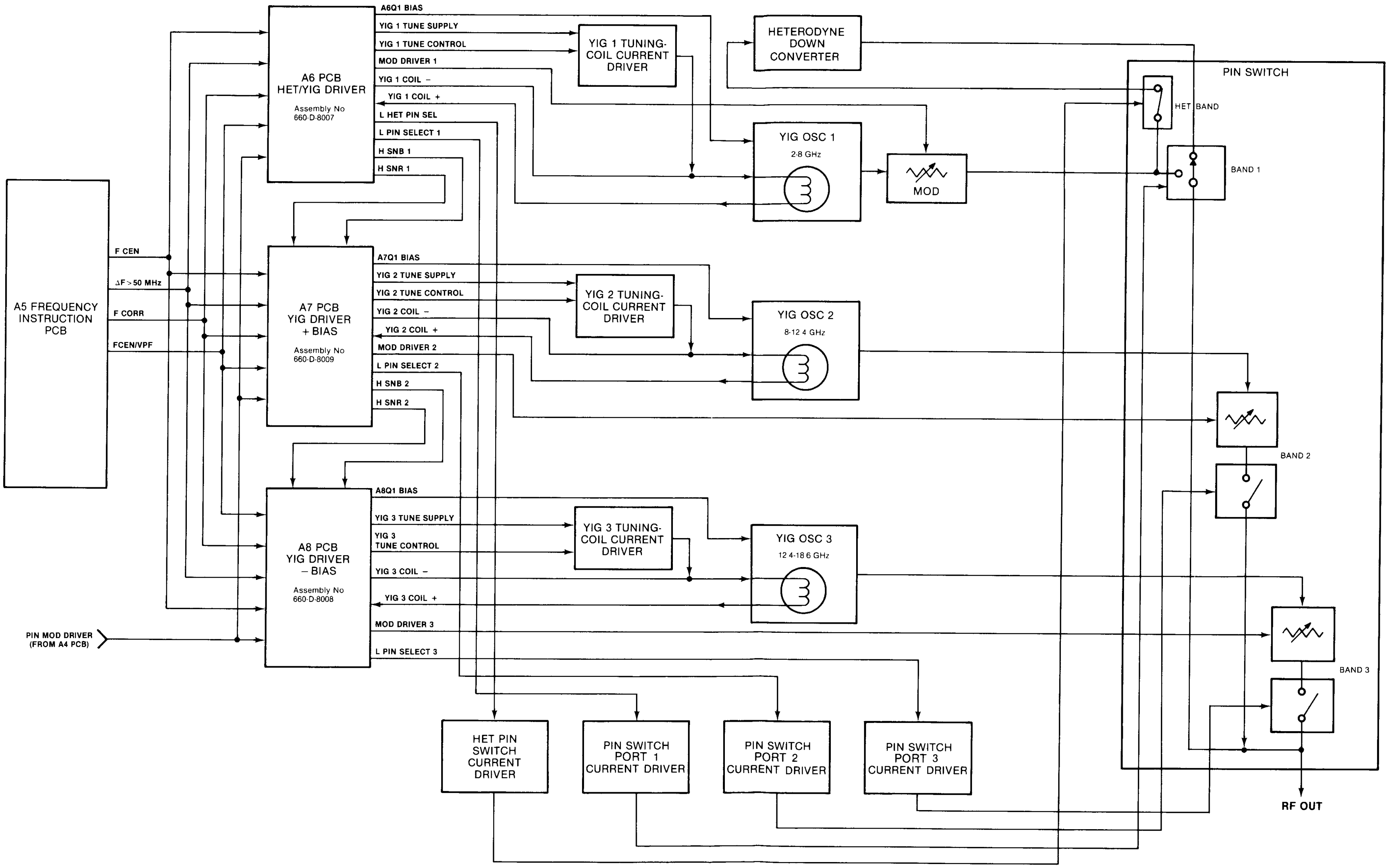


Figure 7-55. A6-A8 YIG Driver PCBs Overall Block Diagram

7-12.2 A6-A8 YIG Driver PCBs, Overall Description

The A6-A8 YIG Driver PCBs provide (1) drive currents for both the PIN switch and the bands 1, 2, and 3 YIG oscillator tuning coils and (2) modulating currents for the ALC-loop PIN attenuator (paragraph 7-11.1). The PCBs also develop the oscillator-bandswitch logic voltages.

The 6600 Series Sweep Generator uses several different YIG driver PCB designs. Such use is necessary to generate the 10 MHz to 40 GHz sweep range and to provide for using YIG oscillators made by several different vendors. Each PCB design is identified by a different assembly (Assy.) number. In some 6600 models (6637, 6638, 6647, etc.), as many as four YIGs may be necessary to sweep the frequency range. Each installed YIG requires a YIG Driver PCB; therefore, four slots (A6-A9) are available. In the four models covered by this manual, the A6 slot contains Assy. 660-D-8007. The A7 and A8 slots may either contain Assy. 660-D-8008 or -8009, depending upon the make of YIG (Avantek, Watkins-Johnson, etc.) installed and the A9 PCB slot is not used.

An overall block diagram for the A6 through A8 PCBs is shown in Figure 7-55 (facing page). This figure shows the main signals entering and exiting the PCBs, plus the interconnections with the A5 PCB and the YIG oscillators. These signals and interconnections are discussed below. For this discussion, assume that the 6647 or 6648 is being used and that the sweep is starting at the low (10 MHz) end of the band.

The three main signals that cause a tuning and bias current to be developed are the **F CEN, ΔF>50 MHz,** and **F CORR** signals from the A5 PCB (paragraph 7-12.1). These three signals are applied in parallel to all three YIG driver PCBs. However, because the **H SNB** (select next band) 1 and 2 oscillator-bandswitch lines are both FALSE, the A6 is the only PCB that can use the signals. Here they are summed and used to generate the frequency sweep.

The fourth A5 signal, **FCEN/VPF,** provides for oscillator bandswitching. An A6 bandswitch occurs when 2 GHz is reached and again when 8 GHz is reached. At 2 GHz , **L HET PIN SELECT** goes FALSE and switches the HET BAND out and BAND 1 to YIG Osc 1. At 8 GHz, several events occur:

a. The YIG oscillator tuning coil retunes the oscillator to a rest frequency of 2 GHz.
b. The **MOD DRIVER 1** line sets the Mod attenuator to maximum attenuation, and the **L PIN SELECT 1** line causes the PIN Switch's Osc 1 switch to be turned off. This action attenuates by ≥60 dBc the feedthrough of the oscillator 1 signal.
c. The **SNB 1** and **SNR 1** (select next linearizer ROM 1) oscillator-bandswitch lines toggle from LOW to HIGH, causing the Osc 2 YIG and linearizer ROM (read only memory) to be selected.

When Osc 2 is selected, the A7 PCB sums the three signals from A5 (**F CEN, ΔF>50 MHz, F CORR**) and uses them to generate the Osc 2 sweep, starting at 8 GHz. As on A6, the **FCEN/VPF** signal from A5 provides for oscillator bandswitching. The A7 has only one bandswitch point (12.4 GHz), when it is reached, the following occurs:

a. The YIG oscillator tuning coil retunes the oscillator to a rest frequency of 8 GHz.
b. The **MOD DRIVER 2** line sets the PIN Switch's Osc 2 attenuator to maximum attenuation, and the **L PIN SELECT 2** line turns the Osc 2 switch off. This action attenuates by ≥60 dBc the feedthrough of the oscillator 2 signal.
c. The **SNB 2** and **SNR 2** lines toggle from LOW to HIGH and select the Osc 3 YIG and ROM.

The Osc 3 circuit action is similar to that described for Osc 1 and Osc 2. The Osc 3 YIG rest frequency is 12.4 GHz.

7-12.3 A6 Het/YIG Driver PCB (Assy. 660-D-8007) Circuit Description

The A6 Het/YIG Driver PCB generates the following voltages and currents:

a. A tuning current for the Osc 1 YIG.
b. A modulating current for the Osc 1 attenuator (Assy. 660-B-9432), which is located in the Osc 1 YIG output circuit.
c. A tracking filter voltage for the Osc 1 YIG. (This filter is mounted inside the Osc 1 YIG package and provides ≥40 dB of harmonic suppression.)
d. A fixed bias voltage (-5V) for the Osc 1 YIG.
e. Linearizer ROM output data. (Linearizing ROMs, if installed, provide correction data for making the frequency characteristics of the YIG oscillator linear.)
f. Bandswitch logic voltages.

A block diagram for the A6 PCB is shown in Figure 7-56. A simplified schematic of the A6 E/I (voltage to current) Converter circuit is given in Figure 7-57. And the A6 PCB schematic (3 sheets) is provided in Figure 7-58.

The **F CEN**, **ΔF>50 MHz**, and **F CORR** signals generated on the A5 PCB are summed together at the E/I Converter (Figure 7-56) and used to generate the YIG tuning-coil Current. The E/I Converter circuit consists of all the components shown in Figure 7-57. As shown, the three A5 voltage signals are applied to U4, via U3D. If the output frequency is <2 GHz, a heterodyne offset voltage via U3B is also summed in with the A5 voltages. This offset voltage causes the YIG to sweep between 4.61 and 6.6 GHz. When this 4.61 to 6.6 GHz sweep is beat with the output from the 4.6 GHz local oscillator in the Down Converter (Assy. 660-D-9157) a 10 MHz to 2 GHz sweep results.

The output from U4 controls the current through the YIG tuning coil, via transistor A6Q2. The current through the coil develops a proportional voltage drop across sense resistor (R Sense) R15.

When the output frequency goes above 2 GHz, a bandswitch occurs. The Bandswitch/ROM Select Logic (Figure 7-56) causes the **L HET YIG SEL** line to go FALSE and open U3B. When U3B opens, the heterodyne offset voltage is removed from the U4 input. The U4 output then causes the YIG to sweep between 2 and 8 GHz.

When the output frequency goes above 8 GHz, the Bandswitch/ROM Select Logic causes the **L YIG SEL** line to go FALSE. When this line goes FALSE, U3D opens and U3A closes. When U3A closes, the R_{fb} (rest) resistor R17 provides the input to U4. This R17 input to U4 causes the YIG coil to tune the oscillator to a rest frequency of 2 GHz. Also when the **L YIG SEL** line goes FALSE, it causes transistor Q1 to saturate and reverse bias transistor A6Q3. When A6Q3 is reverse biased, -15 volts is applied to the emitter of A6Q2. This reduced emitter voltage causes less current to flow through A6Q2 and less heat to be developed across the transistor.

The remaining input to the E/I Converter is the CW FILTER line. When the microprocessor commands that the CW filter be inserted, relay K1 is activated. (The CW filter is inserted when the sweep width is ≤50 MHz or when a CW mode has been selected from the front panel.) When K1 is activated, the R27-C16 network circumvents the YIG tuning coil current-driver loop by introducing an alternate negative-feedback path. This path reduces the noise current flowing through the coil; thereby quieting the YIG oscillator frequency output.

As shown in the A6 block diagram of Figure 7-56, the input to the Tracking Filter Voltage Generator (U2A-U2D) is the voltage ramp developed across R Sense (R15). This R15 voltage ramp is modified in slope (gain) and offset (if necessary) and used indirectly to tune the Band 1 YIG tracking filter. If the Band 1 YIG is supplying the output frequency, the **L YIG SEL** line will be TRUE closing U3C. When U3C closes it supplies the **TRACK FILTER 1** signal to the A10 PCB, which develops a tuning current for the tracking filter coil.

7-12.3 cont. & Figure 7-56.

The inputs to the Bandswitch/ROM Select Logic circuit (U1A, U1B, U1C, U10B, U10C) are the **FCEN/VPF** and **F CEN** voltage signals from the A5 PCB. The **FCEN/VPF** voltage is compared at U9A with a voltage representing 8 GHz and at U9B with a voltage representing 2 GHz. When the **FCEN/VPF** voltage equals or exceeds the 2 GHz voltage at U9B, the **L HET YIG SEL**, **L HET PIN SEL**, and **L HET OFFSET** lines go FALSE. When the **FCEN/VPF** voltage equals or exceeds the 8 GHz voltage at U9A, the **L YIG SEL**, **L YIG 1 FM COIL SEL**, and **L PIN SELECT 1** lines go FALSE and the **H SNB 1** line goes TRUE. When the **F CEN** voltage equals or exceeds the 8 GHz voltage at U9C, the **H SNR 1** line goes TRUE (**L ROM SEL** line goes FALSE).

In addition to the **FCEN/VPF** and **F CEN** analog voltage inputs, there are two logic control inputs to the Bandswitch/ROM Select Logic. These logic control inputs are **L RF OFF** and **L PIN SW OFF**. The **L RF OFF** input is from the microprocessor, via a latch on the A4 PCB. The **L PIN SW OFF** input is from the Sq Wave Sample/Hold Logic circuit on the A4 PCB (paragraph 7-11.1g). When either of these two logic input go TRUE, both the **L HET PIN SELECT** and **L PIN SELECT 1** lines go FALSE.

When the **L HET PIN SELECT** lines is FALSE, it reverse biases A14CR17 (Figure 7-58, Sheet 3). Reverse biasing CR17 causes A14Q5 to turn on, A14Q8 to turn on, and A14Q9 to turn off. When on, Q8 sources current into the PIN Switch. This current shunts the RF at J1 to ground and places a high attenuation between J1 and J5 – the RF OUT port.

Conversely, when the **L HET PIN SELECT** line is TRUE (.01-2 GHz Het Band is selected), CR17 is forward biased. Forward biasing CR17 causes Q5 to turn off, Q8 to turn off, and Q9 to turn on. When on, Q9 sinks current from the PIN Switch. This current biases the switch so that RF is passed from J1 to J5.

When the **L PIN SELECT 1** line changes states, the circuit composed of A14CR18, A14Q6, Q14Q10, and A14Q11 is used to operate the Osc 1 section of the PIN Switch. The operation of this circuit is identical to that described above for the CR17-Q5-Q8-Q9 circuit.

The inputs to the two Linearizing ROMs (U5, U6) are the **ROM Bus** lines from the microprocessor, via the A14U6 latch on the motherboard. The Linearizing ROMs are enabled by the TRUE state of the **L ROM SEL** line from the Bandswitch Logic circuit. When enabled these ROMs output eight bits of data to the A5 PCB.

The input to the PIN Driver/Linearizer (ALC) circuit (U7A, U8B, Q6, Q7) is from the A4 PCB. This circuit has two functions: (1) It provides the Band 1 ALC-loop-gain adjustment, and (2) it makes linear the relationship between the A4 PCB Level Amp output in Vdc (paragraph 7-11.1) and the RF power output in dBm. Control for the PIN Driver/Linearizer circuit is provided by the **H YIG SEL** line from the E/I Converter circuit. The **H YIG SEL** line is TRUE when the Band 1 YIG is supplying the output frequency. The output from this circuit is a current, **MOD DRIVER 1**. This current is supplied to the MOD (Modulator) component, on the RF Components Deck, via A14R34 (Figure 7-58, Sheet 3).

The input to the -5V Bias Supply (U7B, U8A, Q3, Q4, Q5) is the control line, **L RF OFF**. When the front panel RF ON switch is disengaged (out), the microprocessor sets this line TRUE. When **L RF OFF** is TRUE, the -5V Bias Supply is turned off; thus turning off the Band 1 YIG oscillator.

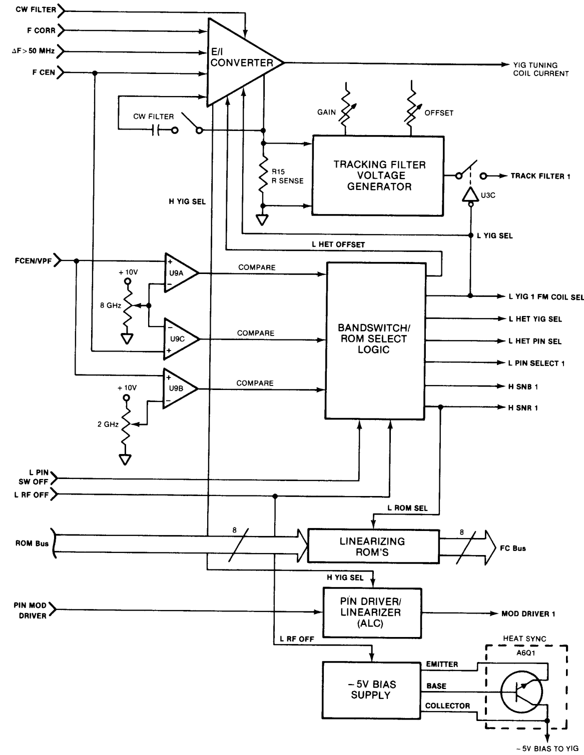


Figure 7-56. A6 Het/YIG Driver PCB (Assy. 660-D-8007) Block Diagram

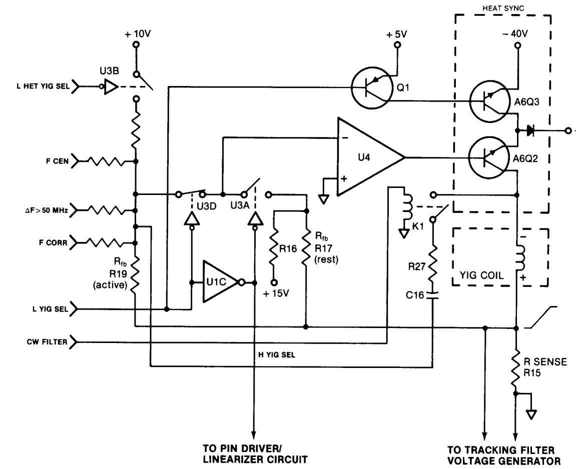


Figure 7-57. A6 HET/YIG Driver PCB E/I Converter Circuit Simplified Schematic

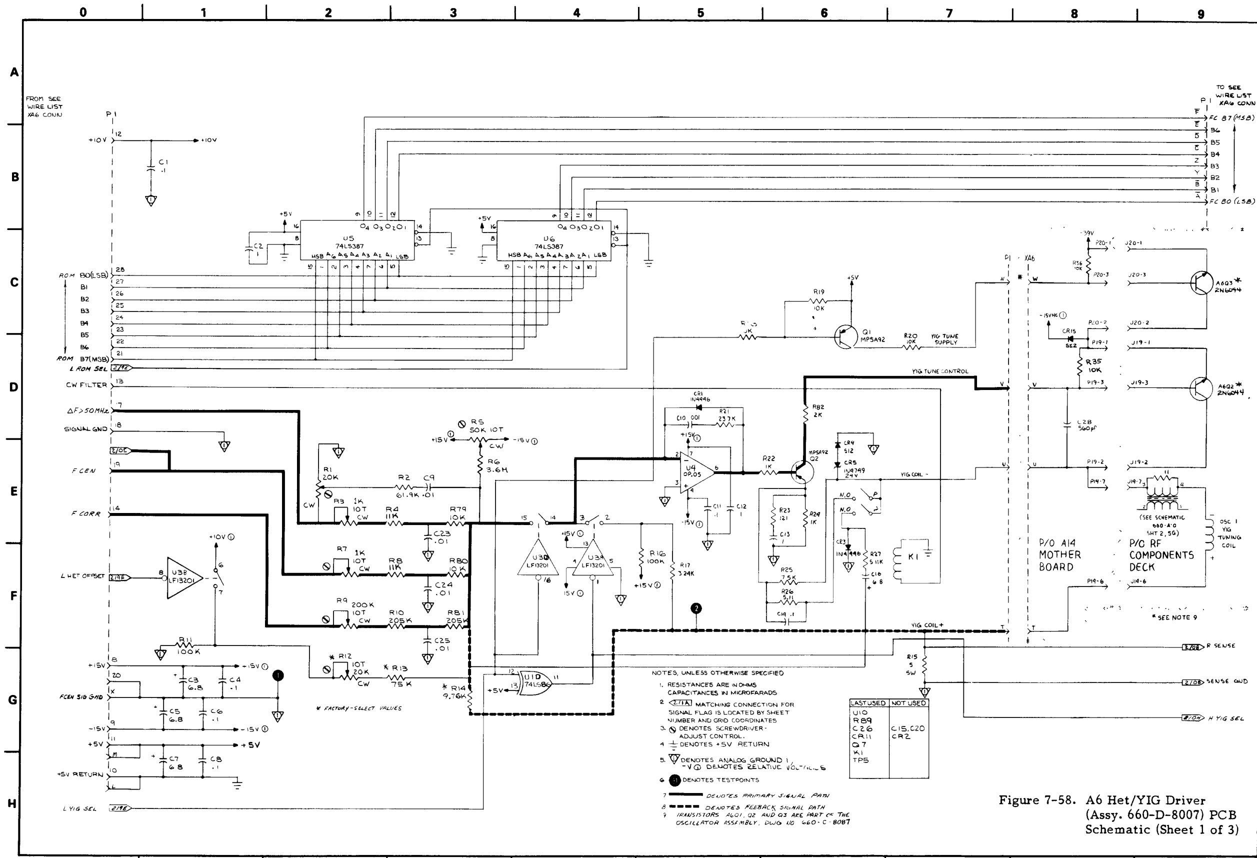
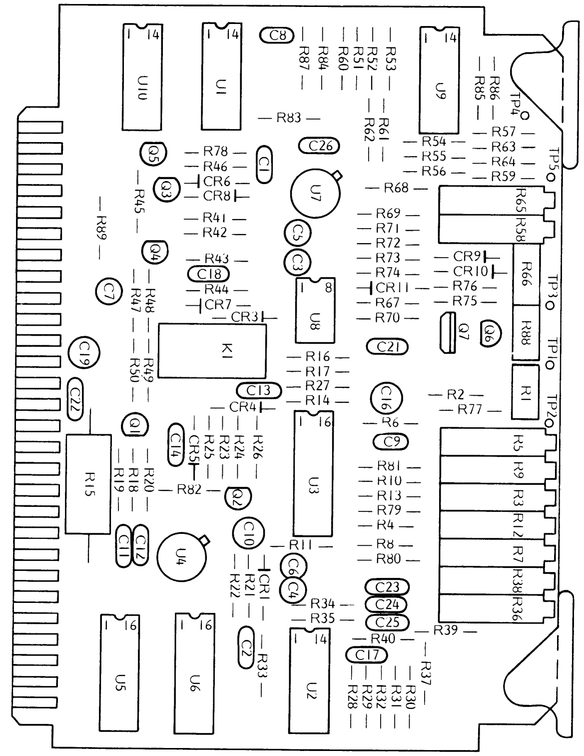


Figure 7-58. A6 Het/YIG Driver (Assy. 660-D-8007) PCB Schematic (Sheet 1 of 3)



A6 PCB Parts Locator Diagram

Figure 7-58. (Sheet 1)

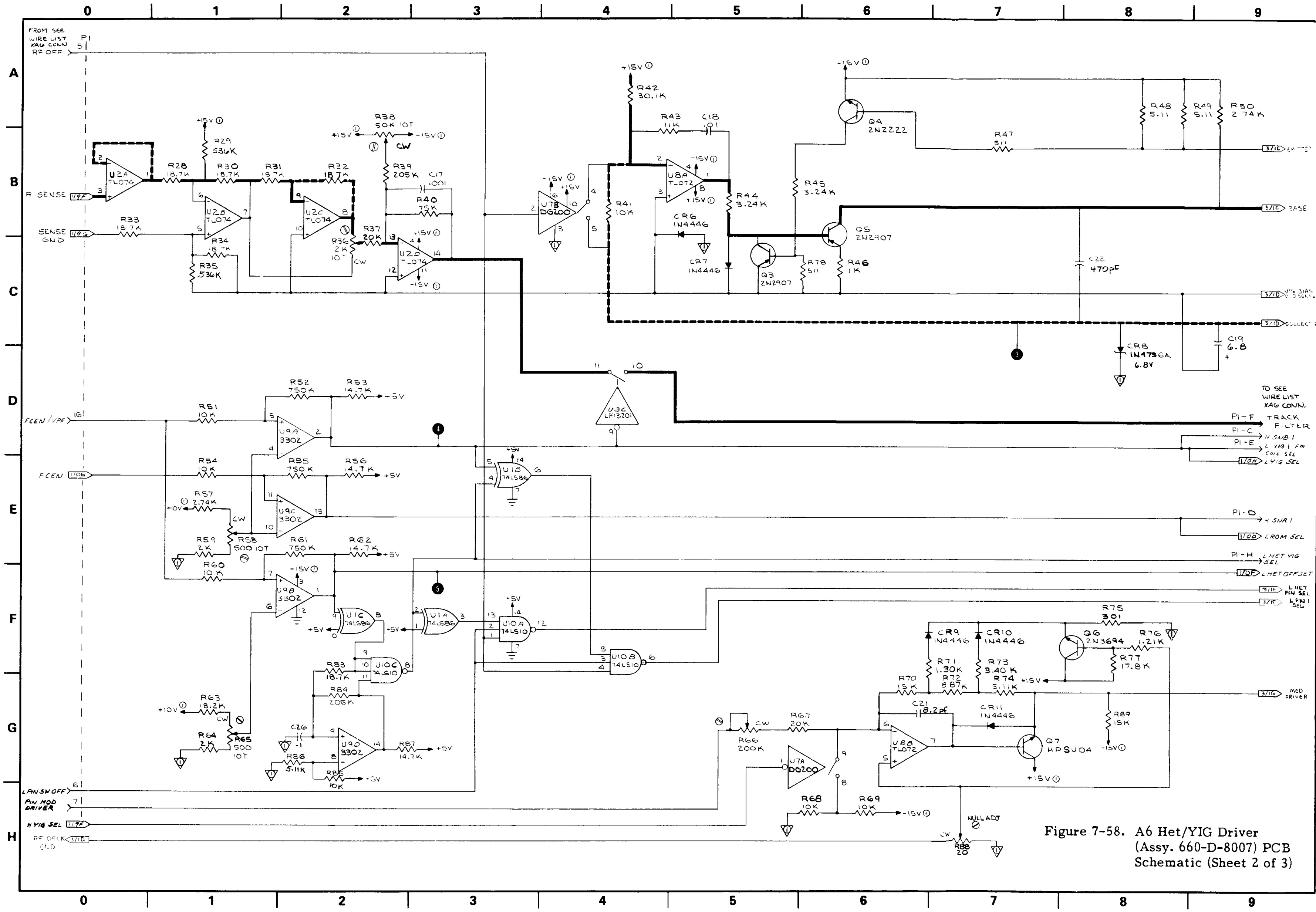


Figure 7-58. A6 Het/YIG Driver (Assy. 660-D-8007) PCB Schematic (Sheet 2 of 3)

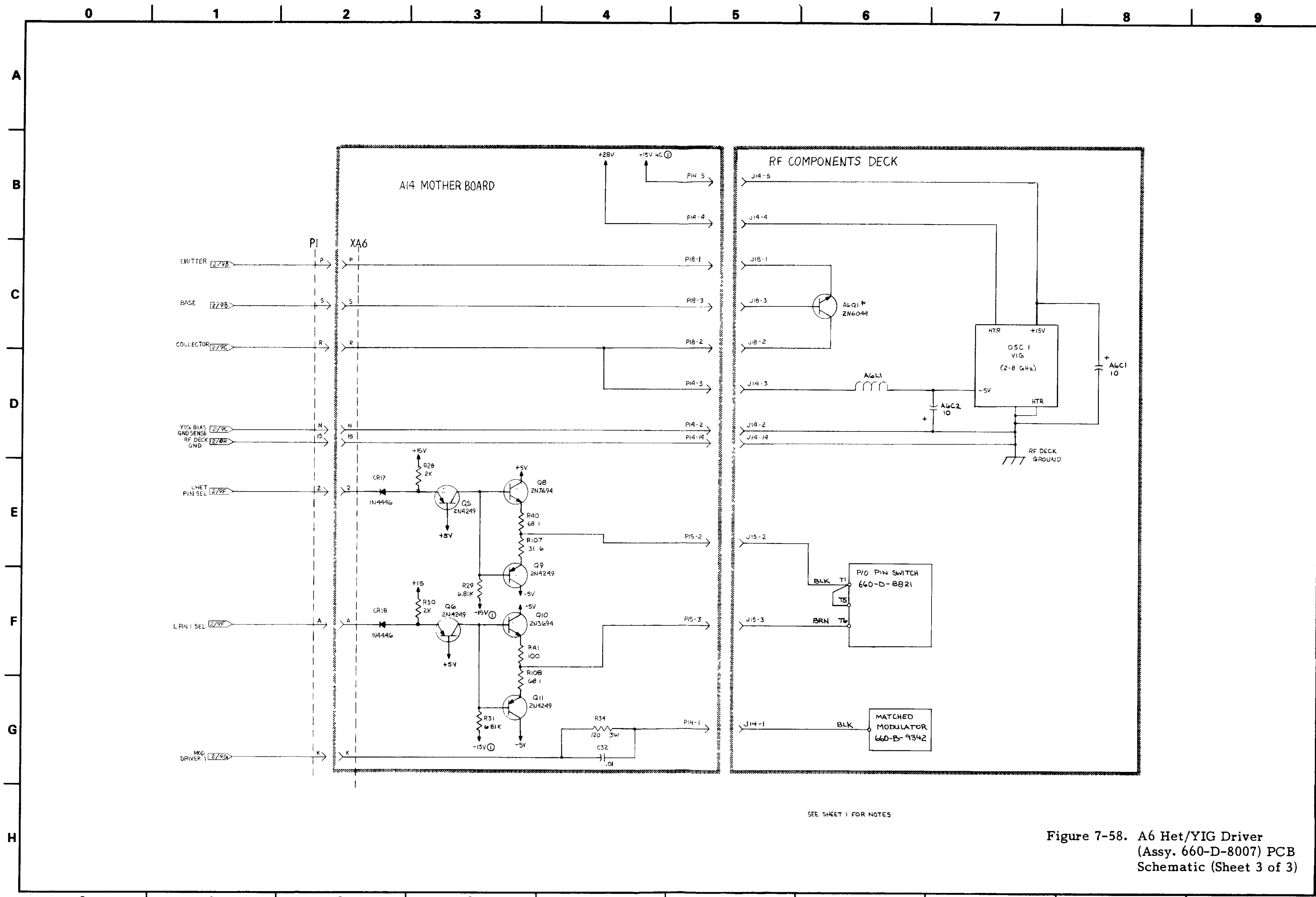
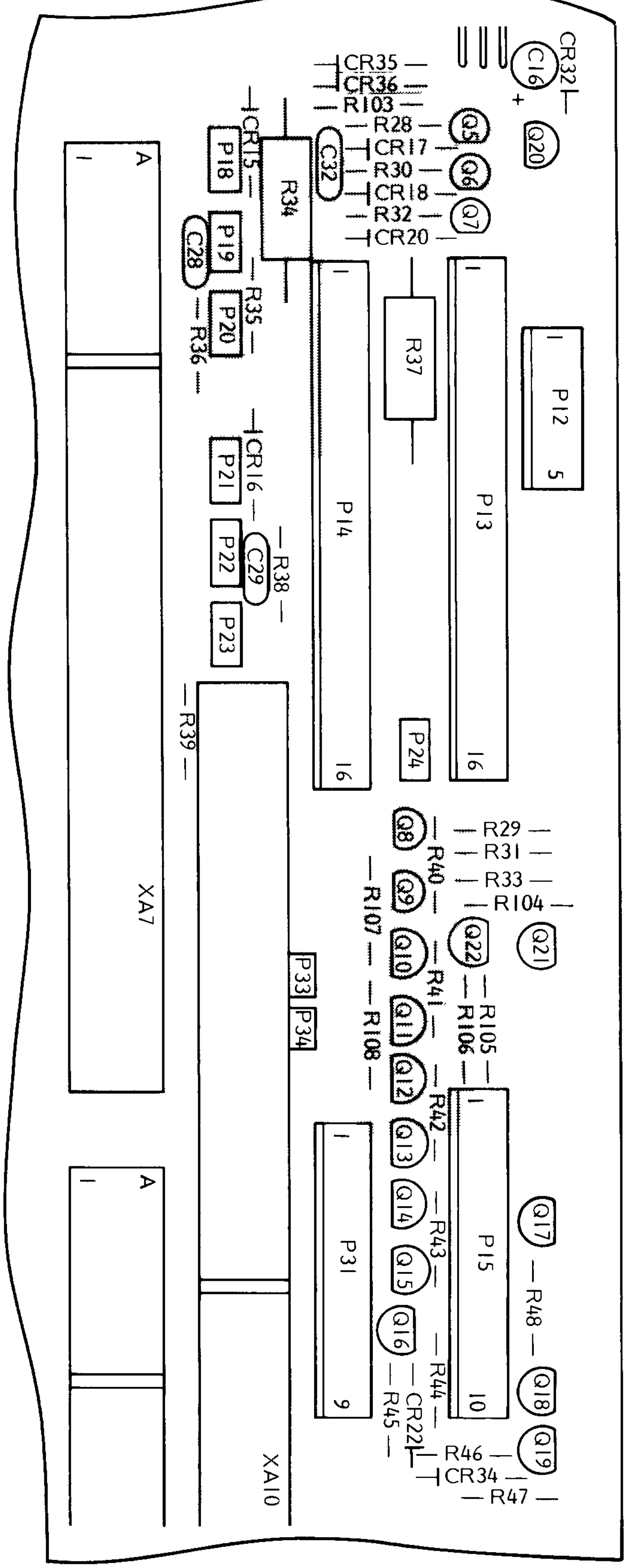
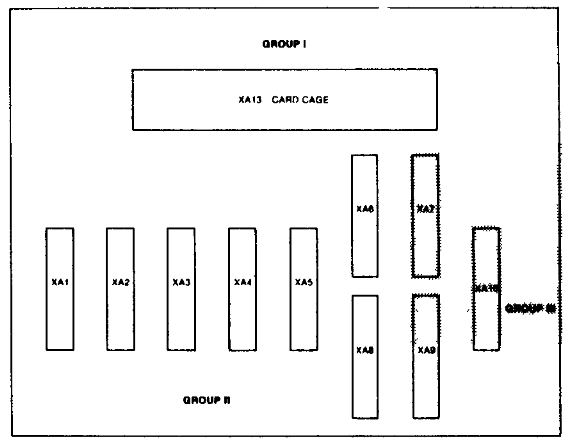


Figure 7-58. A6 Het/YIG Driver (Assy. 660-D-8007) PCB Schematic (Sheet 3 of 3)





Osc 1 YIG, PIN Drive, and PIN/Modulator Parts Locator Diagram

7-12.4 A7, A8 YIG Driver PCBs (Assy. 660-D-8008 and -8009) Circuit Description

The 660-D-8008 and -8009 YIG Driver PCBs are identical except for the polarity of their sweeping-bias supply outputs: The 8008 provides a negative-bias output, and the 8009 provides a positive-bias output. Both assemblies generate the following currents and voltages:

a. Tuning current for the Osc 2 and Osc 3 YIGs.
b. Sweeping-bias current for the Osc 2 and Osc 3 YIGs.
c. Modulating Current for the Osc 2 and Osc 3 PIN Switch attenuators.
d. Linearizer ROM output data.
e. Bandswitch logic voltages.

A block diagram for the 8008 and 8009 assemblies is shown in Figure 7-59. The 8008 assembly schematic (3 sheets) is given in Figure 7-60, and the 8009 assembly schematic (3 sheets) is given in Figure 7-61).

As shown in Figure 7-59, the **F CEN, ΔF>50 MHz**, and **F CORR** signals from the A5 PCB are summed together at the E/I Converter. The operation of this converter is similar to that described for the E/I Converter on the A6 PCB (Assy. 660-D-8007). The 8008 and 8009 E/I Converters differ from A6 by having no heterodyne offset and by having different rest frequencies. The rest frequency is 8 GHz for the A7 YIG and 12.4 GHz for the A8 YIG.

The input to the Sweeping-Bias Supply (U7A-U7D, Q5-Q8, U1B) is from the R Sense resistor (R25). The operation of this bias supply is similar for both the 8008 and 8009 assemblies. The only operational difference is in the polarity of the bias-voltage signal as it goes through the various voltage generation stages. The other circuit differences between the two assemblies are in the values and types of some of the components used: Several resistors have different values and all of the transistors are opposite in type (NPN on one assembly and PNP on the other).

NOTE

Some YIG oscillator types do not require a swept bias. When one of these oscillator-types is installed, the output from the sweeping-bias supply will be a fixed voltage.

The inputs to U2C, the PIN Switch control gate, are the **L RF OFF** and **L PIN SW OFF** lines from the A4 PCB and the **H YIG SEL** line from the Bandswitch Logic. When all three of these inputs are HIGH, the **L PIN SELECT 2** line is TRUE for the A7 PCB, and the **L PIN SELECT 3** line is TRUE for the A8 PCB. The **RF OFF** line is HIGH when the front panel **RF ON** switch is depressed (On). The **PIN SW OFF** line is HIGH during the forward sweep and goes LOW at the start of the sweep retrace (providing RETRACE RF is not On). The **YIG SEL** line is HIGH for the A7 PCB when the Osc 2 YIG is providing the output frequency. The line is HIGH for the A8 PCB when the Osc 3 YIG is providing the output frequency.

The changing logic states of the two PIN SELECT lines operate the Osc 2 and Osc 3 sections of the PIN Switch in a manner similar to that described in paragraph 7-12.3 for the Het Band (L HET PIN SELECT). The A14 PCB PIN Switch drive circuit for Osc 2 consists of CR20, Q7, Q12, Q13, and associated components (Figure 7-60, Sheet 3). The Osc 3 drive circuit consists of CR22, Q16, Q15, Q14, and associated components (Figure 7-61, Sheet 3).

The input to the PIN Driver/Linearizer (U1A, U4B, Q3, Q4) is the **PIN MOD DRIVER** voltage signal from the A4 PCB. The operation of this circuit is the same as that described for the Pin Driver/Linearizer circuit on the A6 PCB (paragraph 7-12.3). The PIN Modulator resistor for the Osc 2 attenuator, located inside the PIN Switch, is A14R37. The Osc 3 attenuator resistor is A14R50.

The inputs to the Bandswitch/ROM Select (U8A-U8D) are as follows:

a. The **FCEN/VPF** and **F CEN** voltage signals from the A5 PCB.

b. The **H SNB** and **H SNR** logic control lines from the preceeding oscillator's YIG driver PCB. For example, for the A7 PCB the lines are **H SNB 1** and **H SNR 1** from the A6 PCB. And for the A8 PCB, the lines are **H SNB 2** and **H SNR 2** from the A7 PCB.

The **FCEN/VPF** and **F CEN** voltages are compared with a voltage representing 12.4 GHz for the A7 YIG. When the **FCEN/VPF** voltage equals or exceeds the comparison voltage, and if the applicable **H SNB** line is TRUE, the following occurs:

c. The applicable PCB's **L YIG SEL** and **H YIG SEL** lines go FALSE.

d. The **H SNB 2** line for the A7 PCB goes TRUE.

When the **F CEN** voltage equals or exceeds the comparison voltage and if the applicable **H SNR** line is TRUE, the following occurs:

e. The **H SNR 2** line for the A7 PCB goes TRUE.

f. The applicable PCB's **L ROM SEL** line goes FALSE.

The input to the Linearizing ROM's (U5, U6) is the **ROM Bus** from the microprocessor, via the A14U6 latch on the Motherboard. The operation of this circuit is the same as that described for the Linearizing ROM's on the A6 PCB.

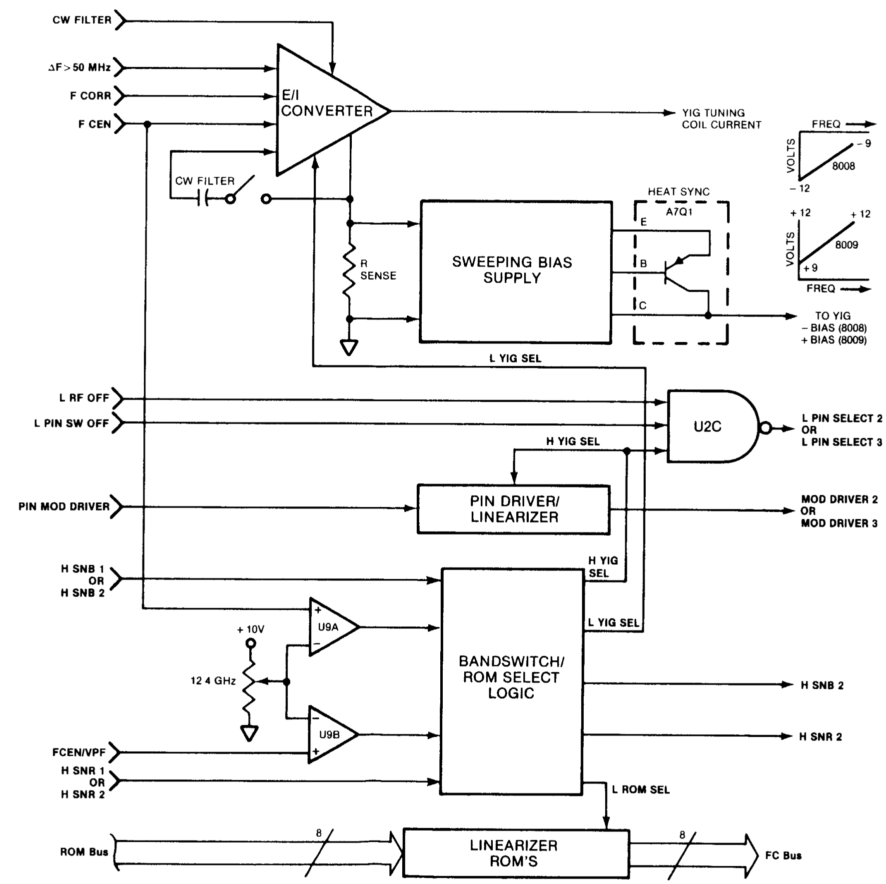


Figure 7-59. A7/A8 YIG Driver PCB (Assy. 660-D-8008, -8009) Block Diagram

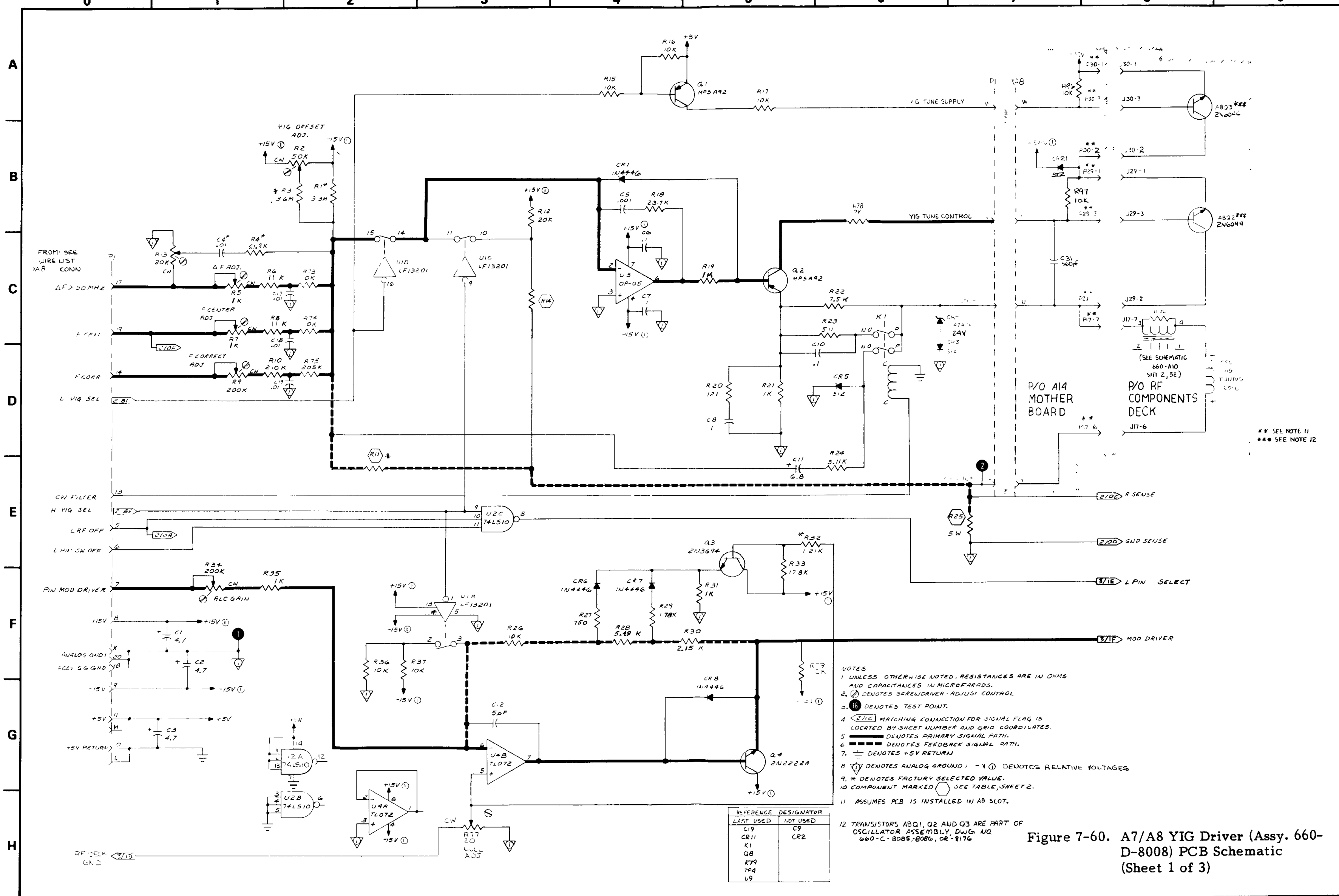
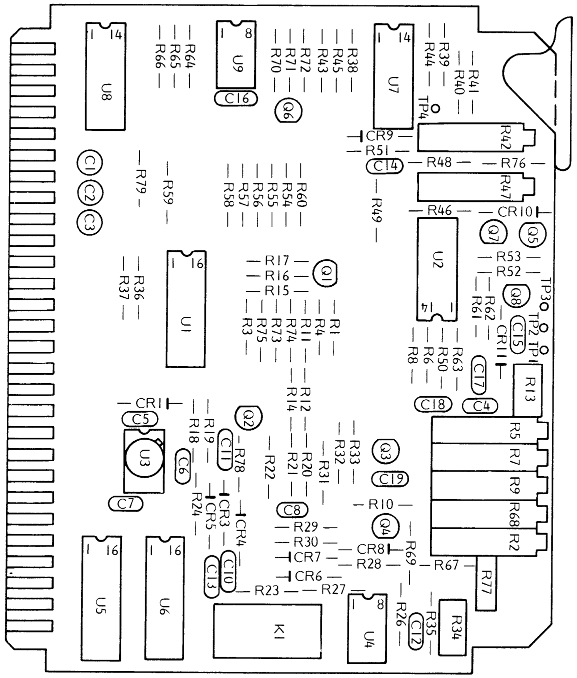
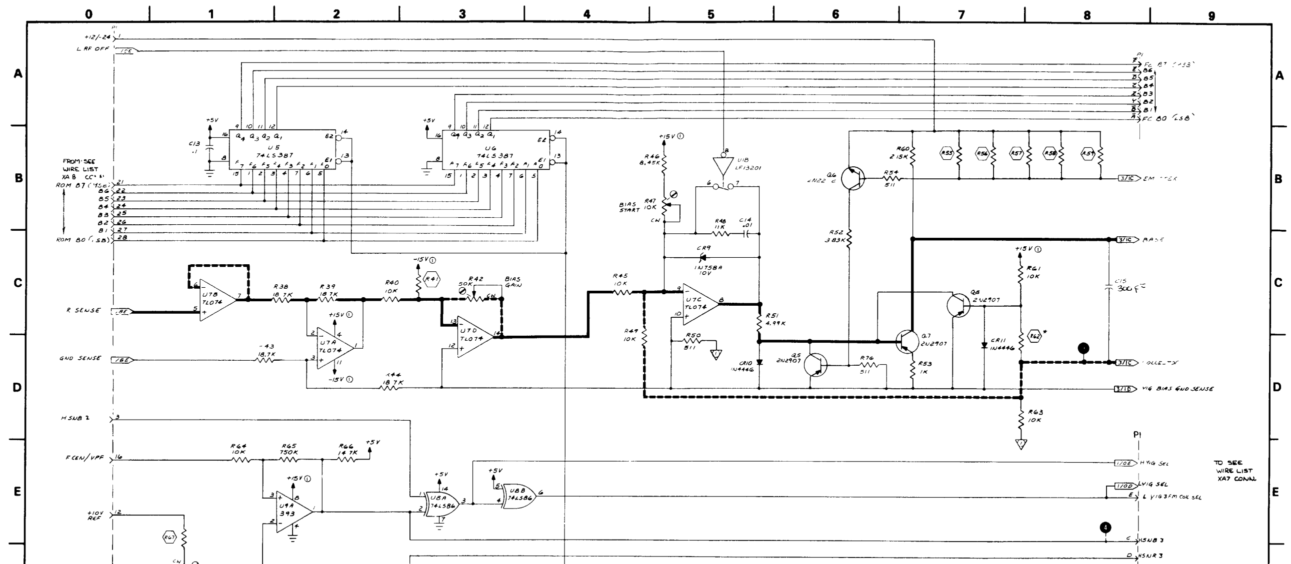


Figure 7-60. A7/A8 YIG Driver (Assy. 660-D-8008) PCB Schematic (Sheet 1 of 3)



A7/A8 PCB Parts Locator Diagram



MODEL	R11	R14	R41	R55 THRU R57	R58	R59	R62	R67	R25	PC ASSY	SLOT
6637/6647 KU-BAND (WJ)	7.[illegible]K	3.16K	60K	8.06	8.06	.5	8.66K	5.11	5	660-D-8008-4	A8
6637/6647 X-BAND (WJ)	7.[illegible]K	2.05K	100K	8.06	8.06	.5	10.5K	866	5	660-D-8008-5	A7

Figure 7-60. A7/A8 YIG Driver (Assy. 660-D-8008) PCB Schematic (Sheet 2 of 3)

parts locator

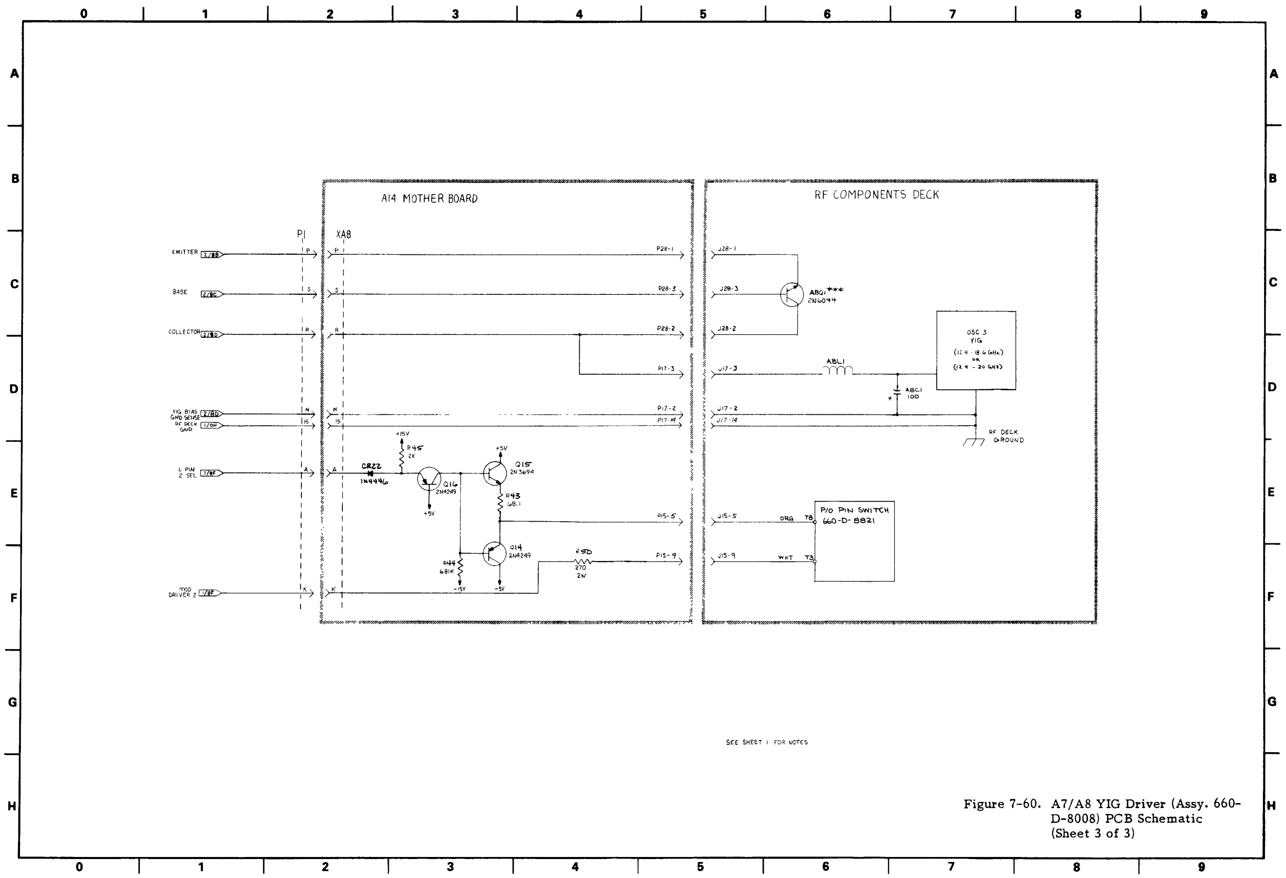
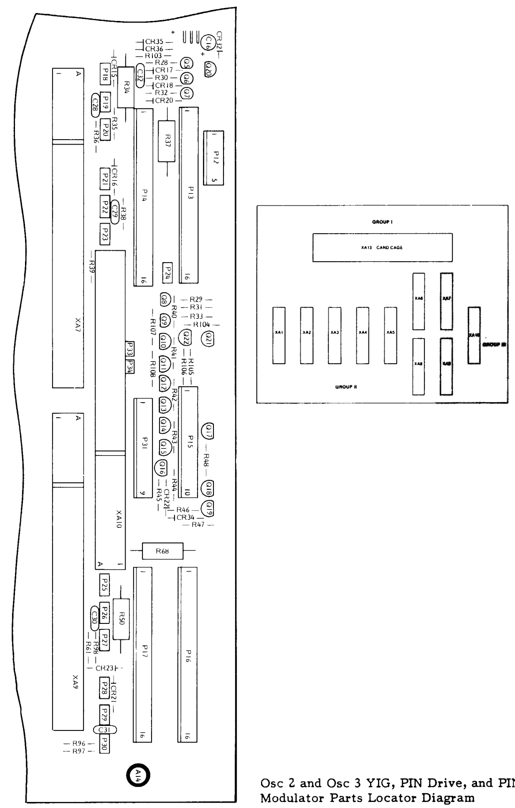
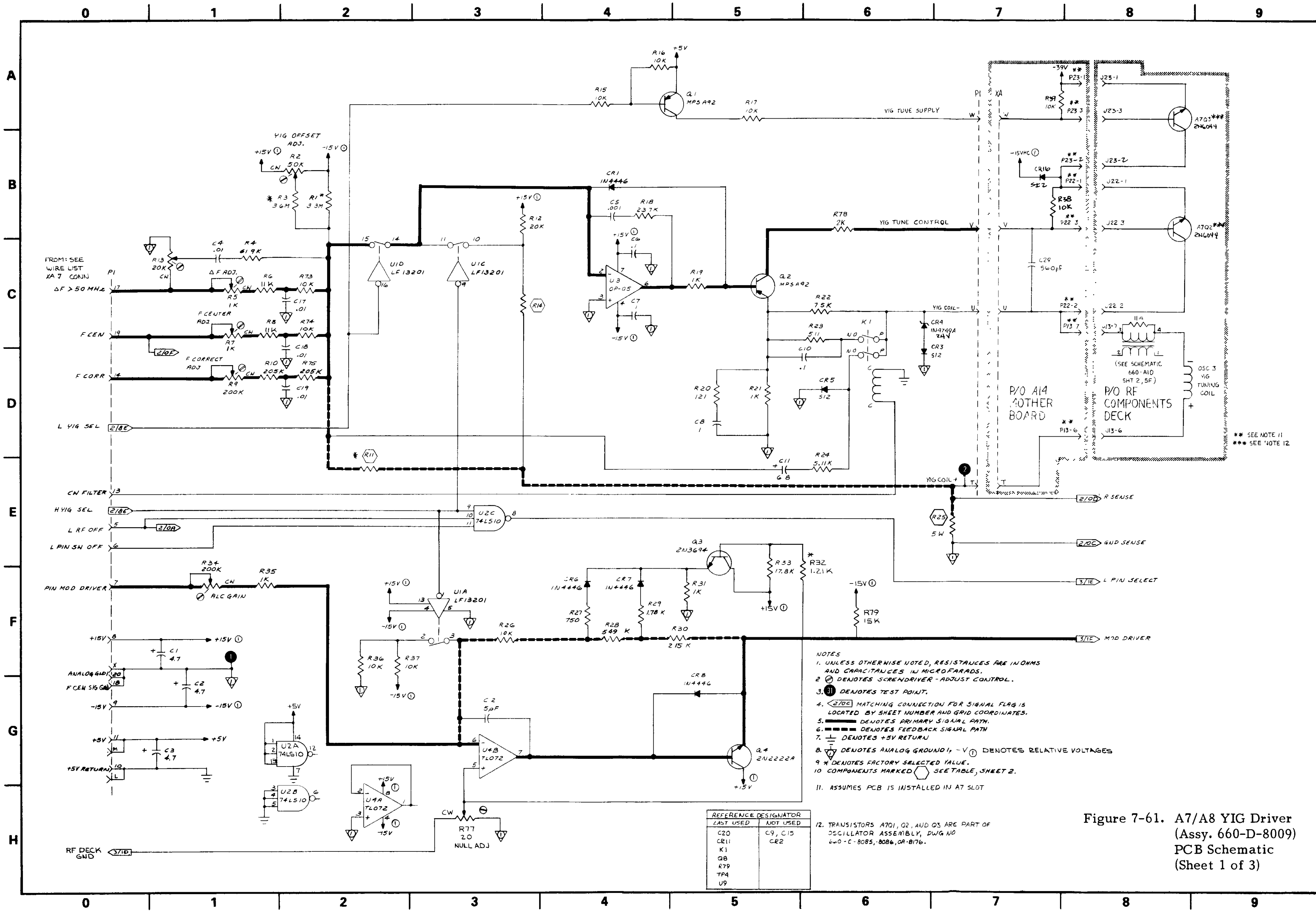


Figure 7-60. A7/A8 YIG Driver (Assy. 660-D-8008) PCB Schematic (Sheet 3 of 3)



Osc 2 and Osc 3 YIG, PIN Drive, and PIN Modulator Parts Locator Diagram

Figure 7-60. (Sheet 3)

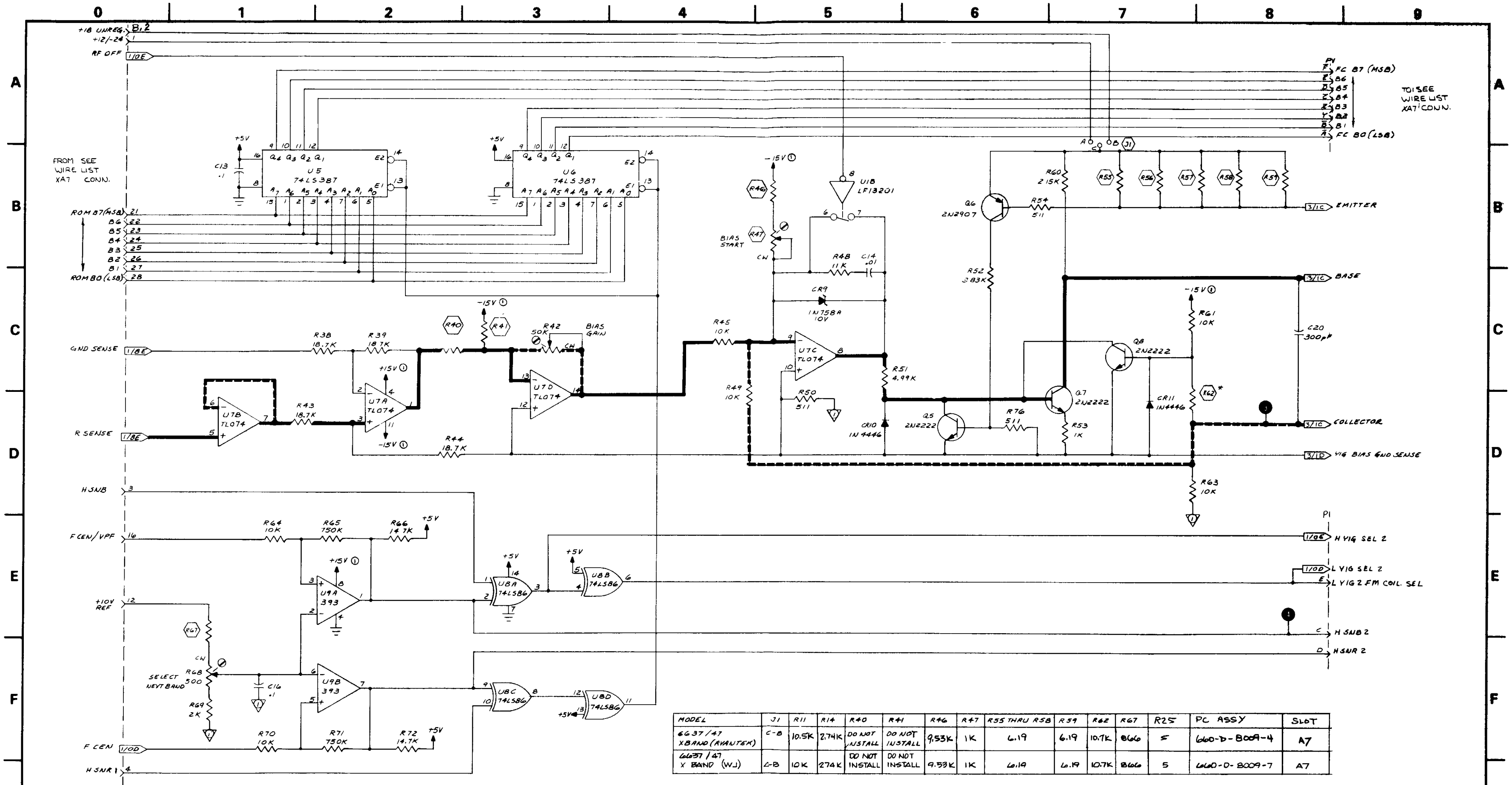


NOTES

1. UNLESS OTHERWISE NOTED, RESISTANCES ARE IN OHMS AND CAPACITANCES IN MICROFARADS.
2. ⊘ DENOTES SCREWDRIVER - ADJUST CONTROL.
3. (31) DENOTES TEST POINT.
4. ⟨2/0C] MATCHING CONNECTION FOR SIGNAL FLAG IS LOCATED BY SHEET NUMBER AND GRID COORDINATES.
5. ▬▬ DENOTES PRIMARY SIGNAL PATH.
6. ▬ ▬ ▬ DENOTES FEEDBACK SIGNAL PATH
7. ⏚ DENOTES +5V RETURN
8. ▽(1) DENOTES ANALOG GROUND 1, −V(1) DENOTES RELATIVE VOLTAGES
9. * DENOTES FACTORY SELECTED VALUE.
10. COMPONENTS MARKED ⬡ SEE TABLE, SHEET 2.
11. ASSUMES PCB IS INSTALLED IN A7 SLOT
12. TRANSISTORS A7Q1, Q2, AND Q3 ARE PART OF OSCILLATOR ASSEMBLY, DWG NO 660-C-8085, -8086, OR -8176.

REFERENCE DESIGNATOR	
LAST USED	NOT USED
C20	C9, C15
CR11	CR2
K1	
Q8	
R79	
TP4	
U9	

Figure 7-61. A7/A8 YIG Driver (Assy. 660-D-8009) PCB Schematic (Sheet 1 of 3)



MODEL	J1	R11	R14	R40	R41	R46	R47	R55 THRU R58	R59	R62	R67	R25	PC ASSY	SLOT
6637/47 XBAND (AVANTEK)	C-B	10.5K	2.74K	DO NOT INSTALL	DO NOT INSTALL	9.53K	1K	6.19	6.19	10.7K	866	5	660-D-8009-4	A7
6637/47 X BAND (WJ)	6-B	10K	274K	DO NOT INSTALL	DO NOT INSTALL	9.53K	1K	6.19	6.19	10.7K	866	5	660-D-8009-7	A7

FOR NOTES SEE SHEET 1.

Figure 7-61. A7/A8 YIG Driver (Assy. 660-D-8009) PCB Schematic (Sheet 2 of 3)

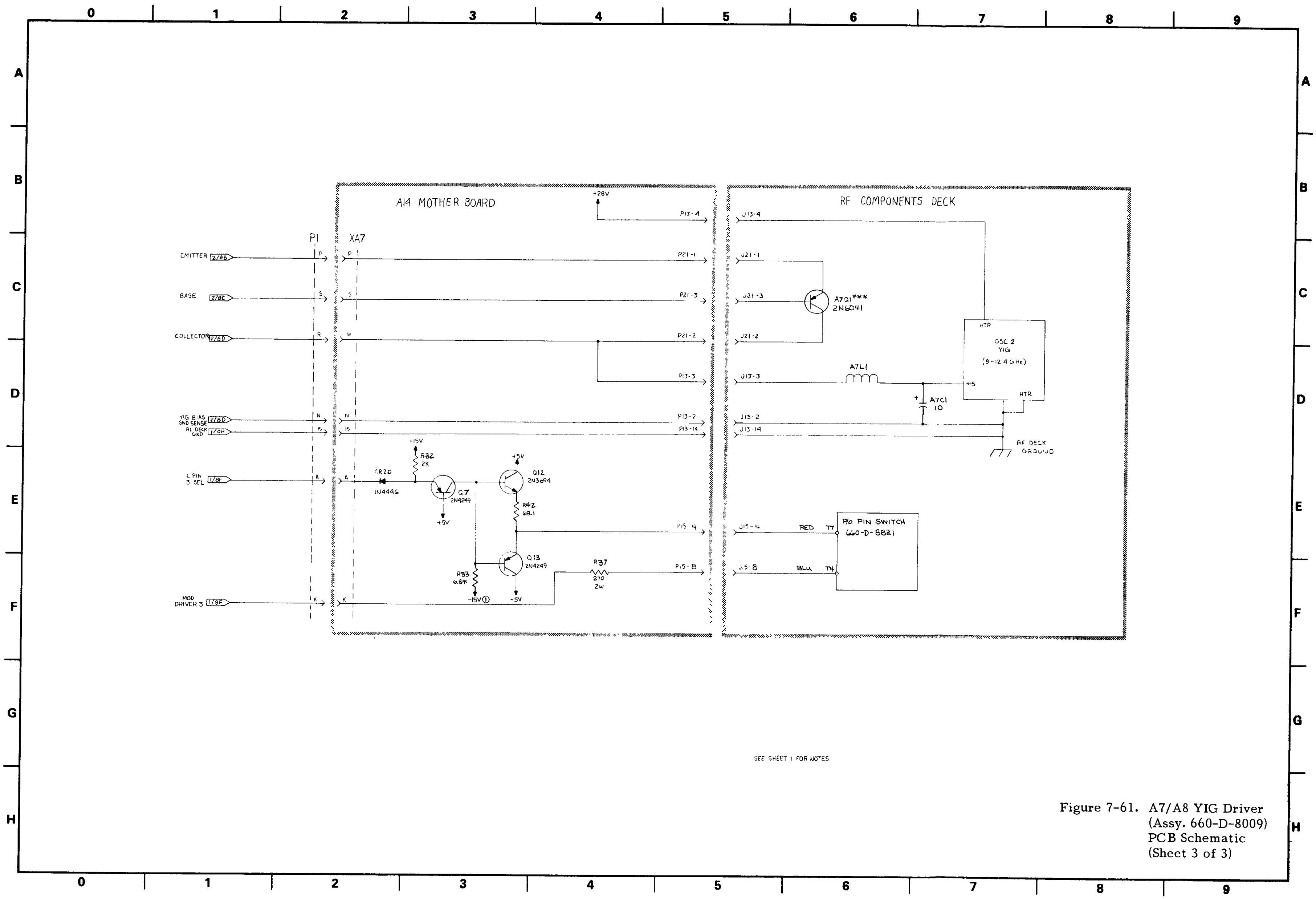


Figure 7-61. A7/A8 YIG Driver (Assy. 660-D-8009) PCB Schematic (Sheet 3 of 3)

7-12.5 A5 Frequency Instruction and A6-A8 YIG Driver PCBs Troubleshooting Information and Data

Error Codes 09, 10, 11, 12, and 14 (Error Code 13 is not used) report on the status of the A5 Frequency Instruction and A6-A8 YIG Driver PCBs. The microprocessor routines associated with these error codes test the A5-A8 PCBs using three methods. In the first method (Error Code 09), the A5 F Center DAC is made to output mid-band frequency data in the .01 to 2 GHz HET band to the A6 PCB. The routine then monitors the **L HET YIG SEL** line for activity. If the line fails to go HIGH, indicating the completion of the Heterodyne Down Converter sweep, "Error 09" is displayed.

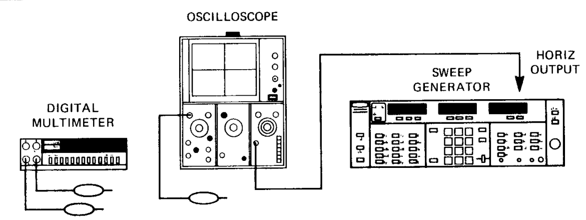
In the second method (Error Codes 10 through 12), the F Center DAC (U7) is made to output mid-band frequency data in each of the Osc 1, Osc 2, and Osc 3 YIG bands, sequentially. At the end of each YIG-band's error-code test, a bit pattern formed by the four **YIG FM COIL SEL** and **SNR** lines (Figure 7-63) is applied to latch buffer A14U7. This bit pattern is compared with test data stored in A12 read-only memory (ROM). If the bit-pattern and ROM test data do not compare favorably, the appropriate error code is displayed.

In the third method (Error Code 14), both the Sweep Width (ΔF) DAC (U24) and the Step Freq DAC (U19) are tested. In this method, (1) the F Center DAC is set to mid-band; (2) the Sweep Width (ΔF) DAC is set to provide a full-band sweep; and (3) the Step Freq DAC is set to 0, then 10 volts. This Step Freq DAC operation simulates a full-band sweep. At the 10V point on this simulated sweep, the **YIG FM COIL SEL/SNR** bit pattern is compared with the ROM test data. If the comparison is unfavorable, "Error 14" is displayed.

To accomplish the A5-A8 error-code tests, the A5 F Center DAC is set as follows:

a. to 1 GHz for Error Code 09,
b. to 5 GHz for Error Code 10,
c. to 10.2 GHz for Error Code 11,
d. to 15.5 GHz for Error Code 12 (6637 and 6647),
e. to 16.2 GHz for Error Code 12 (6638 and 6648), and
f. to 9.3 GHz (6637 and 6647) or 10 GHz (6638 and 6648) for Error Code 14.

The test equipment setup for troubleshooting Error Codes 09-14 is provided in Figure 7-62; the troubleshooting flowcharts are provided in Figures 7-64 through 7-68.

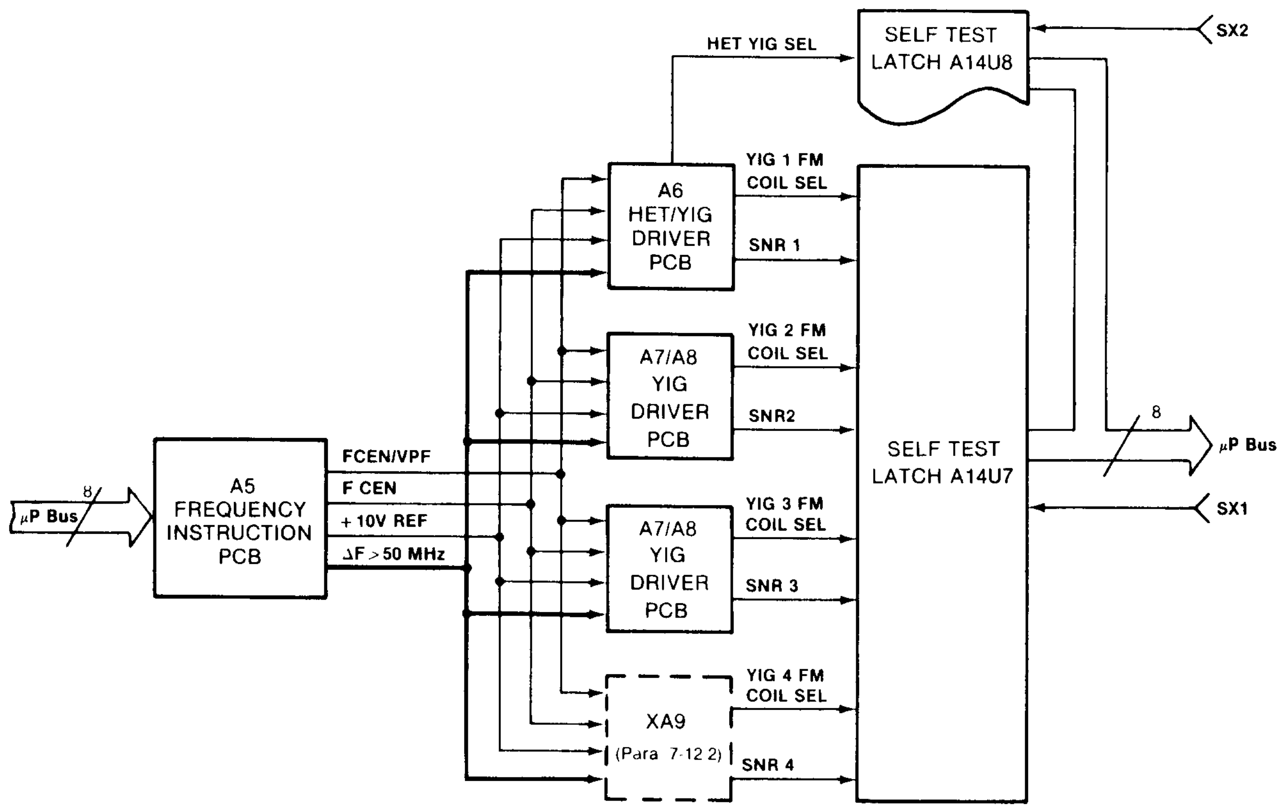


SWEEP GENERATOR CONTROL SETTINGS

FREQUENCY RANGE: CW F0 (Error Codes 09 thru 12)
FULL (Error Code 14)
TRIGGER: AUTO
MARKERS: A11 Off
LEVELING: INTERNAL
LEVEL: 0 dBm
SWEEP TIME: 10 ms
RETRACE RF: Off

RF ON: On
RF SLOPE: Off
F0: 1 GHz (Error Code 09)
5 GHz (Error Code 10)
10 GHz (Error Code 11)
15 GHz (Error Code 12)
9.3 GHz (Error Code 14)

Figure 7-62. Test Equipment Setup for Troubleshooting Error Codes 09 thru 14



A14U7 Input Bit Pattern for Error Code Test Frequencies

SIGNAL MNEMONIC	1 GHz	5 GHz	10 GHz	15 GHz	A14U7 PINS
SNR 4	H	H	H	H	18
SNR 3	L	L	L	L	17
SNR 2	L	L	L	H	14
SNR 1	L	L	H	H	13
YIG 4 FM COIL SEL	H	H	H	H	8
YIG 3 FM COIL SEL	H	H	H	L	7
YIG 2 FM COIL SEL	H	H	L	H	4
YIG 1 FM COIL SEL	L	L	H	H	3

Figure 7-63. Error Codes 9 thru 14, Diagnostic (Self Test) Circuit

GENERAL INFORMATION FOR FIGURE 7-64 THRU 7-68 FLOWCHARTS

1. Before starting any of the flowcharts, check the following dc voltages at connector P1.
   a. +15V, pins 8 (+) and 20 (-).
   b. -15V, pins 9 (-) and 20 (+).
   c. +10V, pins 12 (+) and 20 (-).
   d. +5V, pins 11 (+) and 10 (-).
2. Logic levels are TTL.

Table 7-15. F Center DAC Voltages (Formula: $VDAC = (10/F_{High\ End}) \times (F_{Desired})$

MODEL	1 GHz*	5 GHz*	10 GHz*	15 GHz*
6637		2.688V	5.376V	8.065V
6638		2.500V	5.000V	7.500V
6647	0.538V	2.688V	5.376V	8.065V
6648	0.500V	2.500V	5.000V	7.500V

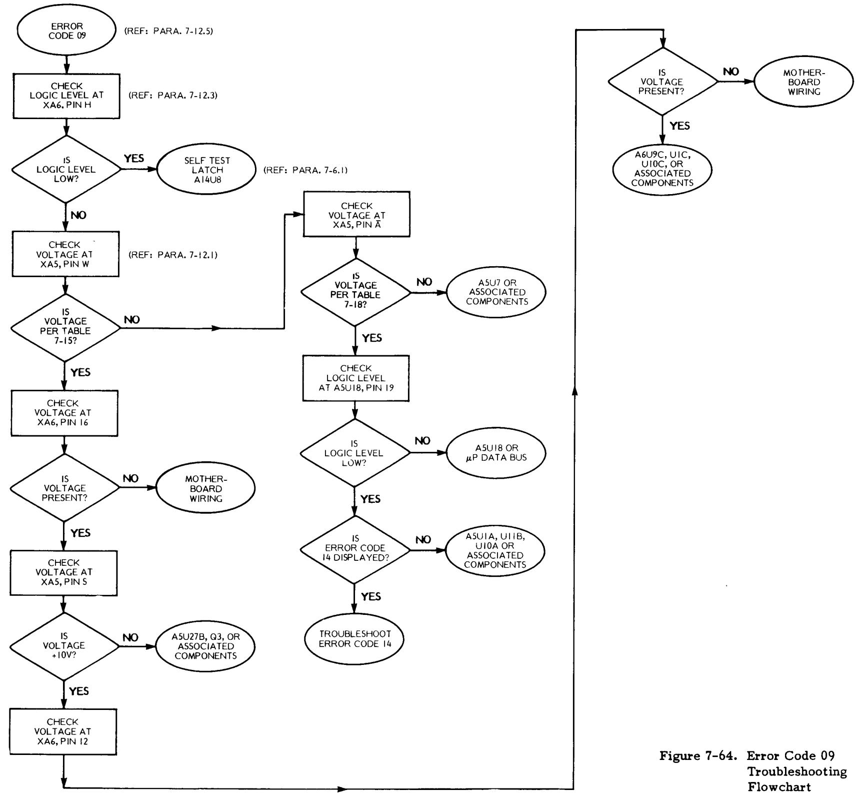


Figure 7-64. Error Code 09 Troubleshooting Flowchart

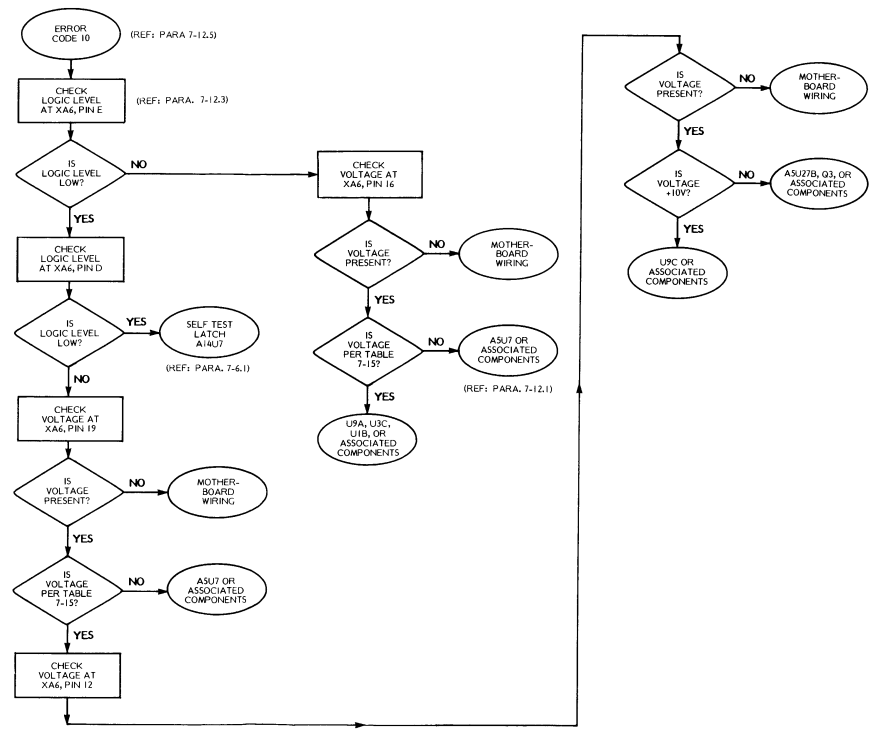


Figure 7-65. Error Code 10 Troubleshooting Flowchart

Figure 7-64.

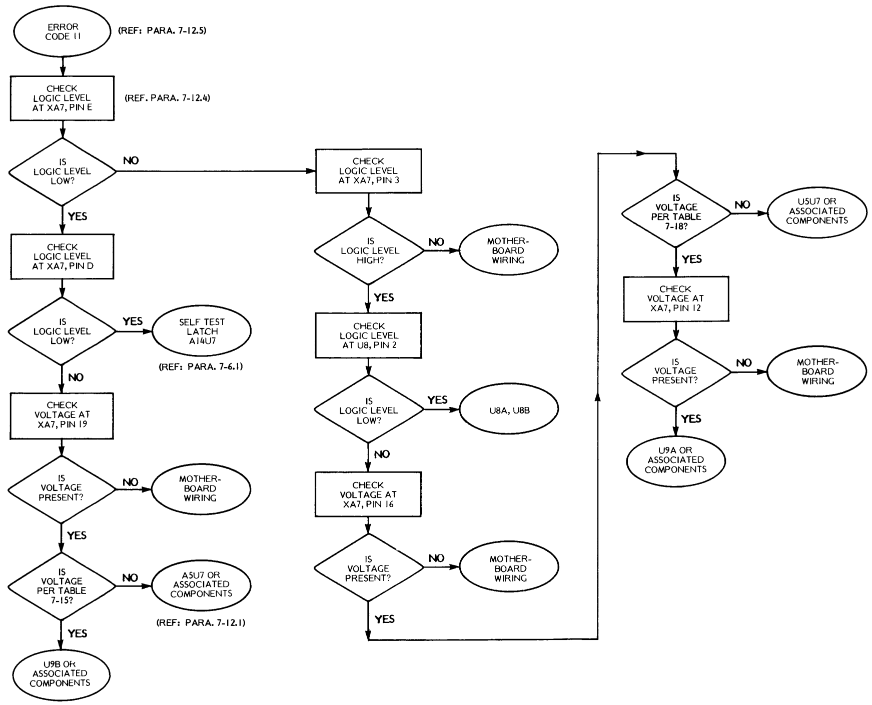


Figure 7-66. Error Code 11 Troubleshooting Flowchart

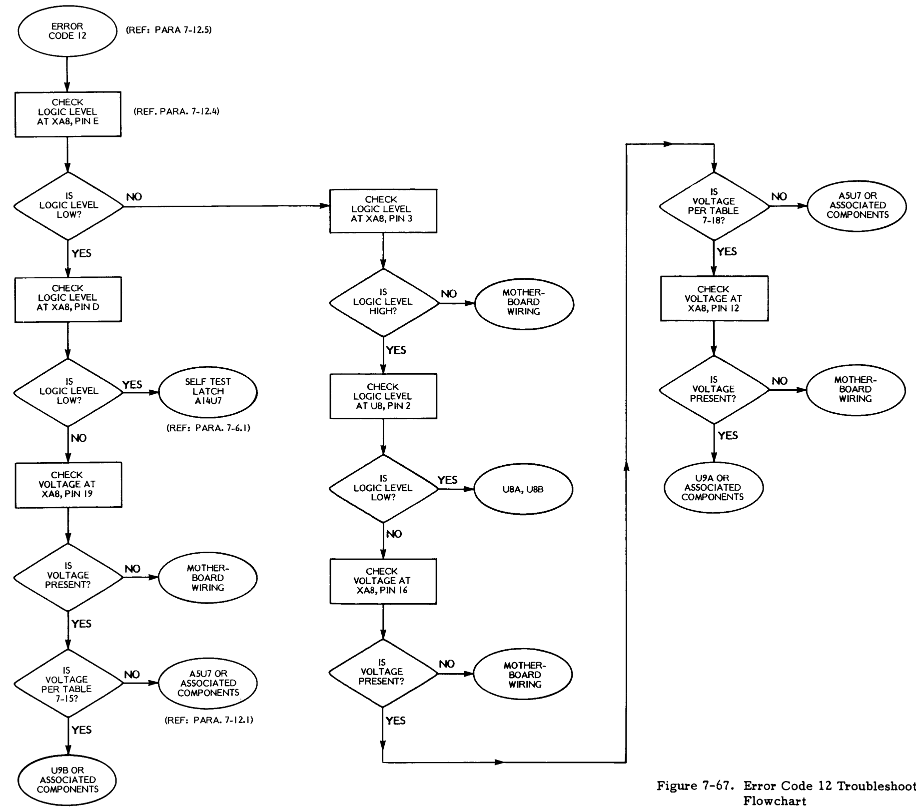
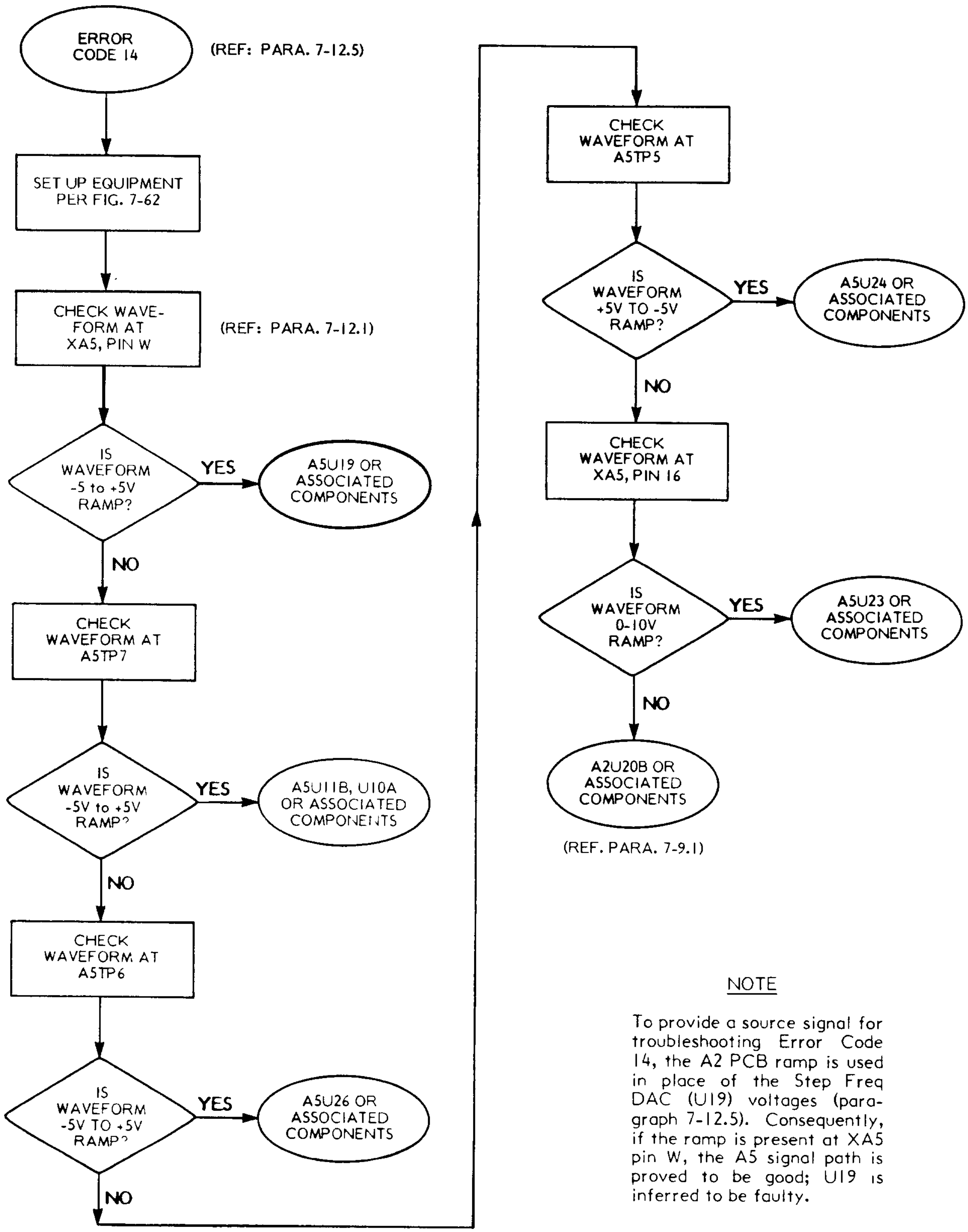


Figure 7-67. Error Code 12 Troubleshooting Flowchart

Figure 7-66.



NOTE

To provide a source signal for troubleshooting Error Code 14, the A2 PCB ramp is used in place of the Step Freq DAC (U19) voltages (paragraph 7-12.5). Consequently, if the ramp is present at XA5 pin W, the A5 signal path is proved to be good; U19 is inferred to be faulty.

Figure 7-68. Error Code 14 Troubleshooting Flowchart

7-13 A10 FM/ATTENUATOR PCB

7-13.1 A10 FM/Attenuator PCB Circuit Description

The A10/FM Attenuator PCB has two primary functions. The PCB generates currents that control (1) FM modulation for the YIG oscillators, (2) drive for the 2 to 8 GHz YIG tracking filter, and (3) operation of the optional 70dB or 110dB Step Attenuator. In addition, this PCB generates the End of Band (EOB) signal that is used on the A2 PCB (paragraph 7-9.1). A functional block diagram of the A10 circuitry is shown in Figure 7-69; the schematic diagram (2 sheets) is shown in Figure 7-70.

The FM input enters this PCB on either the **EXT FM INPUT** signal line, the **ΔF≤50 MHz** signal line, or on both concurrently (Figure 7-69). The **ΔF≤50 MHz** signal line is from the A5 Frequency Instruction PCB. If a delta-frequency sweep mode (ΔF F0, ΔF F1) has been selected and the sweep width (ΔF) is 50 MHz or less, this input is a voltage ramp. As described in paragraph 7-12.1, the amplitude of this ramp depends on the sweep width. For a sweep width of 50 MHz, the amplitude of the ramp is 10 volts (from -5V to +5V). For sweep widths less than 50MHz, the amplitude of the ramp is proportionally less than 10 volts.

The **EXT FM INPUT** signal line is from the rear panel EXT FM Ø LOCK INPUT connector, which is an isolated-shield (or floating ground) type connector. The connector's center conductor and shield leads provide the inputs for the noise-cancelling Diff Input circuit (U4). The output of the U4 circuit is the difference between the two input signals. This ouput is applied to the EXT FM ENABLE switch (U5). This switch is controlled by the **H EXT FM ENABLE** control line from the microprocessor, via a latch on the A2 PCB. If the front panel FM AND PHASELOCK pushbutton is engaged, this control line is TRUE. When TRUE, the line causes the EXT FM ENABLE switch to close, allowing the EXT FM INPUT signal to supply an input to the Variable Gain/Inverter stage.

The Variable Gain/Inverter stage (U7) provides a voltage gain for the FM input signal. The amount of gain this stage provides depends on which YIG oscillator is presently supplying the output frequency. As described in the overall circuit description (paragraph 7-4), the sweep generator uses three YIG oscillators to sweep the 6637 and 6638 frequency bands, and three YIG oscillators plus a down converter (HET band) to sweep the 6647 and 6648 frequency bands. A LOW logic state on one of the four **YIG FM COIL SEL** lines is used to select the U7 feedback resistor (Figure 7-70), thereby setting circuit gain. At any given time, only one **YIG SEL** line is LOW, signifying that the associated YIG oscillator is presently providing the sweep generator output frequency. In a full-band frequency sweep, the sequence in which these lines go from HIGH to LOW is as follows:

a. At the start of the sweep (10 MHz or 2 GHz), the **YIG 1** line is low and the **YIG 2, 3,** and **4** lines are all HIGH.

b. When the sweep reaches 8 GHz, the **YIG 1** line goes HIGH and the **YIG 2** line goes low.

c. When the sweep reaches 12.4 GHz, the **YIG 2** line goes HIGH and the **YIG 3** line goes low.

d. When the top of the band (18.6 or 20 GHz) is reached, the sweep retraces and starts the cycle over again. During the **YIG SEL** line cycle, the **YIG 4** line stays HIGH. This line is not used in any of the sweep generator models covered by this manual.

The output of the Variable Gain/Inverter stage is applied, in parallel, to the WJ (Watkins-Johnson) and Avantek FM coil driver circuits.

To generate its output frequency, the sweep generator uses YIG oscillators manufactured by two companies: Watkins-Johnson and Avantek. To accommodate design differences, the A10 PCB has a separate FM coil-current drive circuit for each YIG type. As shown in the schematic (Figure 7-70), these two drive circuits are similar in design; their main differences lie in circuit-component

7-13.1 cont.

values. Since the two YIG current drivers are similar, only the Avantek circuit will be described.

The output from the Variable Gain/Inverter stage is applied to the Avantek circuit Voltage Amplifier (U9). The output of this amplifier drives the Current Amplifier circuit (Q3, Q4). The output of the Q3/Q4 circuit supplies current to all of the series connected Avantek YIG oscillator FM coils. This coil current returns to ground via the Current Sense resistor on the A10 PCB. The Current Sense resistor (actually four resistors, R51-R54) is effectively in series with the FM coils. The voltage drop across the Current Sense resistor is proportional to the current through the FM coils.

To reiterate, all three YIG oscillators receive their drive and FM coil currents in series. Only one oscillator band at a time, however, has its output switched to the Sweep generator RF output circuit. This RF output switching is a function of the PIN switch, described in paragraph 7-14.

In addition to supplying the input for the FM coil-current driver circuits, the Variable Gain/Inverter stage also supplies the input for the Tracking Filter current-driver circuit. The operation of this circuit is similar to the described for the Avantek FM coil-driver circuit above.

Presently, a tracking filter is used only with the 2-8 GHz YIG oscillator (Oscillator Band 1). This filter is a high-Q YIG band-pass filter that is contained in the same module as the YIG oscillator. This filter YIG is placed in series with the oscillator YIG and tracks at the same frequency; thereby attenuating harmonics and spurious signals.

The fourth current driver circuit on this PCB is the High Current Drivers (U12, U13, U14, U15) that is used for the Option 2, 70 dB or 110 dB Step Attenuator. This circuit provides the operating currents for the attenuator circuits. The step attenuator high current drivers are in place on this PCB even if the optional attenuator is not installed in the sweep generator.

The remaining circuit on the A10 PCB is the End of Band Pulse Generator (U1A -U1D, U2). This circuit generates a low-true pulse whenever a bandswitch point is reached. The inputs to this circuit are the **L HET YIG SEL** line, and the low-true **YIG 1, 2, 3,** and **4** FM coil select lines previously described. The **L HET YIG SEL** line is low only when the sweep generator is in the 10 MHz to 2 GHz heterodyne band (Models 6647 and 6648). (When in the heterodyne band, the **YIG 1** line is also LOW.) When a full-band sweep is used, the following sequence takes place:

e. When the sweep reaches 2 GHz, the **L HET** line goes HIGH (the **YIG 1** line stays LOW) and generates the **L EOB** pulse.

f. When 8 GHz is reached, the **YIG 1** line goes HIGH and the **YIG 2** line goes LOW and generates the **L EOB** pulse.

g. When 12.4 GHz is reached, the **YIG 2** line goes HIGH and the **YIG 3** line goes LOW. The **L EOB** pulse is generated when the **YIG 2 line** goes HIGH.

h. When the top of the band (18.6 or 20 GHz) is reached, the above cycle repeats.

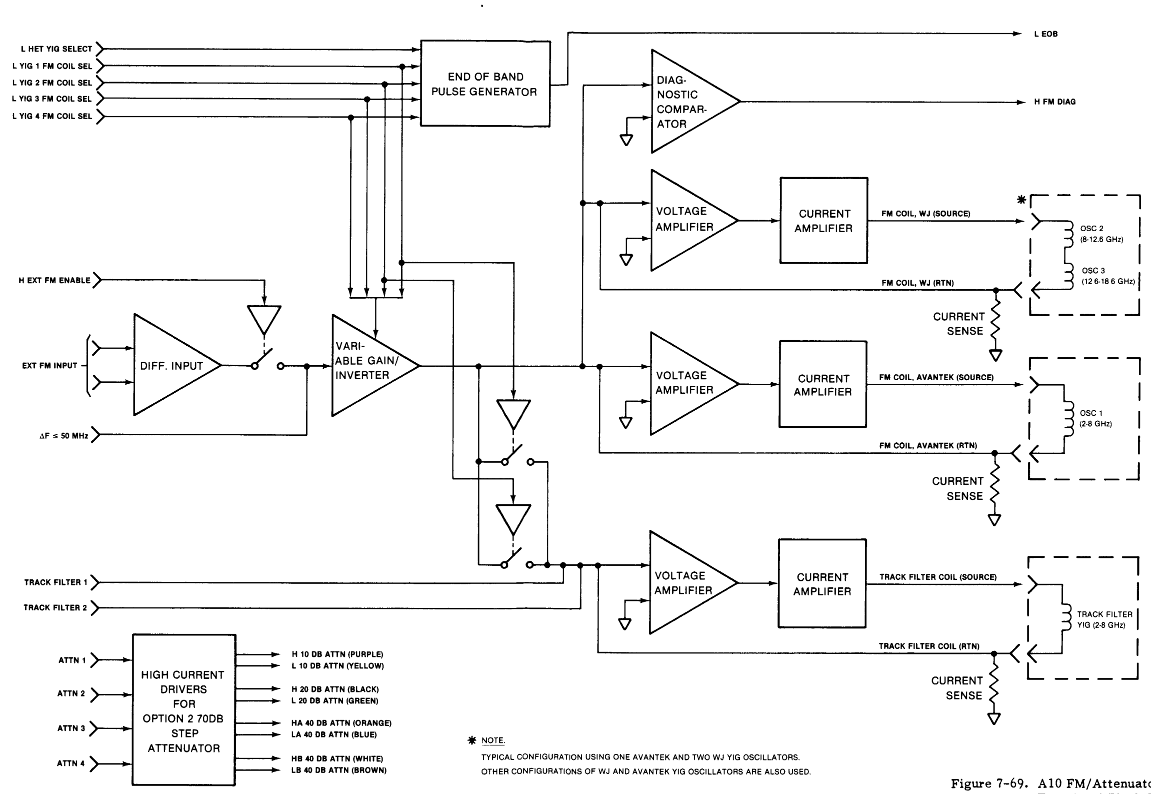


Figure 7-69. A10 FM/Attenuator PCB Functional Block Diagram

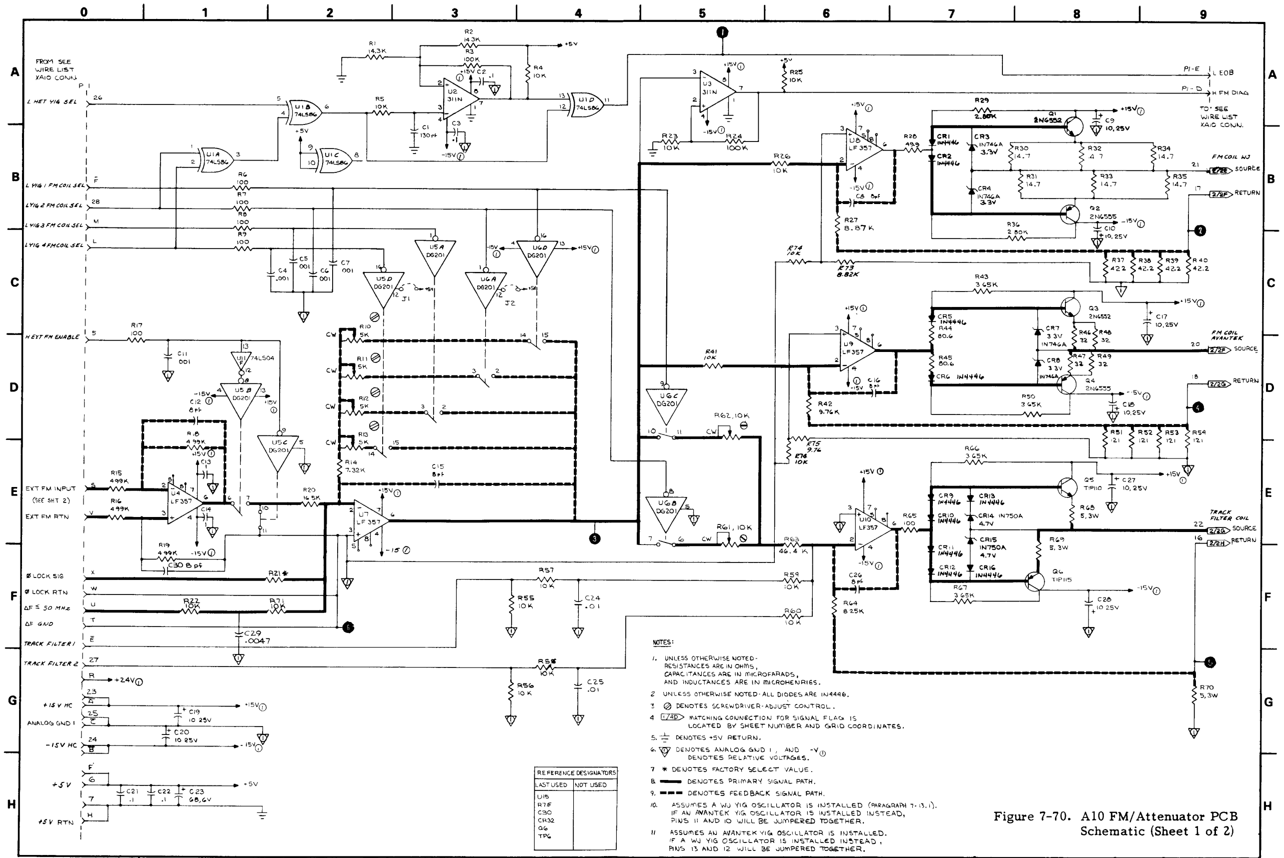
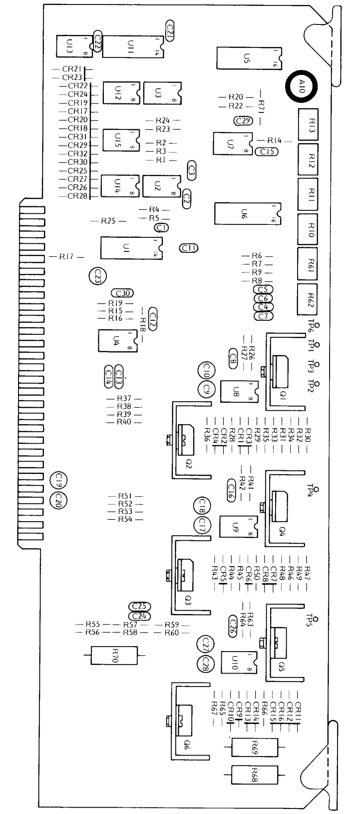


Figure 7-70. A10 FM/Attenuator PCB Schematic (Sheet 1 of 2)



A10 PCB Parts Locator Diagram

Figure 7-70. (Sheet 1)

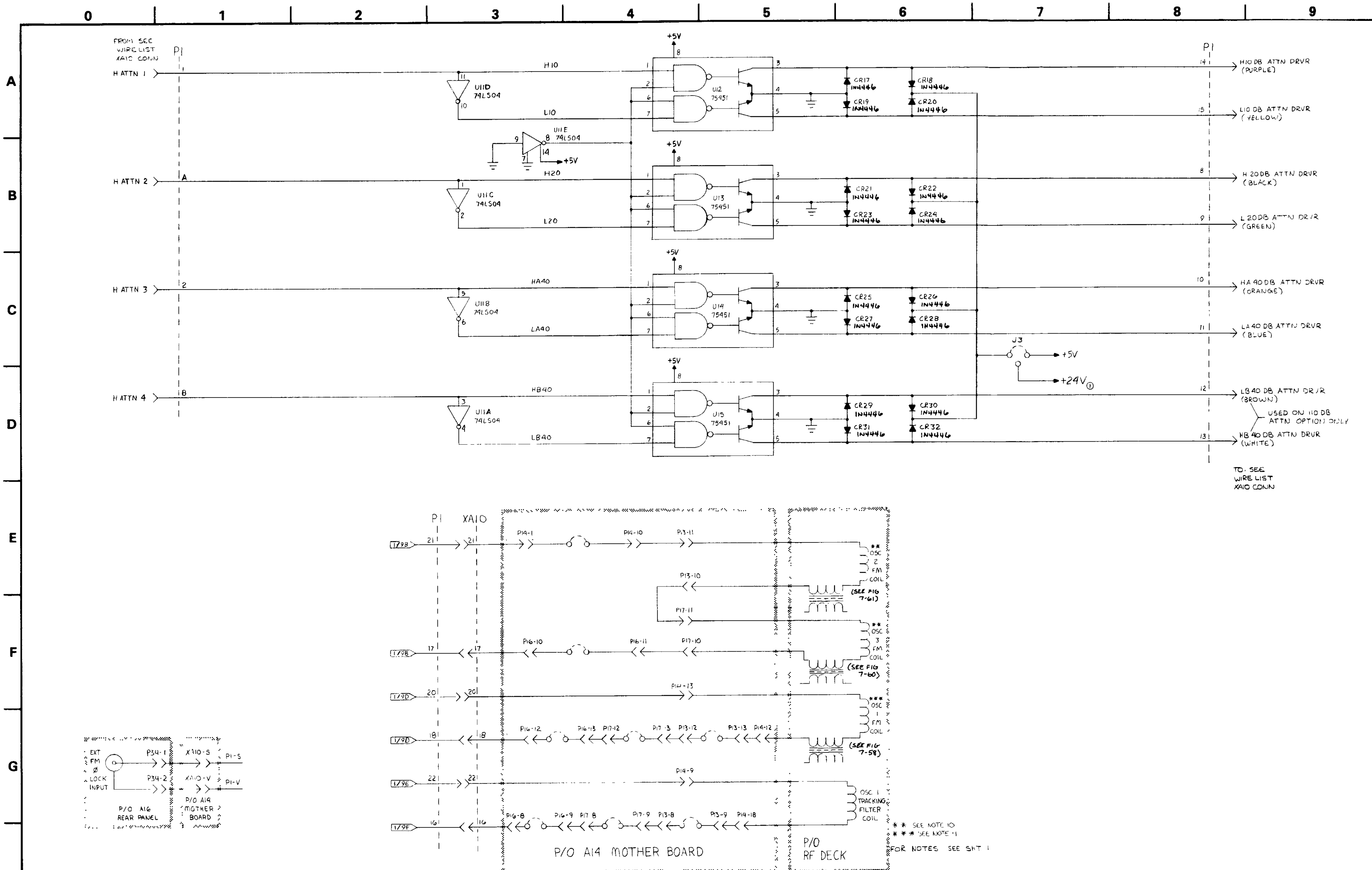
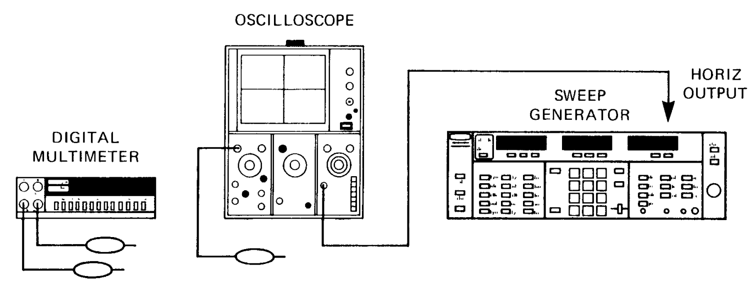


Figure 7-70. A10 FM/Attenuator PCB Schematic (Sheet 2 of 2)

7-13.2 A10 FM/Attenuator PCB Troubleshooting Information and Data

Error Code 23 reports the status of the A10 FM/Attenuator PCB. The microprocessor routine associated with this error code tests the A10 PCB by simulating a ≤50 MHz sweep and then verifying that the **H FM DIAG** bit has toggled from LOW to HIGH.

A test equipment setup for troubleshooting Error Code 23 is provided in Figure 7-71, a troubleshooting flowchart is provided in Figure 7-72, and a troubleshooting block diagram is provided in Figure 7-73.



SWEEP GENERATOR CONTROL SETTINGS

FREQUENCY RANGE: ΔF F0
RF SLOPE: Off
FM AND PHASELOCK: Off
LEVEL: 0 dBm
TRIGGER: AUTO
SWEEP TIME: 10 ms
MARKERS: A11 Off
F0: 1 GHz
LEVELING: INTERNAL
ΔF: 50 MHz
RETRACE RF: Off
RF ON: On

Figure 7-71. Test Equipment Setup for Troubleshooting Error Code 23

GENERAL INFORMATION

1. Before starting flowchart, check dc voltages at connector P1, as follows:

   a. +5V, pin F

   b. +15V, pin $\bar{A}$

   c. -15V, pin $\bar{B}$

2. Logic levels are TTL.

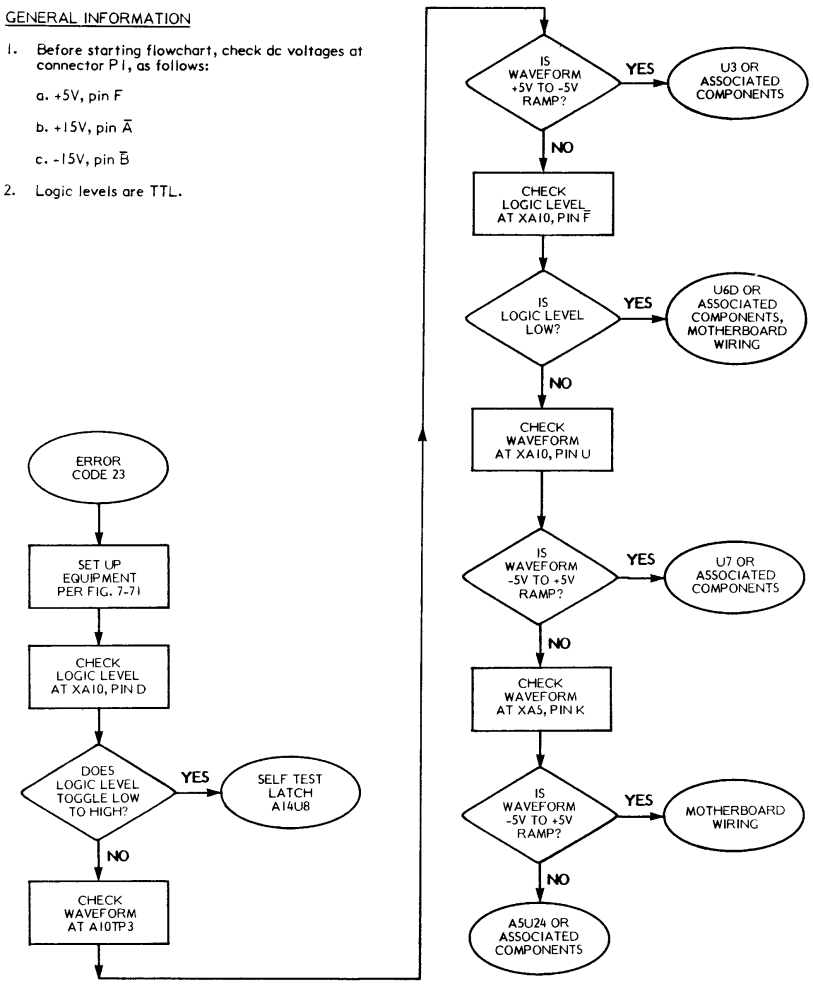


Figure 7-72. Error Code 23 Troubleshooting Flowchart

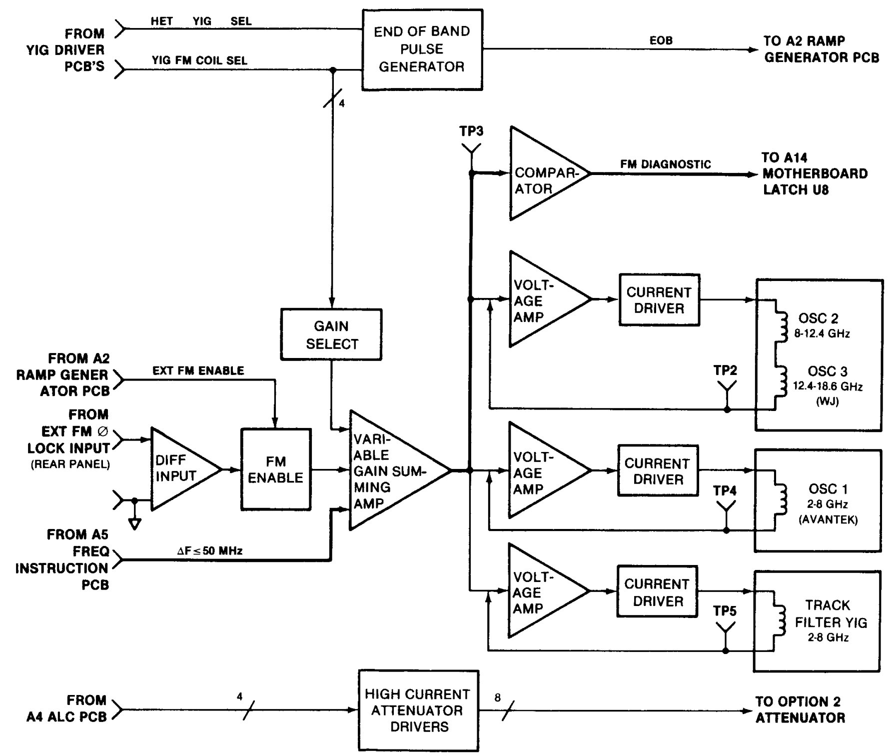


Figure 7-73. Error Code 23 Troubleshooting Block Diagram

Figure 7-72.

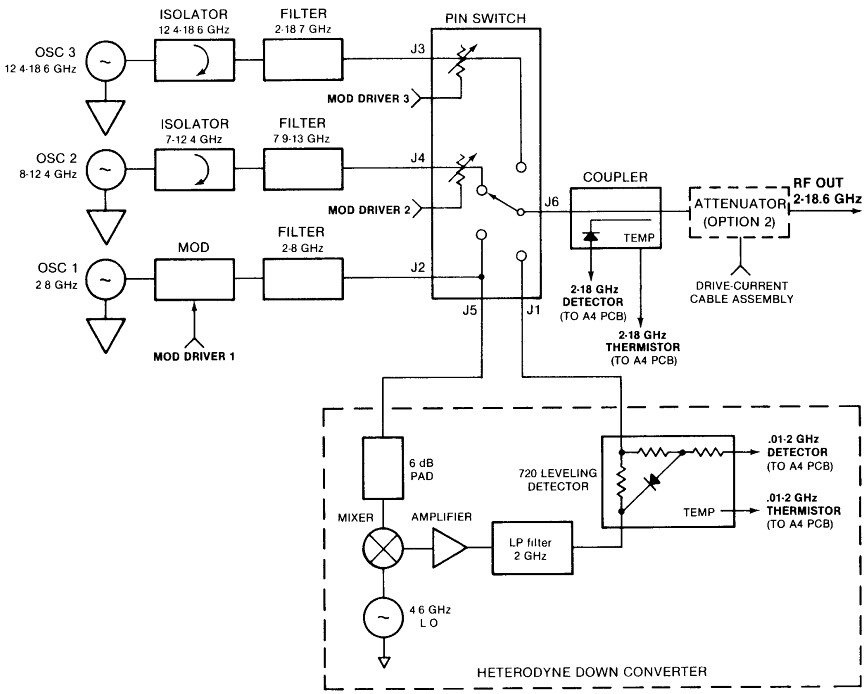


Figure 7-74. Model 6647 RF Components

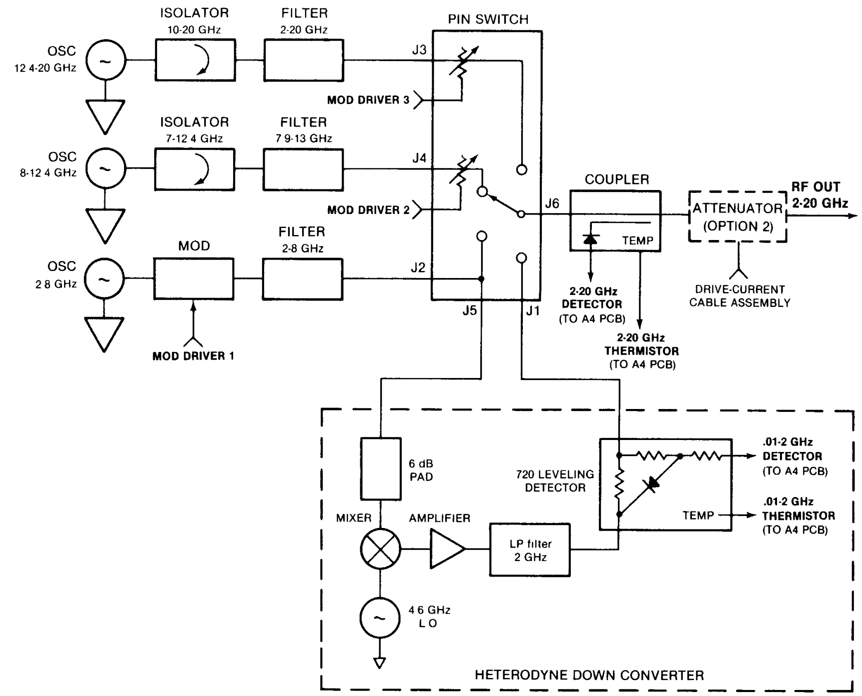


Figure 7-75. Model 6648 RF Components

Figure 7-74.

7-14 RF COMPONENTS, CIRCUIT DESCRIPTION

The RF components are used to generate sweep- and CW-frequency RF signals, and to route such signals to the front and rear (Option 10) panel RF OUTPUT connectors. Block diagrams showing the RF component configurations of the 6647 and 6648 are provided in Figures 7-74 and 7-75 (facing page), respectively. The component configurations of the 6637 and 6638 are identical to the 6647 and 6648, except that the 6637 and 6638 do not have a Heterodyne Down Converter. The RF components are described below:

a. Oscillators. The three YIG-tuned oscillators (YIGs) are of two basic types – Gunn Diode and GaAs FET; they are supplied by two main vendors – Watkins-Johnson (WJ) and Avantek.

b. MOD (Modulator). The MOD unit is a current-controlled variable attenuator that provides amplitude modulation and power leveling for the Osc 1 output. The MOD also provides impedance matching and isolation for the Osc 1 YIG.

c. Isolators. The two Isolators prevent reflected RF energy from returning to the YIG and causing frequency pulling. They attenuate the forward-wave energy by ≈0.5 dB and the reverse-, or standing-wave, energy by ≥ 20 dB.

d. Filters. The three filters provide band-pass filtering for the RF frequencies, to reduce harmonics.

e. PIN Switch. The PIN Switch is a current-controlled variable attenuator that switches between the three YIGs so that only one at a time is coupled to the RF OUTPUT circuit. The switch also provides the means for amplitude modulating and power-leveling the 2-18.6 (or 20) GHz signals.

f. Heterodyne Down Converter (for 6647 and 6648): The Heterodyne Down Converter generates the .01 to 2 GHz sweep- and CW-frequency outputs. When a frequency between .01 and 2 GHz is selected from the front panel, the output of the Osc 1 YIG is modified to sweep between 4.61 and 6.6 GHz. Via the PIN Switch, this modified YIG output is mixed with the output from a 4.6 GHz local oscillator. The difference beat-frequency is amplified and used to provide the .01 to 2 GHz output. When the .01-2 GHz band is selected, a portion of the down converter's Mixer is detected by the Model 720 Leveling Detector and used for internal leveling.

g. Coupler. The Coupler couples and detects a portion of the 2 to 18.6 (or 20) GHz RF output for use in internal power leveling. The detected sample, along with a voltage representing the coupler's temperature, is routed to the A4 PCB.

h. Attenuator. The optional Attenuator provides up to 70 dB of attenuation for the RF output. The drive current for the attenuator is supplied by a cable from the A10 PCB.

i. Transformers (not shown on figure). Three tranformers are used to improve linearity for sweeps ≤50 MHz. A transformer is provided for each of the three YIG oscillators. One transformer winding is in series with the YIG's main tuning coil, and the other winding is in series with the YIG's FM tickler coil.

7-15 A13/A14 SWITCHING POWER SUPPLY AND A14 MOTHERBOARD PCB'S

7-15.1 A13/A14 Switching Power Supply Circuit Description

The A13/A14 Switching Power Supply is a half-bridge, quasi-square wave, high-efficiency +5V converter that also contains the ±15V LC (low current), ±15V HC (high current), +12V, +24V, and -39V regulated voltage, and the +18V, +12/-24V, and +28V unregulated voltage supplies. An overall block diagram of the switching power supply is shown in Figure 7-79. A parts locator diagram for the A13/A14 circuit is shown in Figure 7-80. And the A13/A14 schematics (4 sheets) are shown in Figure 7-81.

WARNING

Voltages hazardous to life are present throughout the Switching Power Supply. When performing any maintenance, use extreme care to avoid electrical shock.

As shown in Figure 7-79, the switching power supply circuits and components are dispersed over the following PCBs and assemblies:

a. A16 Rear Panel Assembly: Line Voltage Selector Module, Fan, Fan Transformer, and Power Switch;

b. A14 Motherboard PCB: Off-Line Rectifier, Over-Current Sense, Over-Voltage Sense, Out of Reg Sense, Line Sense, -39V and +24V Regulator circuits;

c. A13 Switching Power Supply PCB: Control Amplifier, Soft-Start Control, Shut-Down Timer, Pulse-Width Modulator, and Switching Transistors circuits; and

d. A0 Basic Frame Assembly: +/-15V Regulator integrated circuits and -39V Regulator pass transistor.

The ac line power entering the sweep generator is input to the Off-Line Rectifier circuit (A14CR12). This circuit is a full-wave voltage doubler (120V line) or a full-wave bridge rectifier (220V line). The circuit's voltage output for either input-line voltage is 330 Vdc (±165 Vdc). The circuit's output current is sensed by A14R16 and, if greater than 2 amperes, activates the optically-coupled Overcurrent Sense circuit (A14U1). When activated, A14U1 causes the Shut Down Timer circuit to turn off the switching transistor drive voltage. The ±165 Vdc output from the Off-Line Rectifier circuit is applied to the dc-isolated Switching Transistors on A13.

CAUTION

Use an isolation transformer between the sweep generator and the ac line whenever maintenance is being performed on the switching power supply. Because portions of this power supply are referenced to the peak-negative or -positive line voltage, an isolation transformer is necessary to protect test instruments.

The Switching Transistors (A13Q5, A13Q6) alternately switch between **+165 Vdc** and **-165 Vdc** at a 50 kHz rate. These transistors are driven by the Pulse-Width Modulator (PWM) circuit (A13U4, A13Q3, A13Q4). This circuit (Figure 7-76) is used to develop a train of pulses. The duty cycle of this pulse train varies between 25 and 40% (approximately), depending on the amplitude of control voltage Vc. This Vc-voltage amplitude is determined by either the Control Amplifier (A13U2), the Soft-Start Control circuit (A13Q1), or the Shut-Down Timer circuit (A13U3).

The input to the Control Amplifier is the **+5V SENSE** line from the motherboard. This line senses the voltage across the +5V load. The output of A13U2 forces the PWM to adjust the duty cycle to whatever is necessary to maintain +5V at the sense line.

The input to the Soft-Start Control circuit is +12V from the +12V Regulator (A13U1). At the instant the POWER switch is pressed, +12V is applied to A13Q1 and, via C6, to the Vc pin on A13U4. With the Vc pin at +12V, the duty cycle of the A13U4 output pulse-train is minimum, thus causing the output of the +5V supply to be minimum. As C6 charges, the voltage at the A13U4 Vc pin decreases, the duty cycle of the A13U4 output pulse train increases, and the +5V supply output voltage increases. When the Control Amplifier senses that 5 volts has been reached (≈20 ms), regulation occurs. If a malfunction were to occur, such as A13U2 failing, the Over-Voltage circuit (A14Q4) would trigger the Shut-Down Timer circuit at approximately 5.7 volts.

The input to the Shut-Down Timer circuit (A13U3) is a trigger pulse caused by the **OVER-VOLTAGE/CURRENT** line going LOW. When triggered, A13U3 generates a 1-second pulse (approximately) that causes the A13U4 Vc voltage to go to +12V and the A13U4 INH (inhibit) voltage to go LOW. When the INH voltage is LOW, A13U4 is turned off; this shuts down the Switching Transistors. After A13U3 times out, the INH input goes HIGH and the power supply soft-starts. However, if the condition causing the A13U3 trigger is still present, A13U3 generates another pulse and shuts the supply down again. This A13U3 pulsing operation continues until either the over-voltage/current condition is corrected or the POWER switch is pressed OFF.

The outputs from the PWM circuit are coupled across dc isolation transformers T1 and T2, and used to drive FETs Q5 and Q6. These FETs require a bias of ≥5V to be switched on. The outputs from Q5 and Q6 form a composite waveform (Figure 7-76). The peak-to-peak value of this waveform is directly proportional to the peak value of the 120 V line (or directly proportional to the peak-to-peak value of the 220V line). This waveform is coupled to the five secondaries of A13T3. The reduced voltages appearing in these secondaries are also proportional to line voltage. These voltages are rectified and passed through an inductor, which is used as an integrator. The value of the voltage that is output from the inductor can be controlled entirely by T_1 (Figure 7-77) (the duty cycle of the PWM).

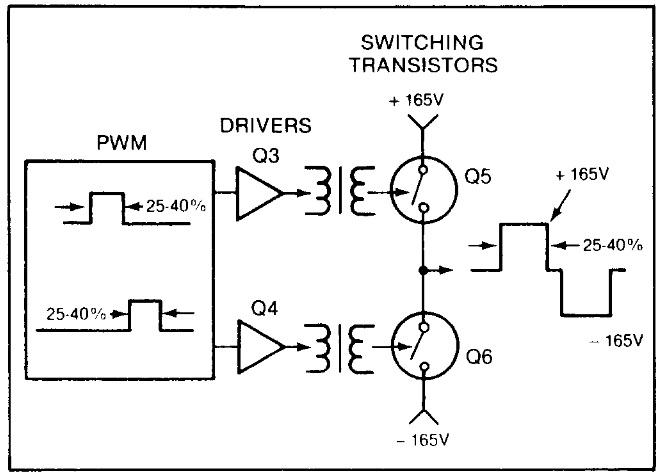


Figure 7-76. A13 Switching Transistors, Simplified Schematic

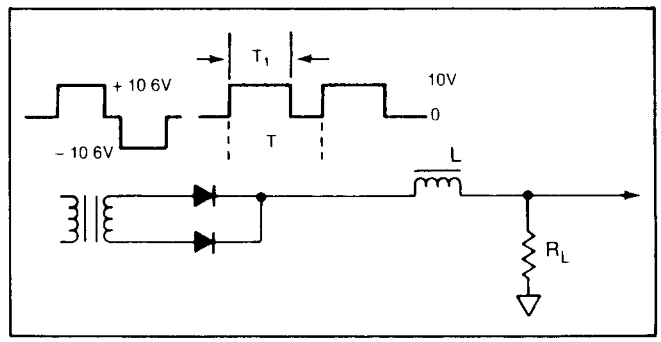


Figure 7-77. A13 Regulator, Simplified Schematic

As shown in Figure 7-79, the five rectifier circuits – excepting the +5V and the +12/-24V circuits – supply their respective outputs to voltage regulators. The -39V Regulator (A14Q1, A14Q2, A14Q3, and A0Q1) is driven by the -43V supply. The +24V Regulator (A14U2) is driven by the +28V supply. The -15V LC (low current) and HC (high current) Regulators (A0U1, A0U2 respectively) are driven by the -18V supply. And the +15V LC and HC Regulators (A0U3 and A0U4 respectively) are driven by the +18V supply. The unregulated +18V also goes to the YIG driver bias supply on the A6, A7, and A8 PCBs and to the +15V Rectifier circuit. Here, the +18V both reverse biases A14CR7/A14CR8 and provides the input for voltage regulator A13U1.

The remaining two circuits in Figure 7-79 are the Out of Reg Sense (U4A, U4B, U5C, U5D) and the Line Voltage Sense (U5A, U5B) circuits. The Out of Reg Sense circuit detects when any of the regulated supplies goes out of tolerance. If such a condition exists, the **L OR** diagnostic line goes TRUE and the A14 OUT OF REG indicator LED lights. The Line Voltage Sense circuit detects when the ac line exceeds the +5% or -10% limits required for circuit operation. This circuit also detects if the Line Voltage Selector Module printed circuit card is correctly positioned for the available line voltage. If either the line voltage is incorrect or the PC card is improperly positioned, the appropriate **L HL** or **L LL** diagnostic line will go TRUE, and the LED indicator will light.

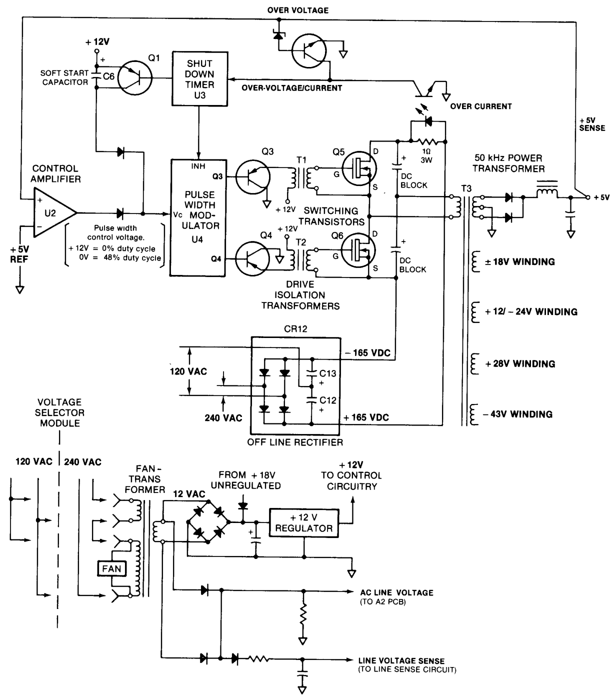


Figure 7-78. A13/A14 Switching Power Supply, Simplified Schematic

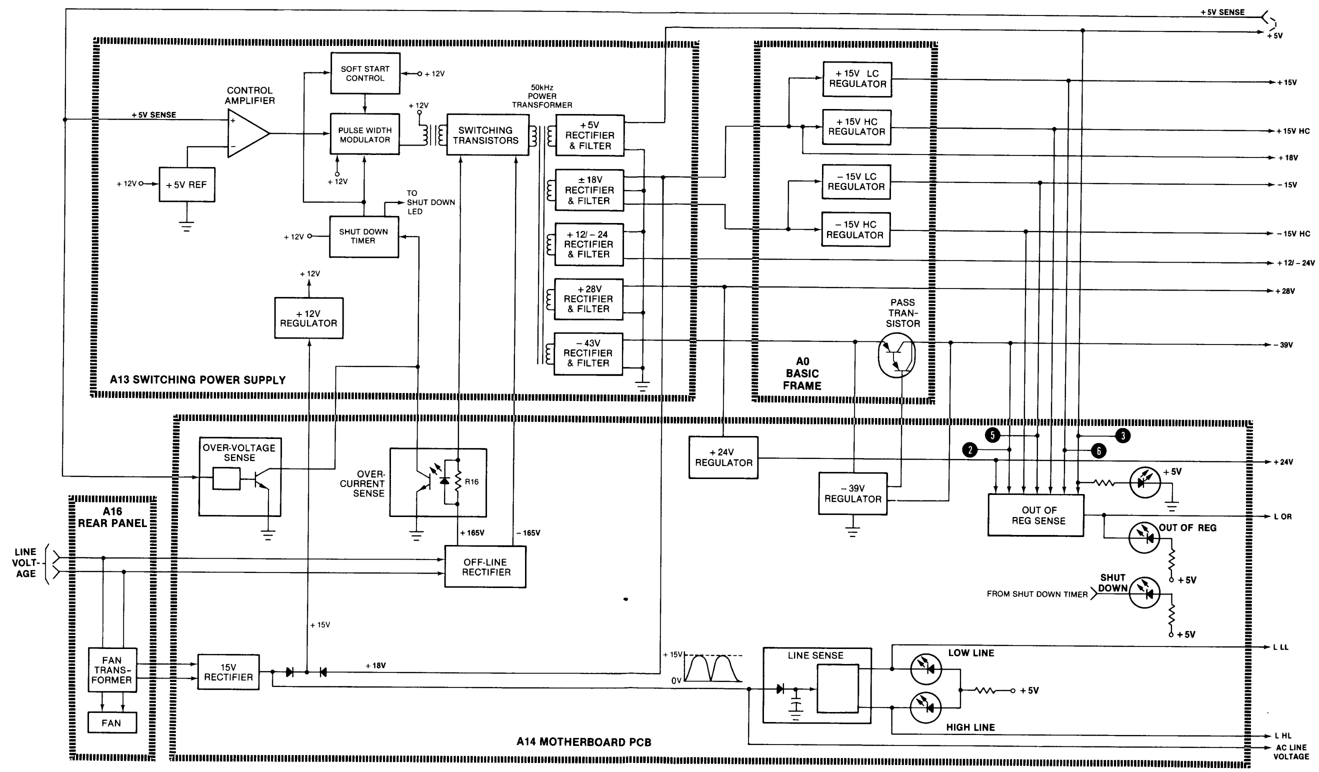
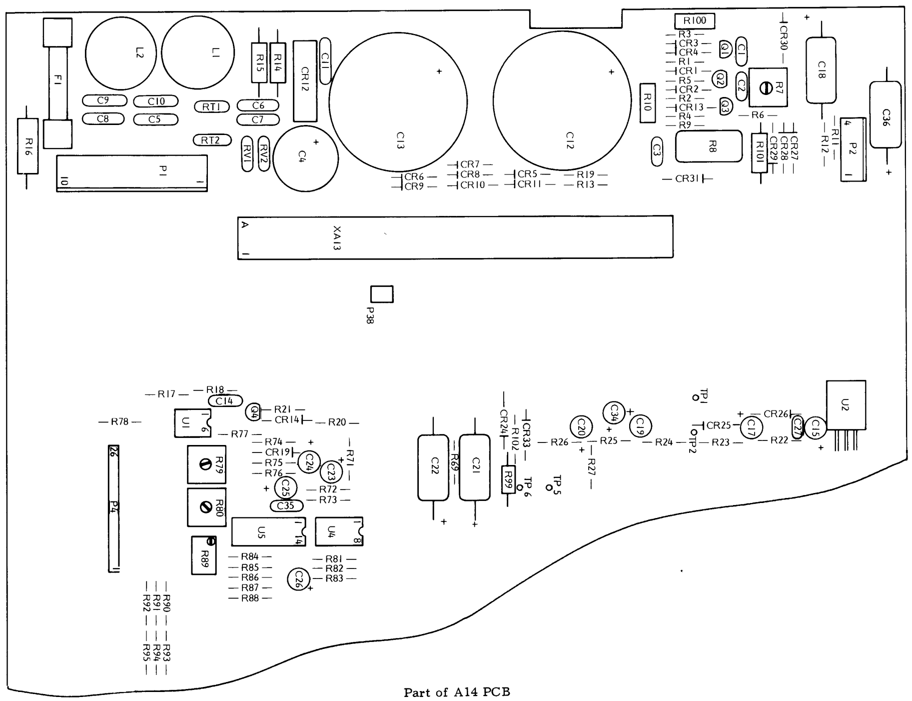
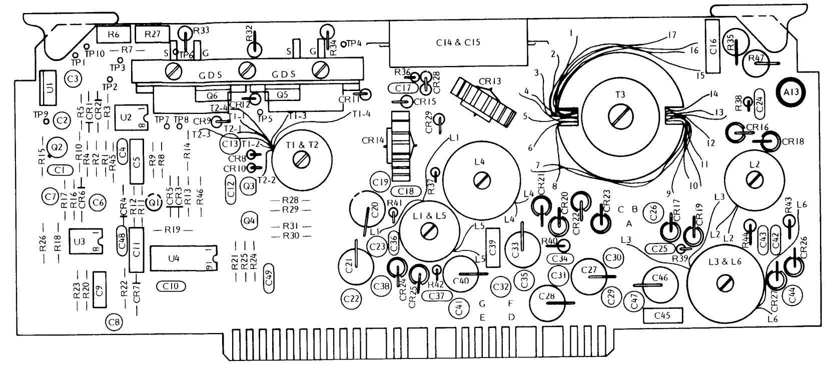


Figure 7-79. A13/A14 Switching Power Supply Overall Block Diagram

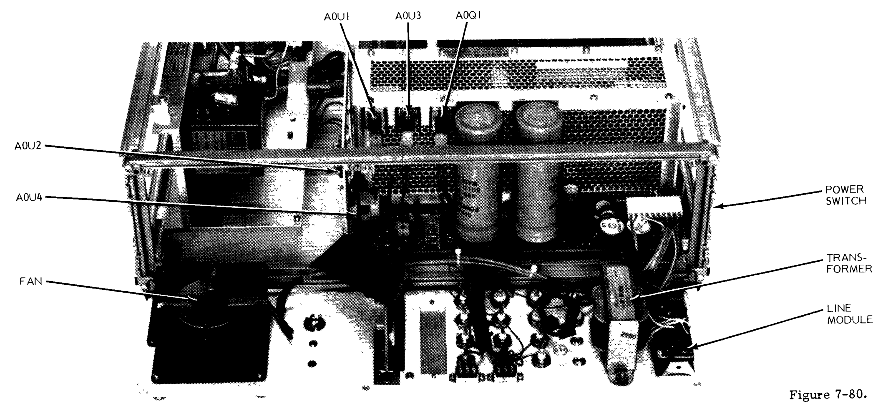
Figure 7-78.



Part of A14 PCB

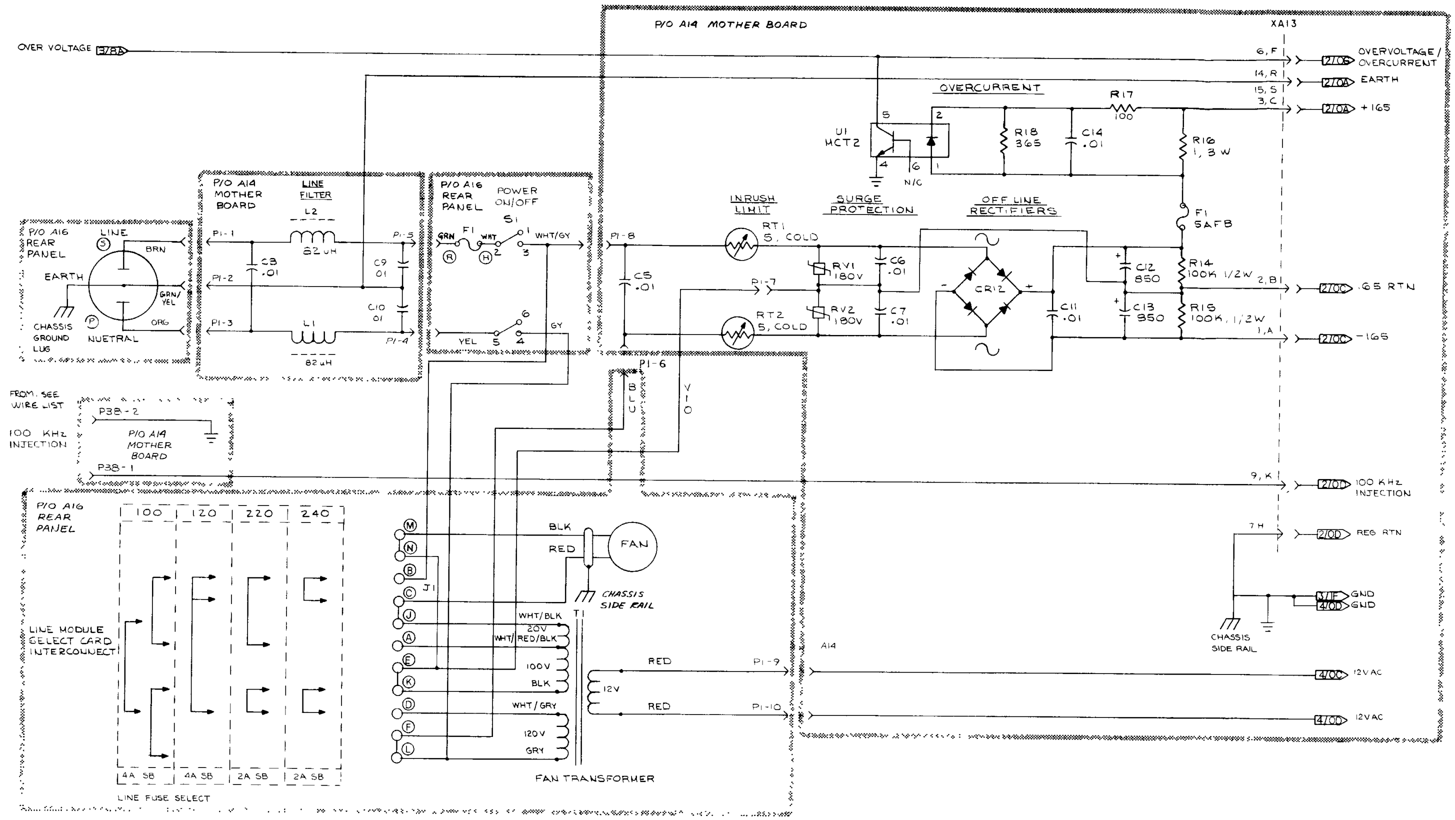


A13 PCB



A16 Rear Panel

Figure 7-80. A13/A14 Switching Power Supply, Parts Locator Diagram



NOTES

UNLESS OTHERWISE SPECIFIED, ALL CIRCUITRY SHOWN IS RESIDENT ON XA14

1. POLARITY SENSITIVE COMPONENTS. IF + 12V IS REQUIRED THESE COMPONENTS WILL BE LOADED IN THE REVERSE DIRECTION.
2. (A) DENOTES CONNECTIONS ON REAR PANEL LINE MODULE.
3. 3 DENOTES WIRE HOLE NUMBER FROM MOTHERBOARD XA14 TO VOLTAGE REGULATORS
4. 2/3C MATCHING CONNECTION FOR SIGNAL FLAG IS LOCATED BY SHEET NUMBER AND GRID COORDINATES.
5. DENOTES SCREWDRIVER ADJUST.
6. DENOTES GROUNDPLANE AREA
7. DENOTES TEST POINTS
8. REMOVE FOR TEST
9. DENOTES PRIMARY SIGNAL PATH.
10. DENOTES FEEDBACK SIGNAL PATH.
11. DENOTES ISOLATED GND. AND -V(1) DENOTES RELATIVE VOLTAGES

Figure 7-81. A13/A14 Switching Power Supply Schematic (Sheet 1 of 4)

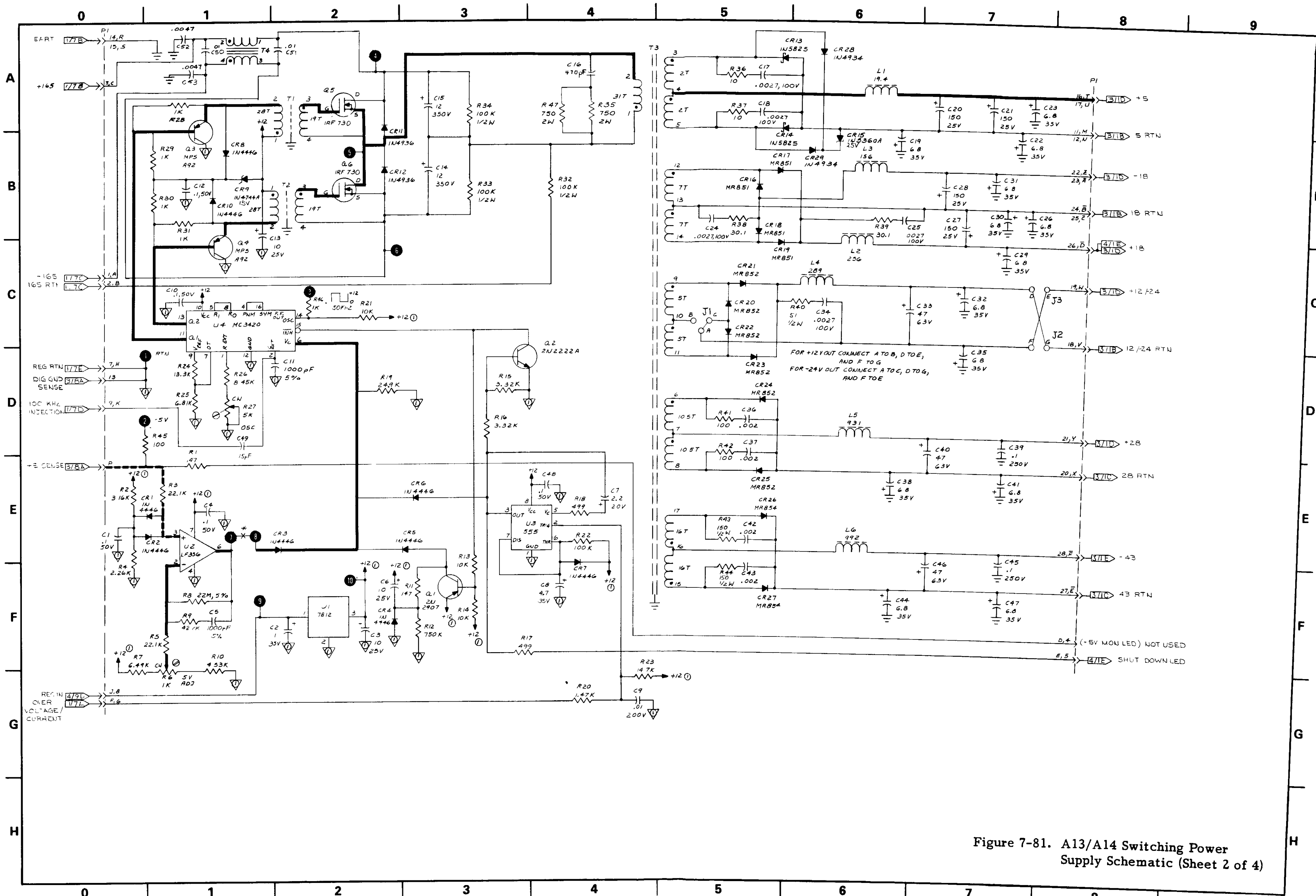


Figure 7-81. A13/A14 Switching Power Supply Schematic (Sheet 2 of 4)

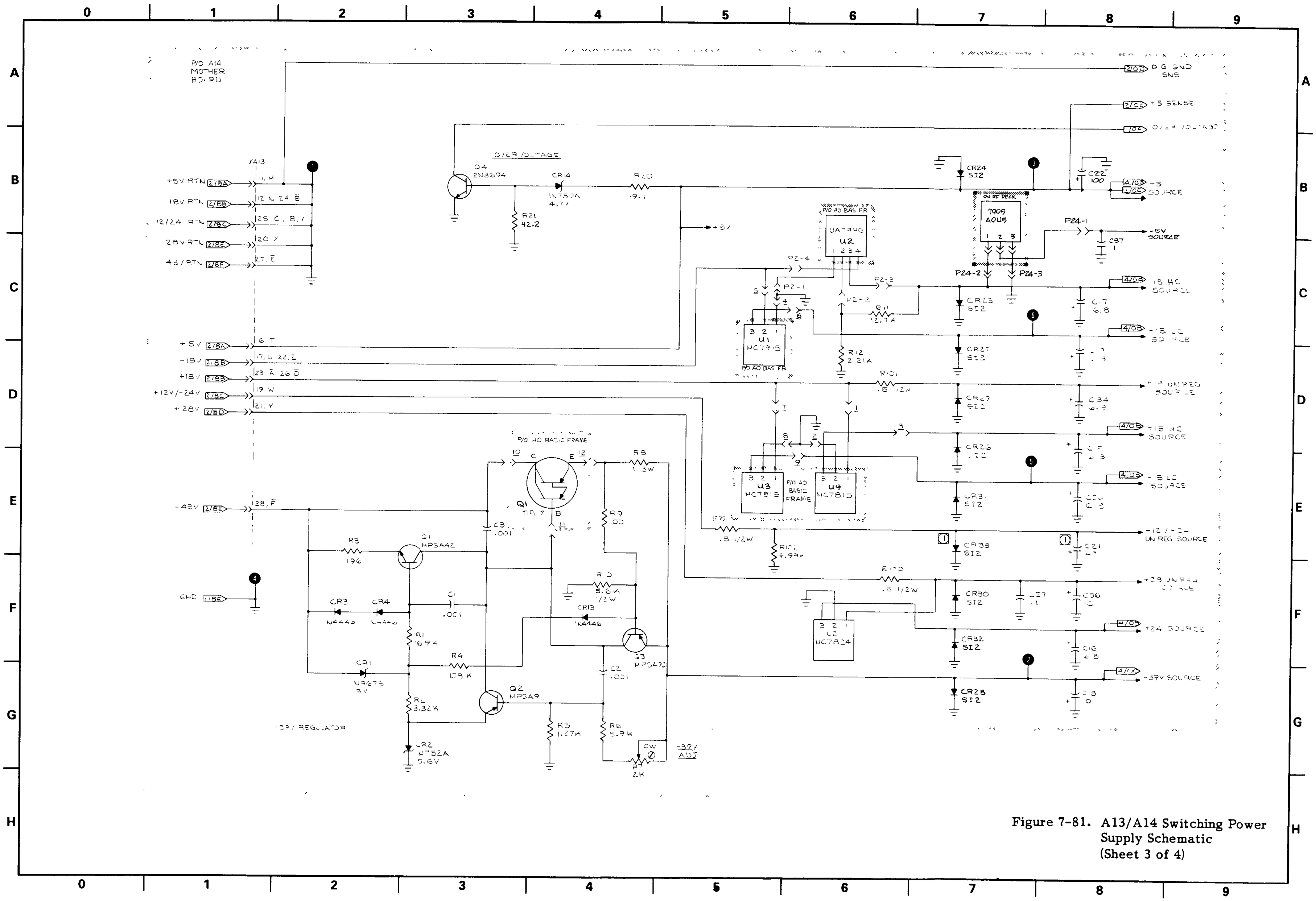


Figure 7-81. A13/A14 Switching Power Supply Schematic (Sheet 3 of 4)

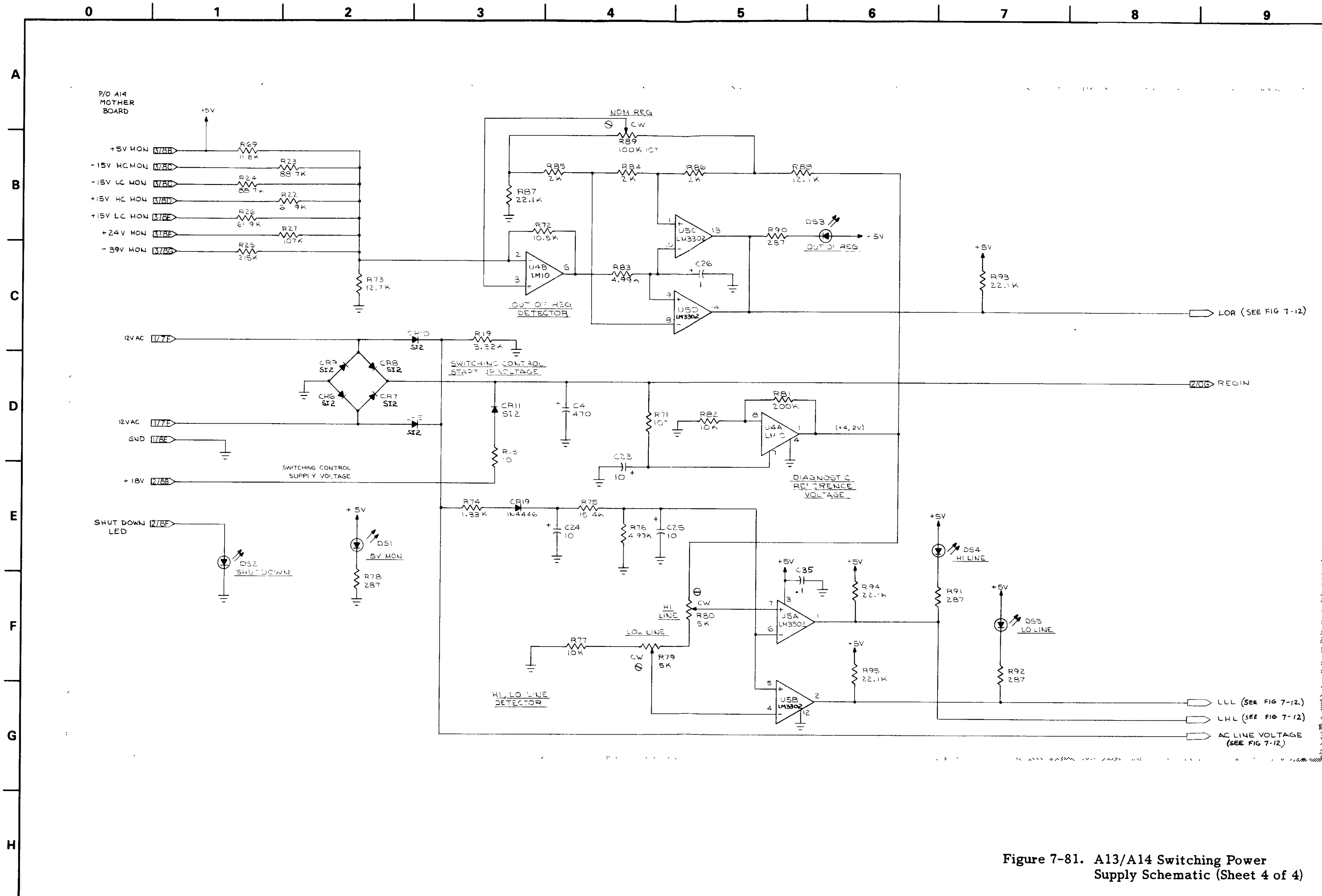


Figure 7-81. A13/A14 Switching Power Supply Schematic (Sheet 4 of 4)

7-15.2 A14 Motherboard PCB, Wire Lists and Service Data

The A14 Motherboard PCB provides the medium for connecting the A1-A10 and A13 PCBs with each other, with the A11 and A12 PCBs, with the RF Components Deck, and with the rear panel connectors and switches. The A14 PCB also contains three groups of circuits, as shown in Figure 7-82. These circuits are shown schematically with the PCB circuits to which they relate, as follows:

a. Group I - Power Supply. Shown in Figure 7-81.

b. Group II - Linearizer ROM and Diagnostic (Self Test) Latch. Shown in Figure 7-12.

c. Group III - YIG Oscillator, PIN Switching, and PIN Modulator Current Drive. Shown in Figures 7-58, 7-60, and 7-61.

This paragraph contains the following service data:

d A tabulation of the A14 PCB connectors that show destinations for each (Table 7-16).

e. A tabulation of the A14 PCB interconnections (wire lists) (Tables 7-17 thru 7-20)

f Diagrams that show YIG oscillator wiring (Figures 7-83, 7-84, and 7-85).

g. A parts locator diagram for the A14 components (Figure 7-86).

NOTE

Within the Group III area of A14 (Figure 7-81) there are two components clusters--Q17, Q18, and Q19; Q20, Q21, and Q22; and their associated resistors and diodes—that are not used in the 6637, 6638, 6647, or 6648. The Q17-Q19 components provide current drive for the Osc 4 switching elements in the PIN Switch. And the Q20-Q22 components provide current drive for a different model PIN Switch.

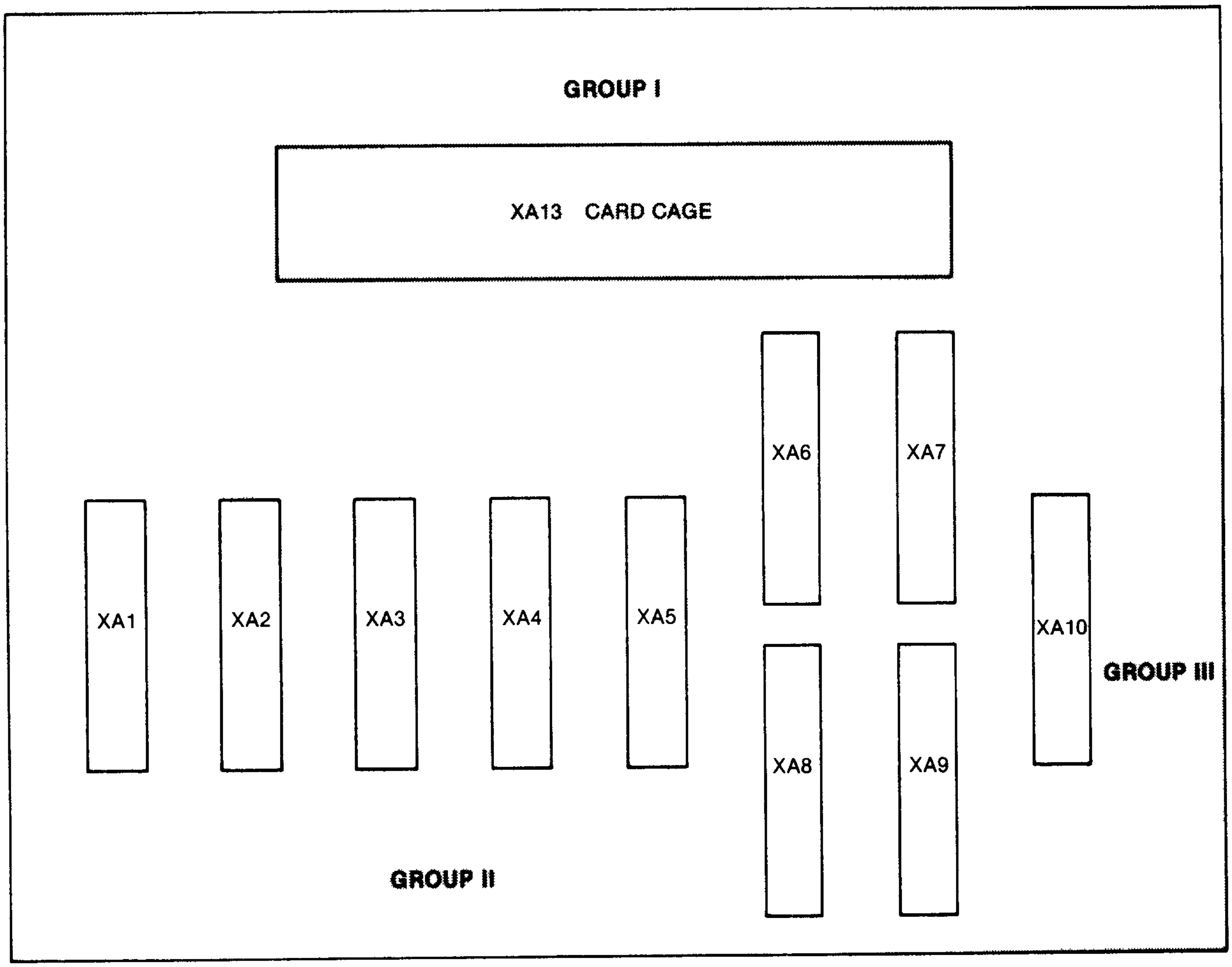


Figure 7-82. A14 Motherboard PCB, Circuit Groups

Table 7-16. A14 Connectors, Destinations

CONN. NO.	NO. OF PINS	DESTINATION
P1	10	Rear Panel - Line Voltage Selector Module
P2	4	-15V HC Regulator, A0U2
P3	26	No mate - Monitors bus for test purposes
P4	26	A18 GPIB Connector PCB
P5	26	Microprocessor - A12J5
P6	26	Microprocessor - A12J6
P7	26	Microprocessor - A12J7
P8	3	Not used
P10	4	Rear Panel - EXT AM INPUT and EXT SQ WAVE INPUT Connectors
P11	4	Not used
P12	5	Heterodyne Down Converter
P13	16	Osc 2 YIG
P14	16	Osc 1 YIG
P15	9	PIN Switch
P16	16	Osc 4 YIG (not used)
P17	16	Osc 3 YIG
P18	3	Transistor A6Q1
P19	3	Transistor A6Q2
P20	3	Transistor A6Q3
P21	3	Transistor A7Q1
P22	3	Transistor A7Q2
P23	3	Transistor A7Q3
P24	3	P13, P14, & A14C16
P25	3	Transistor A9Q1 (not used)
P26	3	Transistor A9Q2 (not used)
P27	3	Transistor A9Q3 (not used)
P28	3	Transistor A8Q1
P29	3	Transistor A8Q2
P30	3	Transistor A8Q3
P31	8	Step Attenuator (Option 2)
P33	2	Not used
P34	2	Rear Panel - EXT FM Ø LOCK INPUT Connector
P35	3	Heterodyne Down Converter Level Detector
P36	3	Coupler Level Detector
P37	2	Front Panel - EXTERNAL INPUT Connector
P38	2	Not used
XA1	56	A1 GPIB Interface PCB
XA2	56	A2 Ramp Generator PCB
XA3	56	A3 Marker Generator PCB
XA4	56	A4 Automatic Level Control PCB
XA5	56	A5 Frequency Instruction PCB
XA6	56	A6 HET/YIG Driver PCB
XA7	56	A7 YIG Driver PCB
XA8	56	A8 YIG Driver PCB
XA9	56	Not used
XA10	56	A10 FM/Attenuator PCB
XA13	56	A13 Switching Power Supply PCB
XA16	16	Rear Panel Connectors: • EXT SWEEP • SWEEP DWELL INPUT • SWEEP TRIGGER INPUT • BANDSWITCH BLANKING Switch • HORIZ OUTPUT DURING CW Switch • SEQ SYNC OUTPUT • MARKER OUTPUT • RETRACE BLANKING (+) • RETRACE BLANKING (-) • HORIZ OUTPUT • 1V/GHz • PENLIFT OUTPUT • BANDSWITCH BLANKING

Table 7-17. Motherboard Wire List, Signal Mnemonic Order – PCB Revision: E

SIGNAL MNEMONIC*	SIGNAL NAME	SOURCE CONNECTOR & PIN NUMBER OR A14 PCB COMPONENT	DESTINATION CONNECTOR & PIN NUMBER OR A14 PCB COMPONENT
L ACTIVATE RELAY	PENLIFT OUTPUT Relay (Rear Panel Connector)	XA2-H	K1
AC LINE VOLTAGE	Line Voltage Sample	CR10-Cathode	XA2-A
ADRS SW - S1	GPIB Address Switch - S1 (1)	P4-3	XA1-M
ADRS SW - S2	GPIB Address Switch - S2 (2)	P4-2	XA1-N
ADRS SW - S4	GPIB Address Switch - S4 (8)	P4-14	XA1-13
ADRS SW - S3	GPIB Address Switch - S3 (4)	P4-1	XA1-P
ADRS SW - S5	GPIB Address Switch - S5	P4-15	XA1-12
$\overline{\text{ATN}}$	Attention - GPIB	P4-12	XA1-B
H ATTN 1	Attenuator 1	XA4-24	XA10-1
H ATTN 2	Attenuator 2	XA4-$\overline{\text{B}}$	XA10-A
H ATTN 3	Attenuator 3	XA4-$\underline{23}$	XA10-2
H ATTN 4	Attenuator 4	XA4-$\overline{\text{A}}$	XA10-B
A6Q1-B	A6Q1 - Base	XA8-S	A14P18-3
A6Q1-C	A6Q1 - Collector	XA6-R	P18-2
A6Q1-E	A6Q1 - Emitter	XA6-P	P18-1
A7Q1-B	A7Q1 - Base	XA7-S	P21-3
A7Q1-C	A7Q1 - Collector	XA7-R	P21-2
A7Q1-E	A7Q1 - Emitter	XA7-P	P21-1
A8Q1-B	A8Q1 - Base	XA8-S	P28-3
A8Q1-C	A8Q1 - Collector	XA8-R	P28-2
A8Q1-E	A8Q1 - Emitter	XA8-P	P28-1
A9Q1-B	A9Q1 - Base	XA9-S	P25-3
A9Q1-C	A9Q1 - Collector	XA9-R	P25-2
A9Q1-E	A9Q1 - Emitter	XA9-P	P25-1
BANDSWITCH BLANKING +	BANDSWITCH BLANKING + (Rear Panel Connector)	XA2-2	XA16-5
BANDSWITCH BLANKING -	BANDSWITCH BLANKING - (Rear Panel Connector)	XA2-3	XA16-12
CR/CR-LF	Carriage Return/ Carriage Return-Line Feed	P4-16	XA1-11
CW FILTER	CW Filter	XA5-T	XA6-13, XA7-13, XA8-13, XA9-13
$\overline{\text{DAV}}$	Data Not Valid - GPIB	P4-11	XA1-C
$\overline{\text{DIO 1}}$	Data Bus 1 - GPIB	P4-6	XA1-J
$\overline{\text{DIO 2}}$	Data Bus 2 - GPIB	P4-7	XA1-H
$\overline{\text{DIO 3}}$	Data Bus 3 - GPIB	P4-8	XA1-F
$\overline{\text{DIO 4}}$	Data Bus 4 - GPIB	P4-5	XA1-K
$\overline{\text{DIO 5}}$	Data Bus 5 - GPIB	P4-18	XA1-9
$\overline{\text{DIO 6}}$	Data Bus 6 - GPIB	P4-21	XA1-6
$\overline{\text{DIO 7}}$	Data Bus 7 - GPIB	P4-20	XA1-7
$\overline{\text{DIO 8}}$	Data Bus 8 - GPIB	P4-19	XA1-8
L DOP	Data Out Port	XA1-22	P6-2
L DOS	Data Out Status	XA1-21	P6-1
H DWELL	Dwell	XA2-21	U8-3
L DWELL (LD)	Dwell (LD)	XA1-6	XA2-17
L DWELL DETECTED	Dwell Detected	XA2-15	U10-14
H EXT FM ENABLE	External FM Enable	XA2-Y	XA10-5
L EGD	External Gain LED Driver	XA4-17	P5-24
L EOB	End of Band	XA10-E	XA2-Z
$\overline{\text{EOI}}$	End or Identify - GPIB	P4-9	XA1-E
EXT ALC GAIN (CW)	External ALC Gain (clockwise end)	EXT ALC GAIN POT.	XA4-F, via A14P39-1
EXT ALC GAIN (CCW)	External ALC Gain (counterclockwise end)	EXT ALC GAIN POT.	XA4-J, via A14P39-3

* L = Low-Active State, H = High Active State

Table 7-17. Motherboard Wire List, Signal Mnemonic Order (Continued) – PCB Revision: E

	SIGNAL MNEMONIC*	SIGNAL NAME	SOURCE CONNECTOR & PIN NUMBER OR A14 PCB COMPONENT	DESTINATION CONNECTOR & PIN NUMBER OR A14 PCB COMPONENT
	EXT ALC GAIN (S)	External ALC Gain (slider arm)	EXT ALC GAIN POT.	XA4-H, via A14P39-2
	EXT AM INPUT	EXT AM Input (rear panel connector)	P10-2	XA4-16
	EXT DET IN	EXTERNAL DETECTOR (OR POWER METER) INPUT (Front Panel Connector)	P37-2	XA4-D
	EXT DET RTN	EXTERNAL Detector Input Return	P37-1	XA4-4
L	EXT DWELL	Sweep Dwell Input (rear panel connector)	XA16-3	XA2-D
	EXT FM INPUT	EXT FM Ø LOCK INPUT (Rear Panel Connector)	P34-1	XA10-S
	EXT FM RTN	EXT FM ØLOCK INPUT Return	P34-2	XA10-V
	EXT RAMP IN	EXT SWEEP (Rear Panel Connector)	XA16-1	XA2-B
	EXT SQ WAVE IN	EXT SQUARE - WAVE INPUT (Rear Panel Connector)	P10-4	XA4-15
L	EXT TRIG PULSE IN	SWEEP TRIGGER INPUT (Rear Panel Connector)	XA16-4	XA2-E
	FCEN	F Center DAC Output	XA5-$\overline{A}$	XA6-19, XA7-19 XA8-19, XA9-19
	FCEN/VPF	F Center/Voltage Proportional to Frequency	XA5-W	XA4-T, XA6-16 XA7-16, XA8-16, P7-206, XA9-16
	FCEN SIG GND	F Center Signal Ground	XA5-Z	XA6-18, XA7-18 XA8-18, XA9-18
	F CORR	F Correction, Analog Signal	XA5-U	XA6-14, XA7-14 XA8-14, XA9-14
	FC BØ (LSB)	F Correction Bus BØ (LSB)	XA6-$\overline{A}$, XA7-$\overline{A}$, XA8-$\overline{A}$ or XA9-$\overline{A}$	XA5-C
	FC B1	F Correction Bus B1	XA6-$\overline{B}$, XA7-$\overline{B}$, XA8-$\overline{B}$ or XA9-$\overline{B}$	XA5-D
	FC B2	F Correction Bus B2	XA6-Y, X7-Y, XA8-Y or XA9-Y	XA5-A
	FC B3	F Correction Bus B3	XA6-Z, XA7-Z, XA8-Z or XA9-Z	XA5-B
	FC B4	F Correction Bus B4	XA6-$\overline{C}$, XA7-$\overline{C}$, XA8-$\overline{C}$ or XA8-$\overline{C}$	XA5-E
	FC B5	F Correction Bus B5	XA6-$\overline{D}$, XA7-$\overline{D}$, XA8-$\overline{D}$ or XA9-$\overline{D}$	XA5-F
	FC B6	F Correction Bus B6	XA6-$\overline{E}$, XA7-$\overline{E}$, XA8-$\overline{E}$ or XA9-$\overline{E}$	XA5-H
	FC B7 (MSB)	F Correction Bus B7 (MSB)	XA6-$\overline{F}$, XA7-$\overline{F}$, XA8-$\overline{F}$ or XA9-$\overline{F}$	XA5-J
	FM COIL, AVANTEK (SOURCE)	FM Coil, Avantek, (+)	XA10-20	P14-13
	FM COIL AVANTEK (RTN)	FM Coil, Avantek, (-)	P16-12	XA10-18
	FM COIL, WJ (SOURCE)	FM Coil, WJ (+)	XA10-21	P14-11
	FM COIL, WJ (RTN)	FM Coil, WJ (-)	P16-10	XA10-17
H	FM DIAG	FM Diagnostic	XA10-D	U8-17
L	FØ IDENTIFY	FØ Identify	P5-18	XA3-22
	GPIB IN	GPIB In	XA1-Z	U10-18
L	HET PIN SEL	Hetrodyne Band Pin Switch Select	XA6-2	XA7-2, CR17-Cathode

* L = Low-Active State, H = High Active State

Table 7-17. Motherboard Wire List, Signal Mnemonic Order (Continued) – PCB Revision: E

	SIGNAL MNEMONIC*	SIGNAL NAME	SOURCE CONNECTOR & PIN NUMBER OR A14 PCB COMPONENT	DESTINATION CONNECTOR & PIN NUMBER OR A14 PCB COMPONENT
L	HET YIG SEL	Hetrodyne Band YIG Select	XA6-H	XA7-H, XA10-26
	HORIZONTAL OUTPUT	HORIZ OUTPUT (Rear Panel Connector)	XA3-J	XA16-10
	HORIZ OUTPUT DURING CW	HORIZ OUTPUT DURING CW +, -Switch (Rear Panel)	XA16-6	U10-17
	$\overline{IFC}$	Interface Clear - GPIB	P4-25	XA1-2
H	INTENSITY MARKER	Intensity Marker	XA3-20	XA2-X, XA2-20 & X
L	KPS	Keycode Port Status	XA1-23	P6-3
L	KSV (SX3)	Keycode-Set Valid	P6-5	XA1-$\overline{B}$
L	LEVEL DIP	Dip the RF Level Signal	XA2-W	XA4-W
L	LISTEN	LISTEN LED (Front Panel)	XA1-16	P6-18
L	LOCAL LOCKOUT	LOCAL LOCKOUT LED (Front Panel)	XA1-19	P6-15
L	M1 IDENTIFY	M1 Identify	P5-5	XA3-21
L	M2 IDENTIFY	M2 Identify	P5-17	XA3-X
	MAN SWEEP INPUT	Manual Sweep Input	P7-5	XA5-17
	MARKER AMPL (CW)	Marker Amplitude Control (Clockwise end)	P7-22	XA3-Z
	MARKER AMPL (CCW)	Marker Amplitude Control (Counterclockwise end)	P7-24	XA5-K
	MARKER AMPL (S)	Marker Amplitude Control (Slider Arm)	P7-23	XA3-Y
	µP LSB (BØ)	Microprocessor Data Bus BØ (LSB)	P6-9	P3-9, U6-3, U7-3, U8-3, U10-3, and XA1-$\underline{F}$, XA2-$\underline{F}$, XA3-$\underline{F}$, XA4-F, XA5-$\underline{F}$
	µP B1	Microprocessor Data Bus B1	P6-22	P3-22, U6-4, U7-4, U8-4, U10-4, and XA1-28, XA2-28, XA3-28, XA4-28, XA5-28
	µP B2	Microprocessor Data Bus B2	P6-8	P3-10, U6-7, U7-7, U8-7, U10-7, and XA1-$\underline{E}$, XA2-$\underline{E}$, XA3-$\underline{E}$, XA4-E, XA5-$\underline{E}$
	µP B3	Microprocessor Data Bus B3	P6-21	P3-23, U6-8, U7-8, U8-8, U10-8, and XA1-27, XA2-27, XA3-27, XA4-27, XA5-27
	µP B4	Microprocessor Data Bus B4	P6-7	P3-11, U6-13, U7-13, U8-13, U10-13, and XA1-$\underline{D}$, XA2-$\underline{D}$ XA3-$\underline{D}$, XA4-D, XA5-$\underline{D}$
	µP B5	Microprocessor Data Bus B5	P6-20	P3-24, U6-14, U7-14, U8-14, U10-14, and XA1-26, XA2-26, XA3-26, XA4-26, XA5-26
	µP B6	Microprocessor Data Bus B6	P6-6	P3-12, U6-17, U7-17, U8-17, U10-17, and XA1-$\underline{C}$, XA2-$\underline{C}$, XA3-$\underline{C}$, XA4-C, XA5-$\underline{C}$

* L = Low-Active State, H = High Active State

Table 7-17. Motherboard Wire List, Signal Mnemonic Order (Continued) – PCB Revision: E

SIGNAL MNEMONIC*	SIGNAL NAME	SOURCE CONNECTOR & PIN NUMBER OR A14 PCB COMPONENT	DESTINATION CONNECTOR & PIN NUMBER OR A14 PCB COMPONENT
µP MSB (B7)	Microprocessor Data Bus B7 (MSB)	P6-19	P3-25, U6-18, U7-18, U8-18, U10-18, and XA1-25, XA2-25, XA3-25, XA4-25, XA5-25
MOD DRIVER 1	Modulator Driver, Oscillator 1	XA6-K	P14-1
MOD DRIVER 2	Modulator Driver, Oscillator 2	XA7-K	P13-1
MOD DRIVER 3	Modulator Driver, Oscillator 3	XA8-K	P17-1
MOD DRIVER 4	Modulator Driver, Oscillator 4	XA9-K	P16-1
L MODIFY ACTIVE	Modify Active	XA3-19	P5-16
L MODIFY CLEAR (SX29)	Modify Clear (SX29)	P5-15	XA3-16
MODIFY SIGNAL	Modify Signal Input, INCREASE/DECREASE Control (Front Panel)	P5-4	XA3-U
$\overline{\text{NDAC}}$	Not Data Accepted - GPIB	P4-24	XA1-3
$\overline{\text{NRFD}}$	Not Ready For Data - GPIB	P4-13	XA1-A
PIN MOD DRIVER	Pin Switch Modulator Driver	XA4-S	XA6-7, XA7-7, XA8-7, XA9-7
L PIN SELECT 1	Pin Switch Select, Oscillator 1	XA6-A	XA4-5, CR18-Cathode
L PIN SELECT 2	Pin Switch Select, Oscillator 2	XA7-A	CR20 - Cathode
L PIN SELECT 3	Pin Switch Select, Oscillator 3	XA8-A	CR22 - Cathode
L PIN SELECT 4	Pin Switch Select, Oscillator 4	XA9-A	CR24 - Cathode
L PIN SW OFF	RETRACE RF Off (Front Panel Switch)	XA4-X	XA6-6, XA7-6, XA8-6, XA9-6
RAMP INPUT	Sweep Ramp Input, A5 PCB	XA2-T	XA5-16
RAMP, 0-10V	Sweep Ramp Input, A3 PCB	XA5-15	XA3-T
RAMP OUTPUT	Sweep Ramp Output, A2 PCB	XA2-T	XA5-16
RAMP OUT	Sweep Ramp Output, A5 PCB	XA5-15	XA3-T
L REMOTE	REMOTE LED (Front Panel)	XA1-17	P6-17
$\overline{\text{REN}}$	Remote Enable - GPIB	P4-26	XA1-1
L RESET OUT	Reset Out (from A12 PCB)	P6-4	XA1-24
L RETRACE BLANKING	Retrace Blanking, (Internal Use)	XA2-18&V	XA1-V, XA3-18&V, XA4-18
RETRACE BLANKING (-)	RETRACE BLANKING OUTPUT (-) (Rear Panel Connector)	XA2-4	XA16-14
RETRACE BLANKING (+)	RETRACE BLANKING OUTPUT (+) (Rear Panel Connector)	XA2-5	XA16-9
RF MARKER	RF Marker	XA3-W	XA4-19
L RF OFF	RF Off (Front Panel Switch)	XA4-V	XA6-5, XA7-5, XA8-5, XA9-5
ROM BØ (LSB)	Linearizer ROM Address Bus BØ (LSB)	U6-2	XA6-28, XA7-28, XA8-28, XA9-28
ROM B1	Linearizer ROM Address Bus B1	U6-5	XA6-27, XA7-27, XA8-27, XA9-27
ROM B2	Linearizer ROM Address Bus B2	U6-6	XA6-26, XA7-26, XA8-26, XA9-26
ROM B3	Linearizer ROM Address Bus B3	U6-9	XA6-25, XA7-25, XA8-25, XA9-25
ROM B4	Linearizer ROM Address Bus B4	U6-12	XA6-24, XA7-24, XA8-24, XA9-24
ROM B5	Linearizer ROM Address Bus B5	U6-15	XA6-23, XA7-23, XA8-23, XA9-23

* L = Low-Active State, H = High Active State

Table 7-17. Motherboard Wire List, Signal Mnemonic Order (Continued) – PCB Revision: E

SIGNAL MNEMONIC*	SIGNAL NAME	SOURCE CONNECTOR & PIN NUMBER OR A14 PCB COMPONENT	DESTINATION CONNECTOR & PIN NUMBER OR A14 PCB COMPONENT
ROM B6	Linearizer ROM Address Bus B6	U6-16	XA6-22, XA7-22, XA8-22, XA9-22
ROM B7 (MSB)	Linearizer ROM Address Bus B7 (MSB)	U6-19	XA6-21, XA7-21, XA8-21, XA9-21
H SEQ	Sequential Sync (Internal Use)	XA2-16	XA1-T
SEQ SYNC	SEQ SYNC OUTPUT (Rear Panel Connector)	XA2-6	XA16-7
RF SLOPE	RF Slope (Front Panel Control)	P7-12	XA4-U
H SNB 1	Select Next Band (End Osc. #1)	XA6-C	XA7-3
H SNB 2	Select Next Band (End Osc. #2)	XA7-C	XA8-3
H SNB 3	Select Next Band (End Osc. #3)	XA8-C	XA9-3
H SNR 1	Select Next Linearizer ROM (End Osc. #1 ROM)	XA6-D	XA7-4 & U7-13
H SNR 2	Select Next Linearizer ROM (End Osc. #2 ROM)	XA7-D	XA8-4 & U7-14
H SNR 3	Select Next Linearizer ROM (End Osc. #3 ROM)	XA8-D	XA9-4 & U7-17
H SNR 4	Select Next Linearizer ROM (End Osc. #4 ROM)	XA9-D	U7-18
SP0	Select μP Output Port #0	P7-21	XA5-24, P3-21
SP1	Select μP Output Port #1	P7-8	XA5-23, P3-8
SP2	Select μP Output Port #2	P7-20	XA5-22, P3-20
SP3	Select μP Output Port #3	P7-7	XA5-21, P3-7
SP4	Select μP Output Port #4	P7-19	XA5-20, P3-19
SP5	Select μP Output Port #5	P5-22	U6-1, P3-4
SP6	Select μP Output Port #6	P7-6	XA5-19, P3-6
SP7	Select μP Output Port #7	P7-18	XA5-18, P3-18
SP8	Select μP Output Port #8	P5-12	XA4-21, P3-5
SP9	Select μP Output Port #9	P5-7	XA3-B̄, P3-3
SP10	Select μP Output Port #10	P5-20	XA3-24, P3-16
SP11	Select μP Output Port #11	P5-6	XA3-Ā, P3-2
SP12	Select μP Output Port #12	P5-19	XA3-23, P3-15
SP13	Select μP Output Port #13	P5-14	XA2-B̄, P3-1
SP14	Select μP Output Port #14	P5-1	XA2-24, P3-14
SP15	Select μP Output Port #15	P5-11	XA4-20, P3-17
SP23 (L DOP)	Select μP Output Port #23	P6-2	XA1-22
$\overline{SRQ}$	Service Request - GPIB	P4-10	XA1-D
L SRQ	SRQ LED (Front Panel)	XA1-18	P6-16
H SWP	Forward Sweep in Progress	XA2-23	P5-2
SX1	Select μP Input Port #1	P5-25	U7-1
SX2	Select μP Input Port #2	P5-23	U8-1
SX3 (L KSV)	Select μP Input Port #3	XA1-B̄	P6-5
SX4	Select μP Input Port #4	P5-3	XA3-17
SX7	Select μP Input Port #7	P5-21	U10-1
SX29 (L MODIFY CLEAR)	Select μP Input Port #29	P5-15	XA3-16
TALK	TALK LED (Front Panel)	XA1-20	P6-14
TRACK FILTER 1	Tracking Filter, Oscillator 1	XA6-F	XA10-Ē
TRACK FILTER 2	Tracking Filter, Oscillator 2	XA7-F	XA10-27
TRACK FILTER COIL (SOURCE)	Tracking Filter Coil Source	XA10-22	P14-9
TRACK FILTER COIL (RTN)	Tracking Filter Coil Return	P16-8	XA10-16
YIG 1 BIAS GND SENSE	YIG Bias Ground Sense, Osc. 1	XA6-N	P14-2
YIG 2 BIAS GND SENSE	YIG Bias Ground Sense, Osc. 2	XA7-N	P13-2
YIG 3 BIAS GND SENSE	YIG Bias Ground Sense, Osc. 3	XA8-N	P17-2

* L = Low-Active State, H = High Active State

Table 7-17. Motherboard Wire List, Signal Mnemonic Order (Continued) – PCB Revision: E

SIGNAL MNEMONIC*	SIGNAL NAME	SOURCE CONNECTOR & PIN NUMBER OR A14 PCB COMPONENT	DESTINATION CONNECTOR & PIN NUMBER OR A14 PCB COMPONENT
YIG 4 BIAS GND SENSE	YIG Bias Ground Sense, Osc. 4	XA9-N	P16-2
YIG 1 COIL (-)	YIG Coil (-), Osc. 1	XA6-U	P19-2
YIG 1 COIL (+)	YIG Coil (+), Osc. 1	XA6-T	P14-6
YIG 2 COIL (-)	YIG Coil (-), Osc. 2	XA7-U	P22-2
YIG 2 COIL (+)	YIG Coil (+), Osc. 2	XA7-T	P13-6
YIG 3 COIL (-)	YIG Coil (-), Osc. 3	XA8-U	P29-2
YIG 3 COIL (+)	YIG Coil (+), Osc. 3	XA8-T	P17-6
YIG 4 COIL (-)	YIG Coil (-), Osc. 4	XA9-U	P26-2
YIG 4 COIL (+)	YIG Coil (+), Osc. 4	XA9-T	P16-6
L YIG 1 FM COIL SEL	YIG FM Coil Select, Osc. 1	XA6-E	XA10-F̄, U7-3
L YIG 2 FM COIL SEL	YIG FM Coil Select, Osc. 2	XA7-E	XA10-28, U7-4
L YIG 3 FM COIL SEL	YIG FM Coil Select, Osc. 3	XA8-E	XA10-M, U7-7
L YIG 4 FM COIL SEL	YIG FM Coil Select, Osc. 4	XA9-E	XA10-L, U7-8
YIG 1 TUNE CONTROL	Tuning Control, Oscillator 1	XA6-V	P19-3
YIG 2 TUNE CONTROL	Tuning Control, Oscillator 2	XA7-V	P22-3
YIG 3 TUNE CONTROL	Tuning Control, Oscillator 3	XA8-V	P29-3
YIG 4 TUNE CONTROL	Tuning Control, Oscillator 4	XA9-V	P26-3
YIG 1 TUNE SUPPLY	Tuning-Supply Switch, Oscillator 1	XA6-W	P20-3
YIG 2 TUNE SUPPLY	Tuning-Supply Switch, Oscillator 2	XA7-W	P23-3
YIG 3 TUNE SUPPLY	Tuning-Supply Switch, Oscillator 3	XA8-W	P30-3
YIG 4 TUNE SUPPLY	Tuning-Supply Switch, Oscillator 4	XA9-W	P27-3
H UNLEVELED	Unleveled Condition	XA4-22	XA1-Ā, P5-13
1V/GHZ	1 V/GHZ OUTPUT (Rear Panel Connector)	XA5-9	XA16-13
VIDEO MARKER	MARKER OUTPUT (Rear Panel Connector)	XA3-8	XA16-8
.01-2GHZ DETECTOR IN	.01 - 2 GHz Detector Input	P35-3	XA4-A
.01-2GHZ DETECTOR RTN	.01 - 2 GHz Detector Return	P35-2	XA4-1
.01-2GHZ THERMISTOR	.01 - 2 GHz Thermistor	P35-1	XA4-2
2-18GHZ DETECTOR IN	2 - 18 GHz Detector Input	P36-3	XA4-C
2-18GHZ DETECTOR RTN	2-18 GHz Detector Return	P36-2	XA4-3
2-18GHZ THERMISTOR	2 - 18 GHz Thermistor	P36-1	XA4-B
+10V REF	+10V Reference	XA5-S	XA6-12, XA7-12, XA8-12, XA9-12
ΔF >50 MHz	Sweep Width (ΔF) >50 MHz	XA5-X	XA6-17, XA7-17, XA8-17, XA9-17
ΔF ≤50 MHz	Sweep Width (ΔF) ≤50 MHz	XA5-K	XA10-U
ΔF ≤50 MHz RTN	Sweep Width (ΔF) ≤50 MHz Return	XA5-L	XA10-T
H 10DB ATTN DRVR (PURPLE)	10 dB Attenuator Driver (Purple Wire)	XA10-14	P31-2
L 10DB ATTN DRVR (YELLOW)	10 dB Attenuator Driver (Yellow Wire)	XA10-15	P31-1
H 20DB ATTN DRVR (BLACK)	20 dB Attenuator Driver (Black Wire)	XA10-8	P31-8
L 20 DB ATTN DRVR (GREEN)	20 dB Attenuator Driver (Green Wire)	XA10-9	P31-7
HA40DB ATTN DRVR (ORANGE)	40 dB Attenuator Driver (Orange Wire)	XA10-10	P31-6
LA 40DB ATTN DRVR (BLUE)	40 dB Attenuator Driver (Blue Wire)	XA10-11	P31-5
HB 40DB ATTN DRVR (WHITE)	40 dB Attenuator Driver (White Wire)	XA10-13	P31-3
LB 40DB ATTN DRVR (BROWN)	40 dB Attenuator Driver (Brown Wire)	XA10-12	P31-4

* L = Low-Active State, H = High Active State

Table 7-18. Power Supply Voltages, Distribution (XA-Numbered Connectors)

VOLTAGE	SOURCE	DESTINATION CONNECTOR AND PIN #, A14 BOARD									
		XA1	XA2	XA3	XA4	XA5	XA6	XA7	XA8	XA9	XA10
+5	XA13-16, 17, T, & U	14, R	14, R	14, R	14, R	14, R	11, M	11, M	11, M	11, M	6, F
+12/-24 (UNREG)	XA13-19						1	1	1	1	
+15	A0U3-3		11, M	11, M	11, M	11, M	8	8	8	8	
+15 HC	A0U4-3										24, A
-15	A0U1-3		12, N	12, N	12, N	12, N	9	9	9	9	
-15 HC	A0U2-3										23, B
+18 (UNREG)	XA13-26						B	B	B	B	
+24	A14U2-3										
+28 (UNREG)	XA13-21, Y										
-39V	A0Q1-Collector										

Table 7-19. Power Supply Voltages, Distribution (P-Numbered Connectors)

VOLTAGE	SOURCE	DESTINATION CONNECTOR AND PIN #, A14 BOARD													
		P3	P5	P6	P7	P12	P13	P14	P16	P17	P20	P23	P24	P27	P30
+5	XA13-16, 17, T, & U	26		25	16,17		15	15					1		
+12/-24 (UNREG)	XA13-19														
+15	A0U3-3		9												
+15 HC	A0U4-3					5	5	5	5	5					
-15	A0U1-3		8												
-15 HC	A0U2-3					3							2		
+18 (UNREG)	XA13-26														
+24	A14U2-3					2									
+28 (UNREG)	XA13-21, Y						4	4	4	4					
-39V	A0Q1-Collector										1	1		1	1

Table 7-20. Motherboard Wire List Connector Order

CONNECTOR & PIN NO.		SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
P1	- 1	FILTERED AC LINE VOLTAGE (HOT)	A14L2	VSM-R**
	- 2	EARTH GROUND	VSM-G	XA13-14, 15, R & S
	- 3	FILTERED AC LINE VOLTAGE (NEUTRAL)	A14L1	VSM-P
	- 4	AC LINE VOLTAGE (NEUTRAL)	A0S1-5	A14L1
	- 5	AC LINE VOLTAGE (HOT)	A0S1-2	A14L2
	- 6	INPUT LINE VOLTAGE (NEUTRAL)	VSM-1	A14RT2
	- 7	165V RTN	VSM-E	XA13-2 & B
	- 8	INPUT LINE VOLTAGE (HOT)	A0S1-3	A14RT1
	- 9	12 VAC NEUTRAL	A0T1-RED	A14CR9 - Cathode, A14CR8-Anode
	- 10	12 VAC HOT	A0T1-RED	A14CR6 - Cathode, A14CR7 - Anode
P2	- 1	GROUND	A14 Ground Plane	A0U2-1
	- 2	CONTROL	A14R11/R12	A0U2-2
	- 3	+15V OUT	A14R11	A0U2-3
	- 4	-18V IN	XA13-22, 23 A & B	A0U2-4
P3	- 1	SP13	P5-14	
	- 2	SP11	P5-6	
	- 3	SP9	P5-7	No
	- 4	SP 5	P5-22	
	- 5	SP 8	P5-12	mating
	- 6	SP 6	P7-6	
	- 7	SP 3	P7-7	connector.
	- 8	SP 1	P7-8	
	- 9	μP LSB (BØ)	P6-9	Used
	- 10	μP B2	P6-8	
	- 11	μP B4	P6-7	for
	- 12	μP B6	P6-6	
	- 13	ANALOG GND 1	A14 Ground Plane	monitoring
	- 14	SP14	P5-1	
	- 15	SP12	P5-19	Bus &
	- 16	SP10	P5-20	
	- 17	SP15	P5-11	SP
	- 18	SP7	P7-18	
	- 19	SP4	P7-19	lines
	- 20	SP2	P7-20	
	- 21	SPØ	P7-21	
	- 22	μP B1	P6-22	
	- 23	μP B3	P6-21	
	- 24	μP B5	P6-19	
	- 25	μP MSB (B7)	P6-20	
	- 26	+5V		
P4	- 1	ADRS SW S3	XA1-P	A18J1-1
	- 2	ADRS SW S2	XA1-N	A18J1-2
	- 3	ADRS SW S1	XA1-M	A18J1-3
	- 4	LOGIC GND	XA1-L	A18J1-4
	- 5	DIO 4	XA1-K	A18J1-5
	- 6	DIO 1	XA1-J	A18J1-6
	- 7	DIO 2	XA1-H	A18J1-7
	- 8	DIO 3	XA1-F	A18J1-8
	- 9	EOI	XA1-E	A18J1-9
	- 10	SRQ	XA1-D	A18J1-10
	- 11	DAV	XA1-C	A18J1-11
	- 12	ATN	XA1-B	A18J1-12
	- 13	NRFD	XA1-A	A18J1-13
	- 14	ADRS SW S4	XA1-13	A18J1-14
	- 15	ADRS SW S5	XA1-12	A18J1-15

* L = Low-Active State, H = High-Active State
**Line Voltage Selector Module

Table 7-20. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.		SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
P4	- 16	CR/CR-LF	XA1-11	A18J1-16
(Cont.)	- 17	BUS GND	XA1-10	A18J1-17
	- 18	$\overline{\text{DIO 5}}$	XA1-9	A18J1-18
	- 19	$\overline{\text{DIO 8}}$	XA1-8	A18J1-19
	- 20	$\overline{\text{DIO 7}}$	XA1-7	A18J1-20
	- 21	$\overline{\text{DIO 6}}$	XA1-6	A18J1-21
	- 22	BUS GND	XA1-5	A18J1-22
	- 23	Not Used	XA1-4	A18J1-23
	- 24	$\overline{\text{NDAC}}$	XA1-3	A18J1-24
	- 25	$\overline{\text{IFC}}$	XA1-2	A18J1-25
	- 26	$\overline{\text{REN}}$	XA1-1	A18J1-26
P5	- 1	SP14	A12P5-1	XA2-24, P3-14
	- 2	H SWP	XA2-23	A12P5-2
	- 3	SX4	A12P5-3	XA3-17
	- 4	H MODIFY SIGNAL	A12P5-4	XA3-U
	- 5	M1 IDENTIFY	A12P5-5	XA3-21
	- 6	SP11	A12P5-6	XA3-$\overline{\text{A}}$, P3-2
	- 7	SP9	A12P5-7	XA3-$\overline{\text{B}}$, P3-3
	- 8	-15V	A0U1-3	A12P5-8
	- 9	+15V	A0U3-3	A12P5-9
	- 10	ANALOG GND 1	A14 Ground Plane	A12P5-10
	- 11	SP15	A12P5-11	XA4-20, P3-17
	- 12	SP8	A12P5-12	XA4-21, P3-5
	- 13	H UNLC	A12P5-13	XA4-22
	- 14	SP13	A12P5-14	XA2-$\overline{\text{B}}$, P3-1
	- 15	MODIFY CLEAR (SX29)	A12P5-15	XA3-16
	- 16	L MODIFY ACTIVE	XA3-19	A12P5-16
	- 17	M2 IDENTIFY	A12P5-17	XA3-X
	- 18	F0 IDENTIFY	A12P5-18	XA3-22
	- 19	SP12	A12P5-19	XA3-23, P3-15
	- 20	SP10	A12P5-20	XA3-24, P3-16
	- 21	SX7	A12P5-21	A14U10-1
	- 22	SP5	A12P5-22	A14U6-1, P3-4
	- 23	SX2	A12P5-23	A14U5-1
	- 24	L EGD	XA4-17	A12P5-24
	- 25	SX1	A12P5-25	A14U7-1
	- 26	SXØ (Unused)		
P6	- 1	DOS	XA1-21	A12P6-1
	- 2	L DOP (SP23)	XA1-22	A12P6-2
	- 3	KPS	XA1-23	A12P6-3
	- 4	L RESET OUT	XA1-24	A12P6-4
	- 5	L KSV (SX3)	XA1-$\overline{\text{B}}$	A12P6-5
	- 6	µP B6	A12P6-6	P3-12, A14U6-17, U7-17, U8-17, U10-17, XA1-$\overline{\text{C}}$, XA3-$\overline{\text{C}}$, XA4-$\overline{\text{C}}$, XA5-$\overline{\text{C}}$
	- 7	µP B4	A12P6-7	P3-11, A14U6-13, U7-13, U8-13, U10-13, XA1-$\overline{\text{D}}$, XA2-$\overline{\text{D}}$, XA3-$\overline{\text{D}}$, XA4-$\overline{\text{D}}$, XA5-$\overline{\text{D}}$
	- 8	µP B2	A12P6-8	P3-10, A14U6-7, U7-7, U8-7, U10-7, XA1-$\overline{\text{E}}$, XA2-$\overline{\text{E}}$, XA3-$\overline{\text{E}}$, XA4-$\overline{\text{E}}$, XA5-$\overline{\text{E}}$
	- 9	µP LSB (BØ)	A12P6-9	P3-9, A14U6-3, U7-3, U8-3, U10-3, XA1-$\overline{\text{F}}$, XA2-$\overline{\text{F}}$, XA3-$\overline{\text{F}}$, XA4-$\overline{\text{F}}$, XA5-$\overline{\text{F}}$
	- 10, - 11	+5V RTN	A14 Ground Plane	A12P6-10, A12P6-11
	- 12, - 13	+5V	XA13-T, U, 16 and 17	A12P6-12, A12P6-13

* L = Low-Active State, H = High-Active State

Table 7-20. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.		SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
P6 (Cont.)	- 14	TALK	XA1-20	A12P6-14
	- 15	LOCAL LOCKOUT	XA1-19	A12P6-15
	- 16	SRQ	XA1-18	A12P6-16
	- 17	REMOTE	XA1-17	A12P6-17
	- 18	LISTEN	XA1-16	A12P6-18
	- 19	µP MSB (B7)	A12P6-19	P3-25, A14U6-18, U7-18, U8-18, U10-18, XA1-25, XA2-25, XA3-25, XA4-25, XA5-25
	- 20	µP B5	A12P6-20	P3-24, A14U6-14, U7-14, U8-14, U10-14, XA1-26, XA2-26, XA3-26, XA4-26, XA5-26
	- 21	µP B3	A12P6-21	P3-23, A14U6-8, U7-8, U8-8, U10-8, XA1-27, XA2-27, XA3-27, XA4-27, XA5-27
	- 22	µP B1	A12P6-22	P3-22, A14U6-4, U7-4, U8-4, U10-4, XA1-28, XA2-28, XA3-28, XA4-28, XA5-28
	- 23, - 24	+5V RTN	A14 Ground Plane	A12P6-23, A12P6-24
	- 25, - 26	+5V	XA13 T, U, 16 and 17	A12P6-25, A12P6-25
P7	- 1, - 2	+5V RTN FOR A11 PCB	A14 Ground Plane	A12P7-1, A12P7-2
	- 3, - 4	+5V FOR A11 PCB	XA13, T, U, 16 and 17	A12P7-3, A12P7-4
	- 5	MAN SWEEP INPUT	A12P7-5	XA5-17
	- 6	SP6	A12P7-6	XA5-19, P3-6
	- 7	SP3	A12P7-7	XA5-21, P3-7
	- 8	SP1	A12P7-8	XA5-23, P3-8
	- 9	Vacant		
	- 10	Vacant		
	- 11	Vacant		
	- 12	RF SLOPE(S)	A12P7-12	XA4-U
	- 13	+10V REF	XA5-S	A12P7-13
	- 14, - 15	+5V RTN FOR A11 PCB	A14 Ground Plane	A12P7-14, A12P7-15
	- 16, - 17	+5V FOR A11 PCB	XA13-T, U, 16 and 17	A12P7-16, A12P7-17
	- 18	SP7	A12P7-18	XA5-18, P3-18
	- 19	SP4	A12P7-19	XA5-20, P3-19
	- 20	SP2	A12P7-20	XA5-22, P3-20
	- 21	SPØ	A12P7-21	XA5-24, P3-21
	- 22	MARKER AMPL(CW)	XA3-2	A12P7-22
	- 23	MARKER AMPL(S)	XA3-Y	A12P7-23
	- 24	MARKER AMPL(CCW)	XA3-L	A12P7-24
	- 25	ANALOG GND 1	A14 Ground Plane	A12P7-25
	- 26	FCEN/VPF	XA8-16	A12P7-26
P8		Not Used		
P10	- 1	SHIELD LEAD	EXT AM INPUT (SHIELD)	
	- 2	EXT AM INPUT	EXT AM INPUT	XA4-16
	- 3	SHIELD LEAD	EXT SQ WAVE INPUT (SHIELD)	
	- 4	EXT SQ WAVE IN	EXT SQ WAVE INPUT	XA4-15

* L = Low-Active State, H = High-Active State

Table 7-20. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
P12 - 1	SPARE		
- 2	+24V	A14U2-3	HDC +24V**
- 3	-15V HC	A0U2-3	HDC -15V
- 4	Vacant		
- 5	+15V HC	A0U4-3	HDC +15V**
P13 - 1	MOD DRIVER 2	XA7-K	No connection
- 2	YIG 2 BIAS GND SENSE	See Fig. 7-84 or 7-85	XA7-N
- 3	A7Q1 BIAS	P21-2	
- 4	+28V	XA13-21, Y	
- 5	+15V HC	A14C16	See Fig.
- 6	YIG 2 COIL (+)	XA7-T	7-84 or 7-85
- 7	YIG 2 COIL (-)	XA7-U	
- 8	TRACK FILTER 2 COIL (+)	See Fig. 7-84 or 7-85	P17-9
- 9	TRACK FILTER 1 COIL (+)	P14-8	See Fig. 7-84 or 7-85
- 10	FM COIL 2, WJ (+)	YIG	P17-11
- 11	FM COIL 1, WJ (+)	P14-10	See Fig. 7-84 or 7-85
- 12	FM COIL 2, AVANTEK (+)	See Fig. 7-84 or 7-85	P17-13
- 13	FM COIL 1, AVANTEK (+)	P14-12	
- 14	Vacant		
- 15	+5V	XA3-T, U, 16, 17	See Fig. 7-84 or 7-85
- 16	+5V RETURN	A14 Ground Plane	
P14 - 1	MOD DRIVER 1	XA6-K	No connection
- 2	YIG 1 BIAS GND SENSE	See Fig. 7-83	XA6-N
- 3	A6Q1 BIAS	P18-2	
- 4	+28V	XA13-21, Y	
- 5	+15V HC	A14C16	See Fig. 7-83
- 6	YIG 1 COIL (+)	XA6-T	
- 7	YIG 1 COIL (-)	XA6-U	
- 8	TRACK FILTER 1 COIL (+)	P19	P13-9
- 9	TRACK FILTER COIL (SOURCE)	XA10-22	See Fig. 7-83
- 10	FM COIL 1, WJ (+)	See Fig. 7-83	P13-11
- 11	FM COIL, WJ (SOURCE)	XA10-21	See Fig. 7-83
- 12	FM COIL 1, AVANTEK (+)	See Fig. 7-83	P13-13
- 13	FM COIL, AVANTEK (SOURCE)	XA10-20	
- 14	Vacant		See Fig. 7-83
- 15	+5V	XA13-T, U16 & 17	
- 16	+5V RETURN	A14 Ground Plane	
P15 - 1	.01-8 GHz PIN PORT SEL	A14R105	Not Used
- 2	HET PORT SELECT	A14R107	PIN Switch T5/T1
- 3	PIN PORT 1 SEL	A14R108	PIN Switch T6
- 4	PIN PORT 2 SEL	A14Q13-E	Pin Switch T7
- 5	PIN PORT 3 SEL	A14Q14-E	PIN Switch T8
- 6	PIN PORT 4 SEL	A14Q17-E	Not Used
- 7	MOD ATTN (GREEN)	XA6-K, via A14R34	PIN Switch T2
- 8	PIN PORT 2 ATTN (BLUE)	XA7-K, via A14R37	PIN Switch T4
- 9	PIN PORT 3 ATTN (WHITE)	XA8-K, via A14R50	PIN Switch T3
- 10	PIN PORT 4 ATTN	XA9-K, via A14R68	Not Used
P16	Not Used		
P17 - 1	MOD DRIVER 3	XA8-K	No connection
- 2	YIG 3 BIAS GND SENSE	See Fig. 7-84 or 7-85	XA8-N
- 3	A8Q1 BIAS	P28-2	
- 4	+28V	XA13-21, Y	
- 5	+15V HC	A14C16	See Fig. 7-84 or 7-85
- 6	YIG 3 COIL (+)	XA8-T	
- 7	YIG 3 COIL (-)	XA8-U	
- 8	TRACK FILTER 3 COIL (+)	See Fig. 7-84 or 7-85	P16-9
- 9	TRACK FILTER 2 COIL (+)	P13-8	See Fig. 7-84 or 7-85

* L = Low-Active State, H = High-Active State
**Line Voltage Selector Module

Table 7-20. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
P17 (Cont.) - 10	FM COIL 3, WJ (+)	See Fig. 7-84 or 7-85	P16-11
- 11	FM COIL 2, WJ (+)	P13-10	See Fig. 7-84 or 7-85
- 12	FM COIL 3, AVANTEK (+)	See Fig. 7-84 or 7-85	P16-13
- 13	FM COIL 2, AVANTEK (+)	P13-12	See Fig. 7-84 or 7-85
- 14	Vacant		
- 15	Vacant		
- 16	Vacant		
P18 - 1	A6Q1-E	XA6-P	A6Q1-E
- 2	A6Q1-C	A6Q1-C	P14-3 & XA6-R
- 3	A6Q1-B	XA6-S	A6Q1-B
P19 - 1	A6Q2-E	CR15-Anode & P20-2	A6Q2-E
- 2	A6Q2-C	A6Q2-C	P14-7 & XA6-U
- 3	A6Q2-B	XA6-V	A6Q2-B
P20 - 1	A6Q3-E (-38V)	-38V	A6Q3-E
- 2	A6Q3-C	A6Q3-C	P19-1
- 3	A6Q3-B	XA6-W & A14R36	A6Q3-B
P21 - 1	A7Q1-E	XA7-P	A7Q1-E
- 2	A7Q1-C	A7Q1-C	P13-3 & XA7-R
- 3	A7Q1-B	XA7-S	A7Q1-B
P22 - 1	A7Q2-E	CR16-Anode & P23-2	A7Q2-E
- 2	A7Q2-C	A7Q2-C	P13-7 & XA7-U
- 3	A7Q2-B	XA7-V	A7Q2-B
P23 - 1	A7Q3-E (-38V)	-38V	A7Q3-E
- 2	A7Q3-C	A7Q3-C	P22-1
- 3	A7Q3-B	XA7-W & A14R39	A7Q3-B
P24 - 1	+5V	A14C22	P13-15 & P14-15
- 2	-15V HC	A0U2-3	A14C16
- 3	GROUND	A14 Ground Plane	P13-16 & P14-16
P25 - 1	A9Q1-E	XA9-P	A9Q1-E
- 2	A9Q1-C	A9Q1-C	P16-3 & XA9-R
- 3	A9Q1-B	XA9-S	A9Q1-B
P26 - 1	A9Q2-E	CR23-Anode & P27-2	A9Q2-E
- 2	A9Q2-C	A9Q2-C	XA9-U & P16-7
- 3	A9Q2-B	XA9-V	A9Q2-B
P27 - 1	A9Q3-E (-38V)	-38V	A9Q3-E
- 2	A9Q3-C	A9Q3-C	P26-1
- 3	A9Q3-B	XA9-W & A14R61	A9Q3-B
P28 - 1	A8Q1-E	XA8-P	A8Q1-E
- 2	A8Q1-C	A8Q1-C	P17-3 & XA8-R
- 3	A8Q1-B	XA8-S	A8Q1-B
P29 - 1	A8Q2-E	CR21-Anode & P30-2	A8Q2-E
- 2	A8Q2-C	A8Q2-C	XA8-U
- 3	A8Q2-B	XA8-V	A8Q2-B

* L = Low-Active State, H = High-Active State

Table 7-20. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
P30 - 1	A8Q3-E (-39V)	-39V	A8Q3-E
- 2	A8Q3-C	A8Q3-C	P29-1
- 3	A8Q3-B	XA8-W & A14R69	A8Q3-B
P31 - 1	L 10DB ATTN DRVR (YELLOW)	XA10-15	
- 2	H 10 DB ATTN DRVR (PURPLE)	XA10-14	
- 3	HB 40DB ATTN DRVR (WHITE)	XA10-13	Option 2
- 4	LB 40DB ATTN DRVR (BROWN)	XA10-12	70 dB Step
- 5	LA 40DB ATTN DRVR (BLUE)	XA10-11	Attenuator
- 6	HA 40DB ATTN DRVR (ORANGE)	XA10-10	
- 7	L 20DB ATTN DRVR (GREEN)	XA10-9	
- 8	H 20DB ATTN DRVR (BLACK)	XA10-8	
P33	Not Used		
P34 - 1	EXT FM INPUT	EXT FM ∅ LOCK INPUT	XA10-S
- 2	GROUND	(Rear Panel Connector)	XA10-V
P35 - 1	.01-2GHz THERMISTOR		XA4-2
- 2	.01-2GHz DETECTOR RTN		XA4-1
- 3	.01-2GHz DETECTOR IN		XA4-A
P36 - 1	2-18GHz THERMISTOR		XA4-B
- 2	2-18GHz DETECTOR RTN		XA4-3
- 3	2-18GHz DETECTOR IN		XA4-C
P37 - 1	EXT DET RTN	EXTERNAL DETECTOR INPUT	XA4-4
- 2	EXT DET IN	(Front Panel Connector)	XA4-D
P39 - 1	EXT ALC GAIN (CW)	EXT ALC GAIN Potentiometer	XA4-E
- 2	EXT ALC GAIN (S)	EXT ALC GAIN Potentiometer	XA4-F
- 3	EXT ALC GAIN (CCW)	EXT ALC GAIN Potentiometer	XA4-J
XA1 - 1	$\overline{\text{REN}}$	P4-26	A1P1-1
- 2	$\overline{\text{IFC}}$	P4-25	A1P1-2
- 3	$\overline{\text{NDAC}}$	P4-24	A1P1-3
- 4	Not Used	P4-23	A1P1-4
- 5	BUS GND	P4-22	A1P1-5
- 6	$\overline{\text{DIO6}}$	P4-21	A1P1-6
- 7	$\overline{\text{DIO7}}$	P4-20	A1P1-7
- 8	$\overline{\text{DIO8}}$	P4-19	A1P1-8
- 9	$\overline{\text{DIO5}}$	P4-18	A1P1-9
- 10	BUS GND	P4-17	A1P1-10
- 11	CR/CR-LF	P4-16	A1P1-11
- 12	ADRS SW S5	P4-15	A1P1-12
- 13	ADRS SW S4	P4-14	A1P1-13
- 14	+5V	XA13-T, U, 16, 17	A1P1-14
- 15	+5V RETURN	A14 Ground Plane	A1P1-15
- 16	L LISTEN	A1P1-16	P6-18
- 17	L REMOTE	A1P1-17	P6-17
- 18	L SRQ	A1P1-18	P6-16
- 19	L LOCAL LOCKOUT	A1P1-19	P6-15
- 20	L TALK	A1P1-20	P6-14
- 21	L DOS	A1P1-21	P6-1
- 22	L DOP	A1P1-22	P6-2
- 23	L KPS	A1P1-23	P6-3

* L = Low-Active State, H = High-Active State

Table 7-20. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
XA1 - 24	L RESET OUT	A1P1-24	P6-4
(Cont.) - 25	µP MSB (B7)	P6-19	A1P1-25
- 26	µP B5	P6-20	A1P1-26
- 27	µP B3	P6-21	A1P1-27
- 28	µP B1	P6-22	A1P1-28
- A	NRFD	P4-13	A1P1-A
- B	ATN	P4-12	A1P1-B
- C	DAV	P4-11	A1P1-C
- D	SRQ	P4-10	A1P1-D
- E	EOI	P4-9	A1P1-E
- F	DIO3	P4-8	A1P1-F
- H	DIO2	P4-7	A1P1-H
- J	DIO1	P4-6	A1P1-J
- K	DIO4	P4-5	A1P1-K
- L	LOGIC GND	P4-4	A1P1-L
- M	ADRS SW S1	P4-3	A1P1-M
- N	ADRS SW S2	P4-2	A1P1-N
- P	ADRS SW S3	P4-1	A1P1-P
- R	+5V	XA13-T, U, 16, 17	A1P1-R
- S	+5V RETURN	A14 Ground Plane	A1P1-S
- T	H SEQ	XA2-16	A1P1-T
- U	L DWELL (LD)	A1P1-U	XA2-17
- V	L RETRACE BLANKING	XA2-18	A1P1-V
- W	Vacant		A1P1-W
- X	H INTENSITY MARKER	XA2-20	A1P1-X
- Y	Vacant		A1P1-Y
- Z̲	GPIB IN	A1P1-Z	A14U10-18
- A̲	H UNLC	XA4-22	A1P1-A̲
- B̲	L KSV (SX3)	P6-22	A1P1-B̲
- C̲	µP B6	P6-6	A1P1-C̲
- D̲	µP B4	P6-7	A1P1-D̲
- E̲	µP B2	P6-8	A1P1-E̲
- F̲	µP LSB BØ	P6-9	A1P1-F̲
XA2 - 1	Vacant		A2P1-1
- 2	BANDSWITCH BLANKING +	A2P1-2	XA16-5
- 3	BANDSWITCH BLANKING -	A2P1-3	XA16-12
- 4	RETRACE BLANKING (-)	A2P1-4	XA16-14
- 5	RETRACE BLANKING (+)	A2P1-5	XA16-9
- 6	SEQ SYNC	A2P1-6	XA16-7
- 7	Vacant		A2P1-7
- 8	Vacant		A2P1-8
- 9	ANALOG GND 2		A2P1-9
- 10	ANALOG GND 1	A14 Ground Plane	A2P1-10
- 11	+15V	A0U3-3	A2P1-11
- 12	-15V	A0U1-3	A2P1-12
- 13	+5V RETURN	A14 Ground Plane	A2P1-13
- 14	+5V	XA13-T, U, 16, 17	A2P1-14
- 15	L DWELL DETECTED	A2P1-15	A14U10-14
- 16	H SEQ	A2P1-16	XA1-T
- 17	L DWELL (LD)	XA1-U	A2P1-17
- 18	L RETRACE BLANKING	A2P1-18	XA1-V, XA3-18, V & XA4-18,
- 19	Vacant		A2P1-19
- 20	H INTENSITY MARKER	XA3-20	A2P1-20
- 21	H DWELL	A2P1-21	A14U8-3
- 22	Vacant		A2P1-22
- 23	H SWP	A2P1-23	P5-2
- 24	SP14	P5-1	A2P1-24
- 25	µP MSB (B7)	P6-19	A2P1-25
- 26	µP B5	P6-20	A2P1-26
- 27	µP B3	P6-21	A2P1-27
- 28	µP B1	P6-22	A2P1-28
- A	AC LINE VOLTAGE	CR10-Cathode	A2P1-A

* L = Low-Active State, H = High-Active State

Table 7-20. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
XA2 - B	EXT RAMP IN	XA16-1	A2P1-B
(Cont.) - C	Vacant		A2P1-C
- D	L EXT DWELL	XA16-3	A2P1-D
- E	L EXT TRIG PULSE IN	XA16-4	A2P1-E
- F	Vacant		A2P1-F
- H	L ACTIVATE RELAY	A2P1-H	A14K1
- J	Vacant		A2P1-J
- K	ANALOG GND 2	A14 Ground Plane	A2P1-K
- L	ANALOG GND 1		A2P1-L
- M	+15V	A0U3-3	A2P1-M
- N	-15V	A0U1-3	A2P1-N
- P	+5V RETURN	A14 Ground Plane	A2P1-P
- R	+5V	XA13-T, U, 16, 17	A2P1-R
- S	Vacant		A2P1-S
- T	RAMP OUTPUT	A2P1-T	XA5-16
- U	Vacant		A2P1-U
- V	L RETRACE BLANKING	A2P1-V	XA1-V; XA3-18, V; XA4-18,
- W	L LEVEL DIP	A2P1-W	XA4-W
- X	H INTENSITY MARKER	XA3-20	A2P1-X
- Y	H EXT FM ENABLE	A2P1-Y	XA10-5
- Z	L EOB	XA10-E	A2P1-Z
- $\overline{A}$	Vacant		A2P1-$\overline{A}$
- $\overline{B}$	SP13	P5-14	A2P1-$\overline{B}$
- $\overline{C}$	μP B6	P6-6	A2P1-$\overline{C}$
- $\overline{D}$	μP B4	P6-7	A2P1-$\overline{D}$
- $\overline{E}$	μP B2	P6-8	A2P1-$\overline{E}$
- $\overline{F}$	μP LSB (BØ)	P6-9	A2P1-$\overline{F}$
XA3 - 1	Vacant		A3P1-1
- 2	Vacant		A3P1-2
- 3	Vacant		A3P1-3
- 4	Vacant		A3P1-4
- 5	Vacant		A3P1-5
- 6	Vacant		A3P1-6
- 7	Vacant		A3P1-7
- 8	VIDEO MARKER	A3P1-8	XA16-8
- 9	ANALOG GND 2	A14 Ground Plane	A3P1-9
- 10	ANALOG GND 1		A3P1-10
- 11	+15V	A0U3-3	A3P1-11
- 12	-15V	A0U1-3	A3P1-12
- 13	+5V RETURN	A14 Ground Plane	A3P1-13
- 14	+5V	XA13-T, U, 16, 17	A3P1-14
- 15	Vacant		A3P1-15
- 16	L MODIFY CLEAR (SX29)	P5-15	A3P1-16
- 17	SX4	P5-3	A3P1-17
- 18	L RETRACE BLANKING	XA2-V,18	A3P1-18
- 19	L MODIFY ACTIVE	A3P1-19	P5-16
- 20	H INTENSITY MARKER	A3P1-20	XA2-X
- 21	L M1 IDENTIFY	P5-5	A3P1-21
- 22	L F0 IDENTIFY	P5-18	A3P1-22
- 23	SP12	P5-19	A3P1-23
- 24	SP10	P5-20	A3P1-24
- 25	μP MSB (B7)	P6-19	A3P1-25
- 26	μP B5	P6-20	A3P1-26
- 27	μP B3	P6-21	A3P1-27
- 28	μP B1	P6-22	A3P1-28
- A	Vacant		A3P1-A
- B	Vacant		A3P1-B
- C	Vacant		A3P1-C
- D	Vacant		A3P1-D
- E	Vacant		A3P1-E
- F	Vacant		A3P1-F
- H	Vacant		A3P1-H
- J	HORIZONTAL OUTPUT	A3P1-J	XA16-10
- K	ANALOG GND 2		

* L = Low-Active State, H = High-Active State

Table 7-20. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
XA3			A3P1-K
(Cont.) - L	ANALOG GND 1	A14 Ground Plane	A3P1-L
- M	+15V	A0U3-3	A3P1-M
- N	-15V	A0U1-3	A3P1-N
- P	+5V RETURN	A14 Ground Plane	A3P1-P
- R	+5V	XA13-T, U, 16, 17	A3P1-R
- S	Vacant		A3P1-S
- T	RAMP, 0-10V	A3P1-T	XA5-15
- U	MODIFY SIGNAL	P5-4	A3P1-U
- V	L RETRACE BLANKING	A3P1-V	XA4-18
- W	RF MARKER	A3P1-W	XA4-19
- X	L M2 IDENTIFY	P5-17	A3P1-X
- Y	MARKER AMPL(S)	P7-23	A3P1-Y
- Z̲	MARKER AMPL(CW)	P7-22	A3P1-Z̲
- A̲	SP11	P5-6	A3P1-A̲
- B̲	SP9	P5-7	A3P1-B̲
- C̲	μP B6	P6-6	A3P1-C̲
- D̲	μP B4	P6-7	A3P1-D̲
- E̲	μP B2	P6-8	A3P1-E̲
- F̲	μP LSB (BØ)	P6-9	A3P1-F̲
XA4 - 1	.01-2GHZ DETECTOR RTN	P35-2	A4P1-1
- 2	.01-2GHZ THERMISTOR	P35-1	A4P1-2
- 3	2-18GHZ DETECTOR RTN	P36-2	A4P1-3
- 4	EXT DET RTN	P37-1	A4P1-4
- 5	Vacant		A4P1-5
- 6	Vacant		A4P1-6
- 7	Vacant		A4P1-7
- 8	Vacant		A4P1-8
- 9	Vacant		A4P1-9
- 10	ANALOG GND 1		A4P1-10
- 11	+15V	A0U3-3	A4P1-11
- 12	-15V	A0U1-3	A4P1-12
- 13	+5V RETURN	A14 Ground Plane	A4P1-13
- 14	+5V	XA13-T, U, 16, 17	A4P1-14
- 15	EXT SQ WAVE IN	P10-4	A4P1-15
- 16	EXT AM INPUT	P10-2	A4P1-16
- 17	L EGD	A4P1-17	P5-24
- 18	L RETRACE BLANKING	XA2-18,V	A4P1-18
- 19	RF MARKER	XA3-W	A4P1-19
- 20	SP15	P5-11	A4P1-20
- 21	SP8	P5-12	A4P1-21
- 22	H UNLC	A4P1-22	P5-13
- 23	H ATTN 3	A4P1-23	XA10-2
- 24	H ATTN 1	A4P1-24	XA10-1
- 25	μP MSB (B7)	P6-19	A4P1-25
- 26	μP B5	P6-20	A4P1-26
- 27	μP B3	P6-21	A4P1-27
- 28	μP B1	P6-22	A4P1-28
- A	.01-2GHZ DETECTOR IN	P35-3	A4P1-A
- B	2-18GHZ THERMISTOR	P36-1	A4P1-B
- C	2-18GHZ DETECTOR IN	P36-3	A4P1-C
- D	EXT DET IN	P37-2	A4P1-D
- E	ANALOG GND 2	A14 Ground Plane	A4P1-E
- F	EXT ALC GAIN (CW)	P39-1	A4P1-F
- H	EXT ALC GAIN (S)	P39-2	A4P1-H
- J	EXT ALC GAIN (CCW)	P39-3	A4P1-J
- K	Vacant		A4P1-K
- L	ANALOG GND 1	A14 Ground Plane	A4P1-L
- M	+15V	A0U3-3	A4P1-M
- N	-15V	A0U1-3	A4P1-N
- P	+5V RETURN	A14 Ground Plane	A4P1-P
- R	+5V	XA13-T, U, 16, 17	A4P1-R
- S	PIN MOD DRIVER	A4P1-S	XA6-7

* L = Low-Active State, H = High-Active State

Table 7-20. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
XA4 - T	FCEN/VPF	XA5-W	A4P1-T
(Cont.) - U	RF SLOPE	P7-12	A4P1-U
- V	L RF OFF	A4P1-V	XA6-5, XA7-5, XA8-5 & XA9-5
- W	L LEVEL DIP	XA2-W	A4P1-W
- X	L PIN SW OFF	A4P1-X	XA6-6, XA7-6, XA8-6 & XA9-6
- Y	Vacant		A4P1-Y
- $\underline{Z}$	L HET YIG SEL	XA6-H/XA7-H	A4P1-Z
- $\underline{A}$	H ATTN 4	A4P1-$\underline{A}$	XA10-B
- $\underline{B}$	H ATTN 2	A4P1-$\underline{B}$	XA10-$\underline{A}$
- $\underline{C}$	µP B6	P6-6	A4P1-$\underline{C}$
- $\underline{D}$	µP B4	P6-7	A4P1-$\underline{D}$
- $\underline{E}$	µP B2	P6-8	A4P1-$\underline{E}$
- F	µP LSB (BØ)	P6-9	A4P1-F
XA5 - 1	+24V	A14U2-3	A5P1-1
- 2	Vacant		A5P1-2
- 3	Vacant		A5P1-3
- 4	Vacant		A5P1-4
- 5	Vacant		A5P1-5
- 6	Vacant		A5P1-6
- 7	Vacant		A5P1-7
- 8	Vacant		A5P1-8
- 9	V/GHZ	A5P1-9	XA16-13
- 10	ANALOG GND 1	A14 Ground Plane	A5P1-10
- 11	+15V	A0U3-3	A5P1-11
- 12	-15V	A0U1-3	A5P1-12
- 13	+5V RTN	A14 Ground Plane	A5P1-13
- 14	+5V	XA13-T, U, 16, 17	A5P1-14
- 15	RAMP OUT	A5P1-15	XA3-T
- 16	RAMP INPUT	XA2-T	A5P1-16
- 17	MAN SWEEP INPUT	P7-5	A5P1-17
- 18	SP7	P7-18	A5P1-18
- 19	SP6	P7-6	A5P1-19
- 20	SP4	P7-19	A5P1-20
- 21	SP3	P7-7	A5P1-21
- 22	SP2	P7-20	A5P1-22
- 23	SP1	P7-8	A5P1-23
- 24	SP0	P7-21	A5P1-24
- 25	µP MSB (B7)	P6-19	A5P1-25
- 26	µP B5	P6-20	A5P1-26
- 27	µP B3	P6-21	A5P1-27
- 28	µP B1	P6-22	A5P1-28
- A	FC B2	XA6-Y, XA7-Y, XA8-Y or XA9-Y	A5P1-A
- B	FC B3	XA6-Z, XA7-Z XA8-$\underline{Z}$ or XA9-Z	A5P1-B
- C	FC BØ	XA6-$\underline{A}$, XA7-$\underline{A}$, XA8-$\underline{A}$ or XA9-$\underline{A}$	A5P1-C
- D	FC B1	XA6-$\underline{B}$, XA7-$\underline{B}$ XA8-$\underline{B}$ or XA9-$\underline{B}$	A5P1-D
- E	FC B4	XA6-$\underline{C}$, XA7-$\underline{C}$, XA8-$\underline{C}$ or XA9-$\underline{C}$	A5P1-E
- F	FC B5	XA6-$\underline{D}$, XA7-$\underline{D}$ XA8-$\underline{D}$ or XA9-$\underline{D}$	A5P1-F
- H	FC B6	XA6-$\underline{E}$, XA7-$\underline{E}$, XA8-$\underline{E}$ or XA9-$\underline{E}$	A5P1-H
- J	FC B7	XA6-F, XA7-F XA8-F or XA9-F	A5P1-J
- K	ΔF ≤50 MHz	A5P1-K	XA10-U
- L	ΔF ≤50 MHz RTN	A5P1-L	XA10-T
- M	+15V	A0U3-3	A5P1-M

* L = Low-Active State, H = High-Active State

Table 7-20. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.		SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
XA5	- N	-15V	A0U1-3	A5P1-N
(Cont.)	- P	+5V RTN	A14 Ground Plane	A5P1-P
	- R	+5V	XA13-T, U, 16, 17	A5P1-R
	- S	+10V REF	A5P1-S	XA6-12, XA7-12 XA8-12, XA9-12 & P7-13
	- T	CW FILTER	A5P1-T	XA6-13, XA7-13 XA8-13 & XA9-13
	- U	F CORR	A5P1-U	XA6-14, XA7-14 XA8-14 & XA9-14
	- V	Vacant		A5P1-V
	- W	FCEN/VPF	A5P1-W	XA4-T, XA6-16, XA7-16, XA8-16, XA9-16 & P7-26
	- X	ΔF >50 MHz	A5P1-X	XA6-17, XA7-17, XA8-17 & XA9-17
	- Y	ANALOG GND 3	A5P1-Y	XA6-18, XA7-18, XA8-18 & XA9-18
	- Z	FCEN SIG GND	A5P1-Z	XA6-18, XA7-18, XA8-18 & XA9-18
	- $\overline{A}$	F CEN	A5P1-$\overline{A}$	XA6-19, XA7-19, XA8-19 & XA9-19
	- $\overline{B}$	ANALOG GND 2	A14 Ground Plane	A5P1-$\overline{B}$
	- $\overline{C}$	µP B6	P6-6	A5P1-$\overline{C}$
	- $\overline{D}$	µP B4	P6-7	A5P1-$\overline{D}$
	- $\overline{E}$	µP B2	P6-8	A5P1-$\overline{E}$
	- $\overline{F}$	µP LSB (BØ)	P6-9	A5P1-$\overline{F}$
XA6	- 1	+12/-24V	XA13-W, 19	A6P1-1
	- 2	L HET PIN SEL	A6P1-2	A14CR17-Cathode XA7-2
	- 3	Vacant		A6P1-3
	- 4	Vacant		A6P1-4
	- 5	L RF OFF	XA4-V	A6P1-5
	- 6	L PIN SW OFF	XA4-X	A6P1-6
	- 7	PIN MOD DRIVER	XA4-S	A6P1-7
	- 8	+15V	A0U3-3	A6P1-8
	- 9	-15V	A0U1-3	A6P1-9
	- 10	+5V RETURN	A14 Ground Plane	A6P1-10
	- 11	+5V	XA13-T, U, 16, 17	A6P1-11
	- 12	+10V REF	XA5-S	A6P1-12
	- 13	CW FILTER	XA5-T	A6P1-13
	- 14	F CORR	XA5-U	A6P1-14
	- 15	RF DECK GND	A14 Ground Plane	A6P1-15
	- 16	FCEN/VPF	XA5-W	A6P1-16
	- 17	ΔF >50 MHz	XA5-X	A6P1-17
	- 18	F CEN SIG GND	XA5-Z	A6P1-18
	- 19	F CEN	XA5-$\overline{A}$	A6P1-19
	- 20	ANALOG GND 1	A14 Ground Plane	A6P1-20
	- 21	ROM B7 (MSB)	A14U6-19	A6P1-21
	- 22	ROM B6	A14U6-16	A6P1-22
	- 23	ROM B5	A14U6-15	A6P1-23
	- 24	ROM B4	A14U6-12	A6P1-24
	- 25	ROM B3	A14U6-9	A6P1-25
	- 26	ROM B2	A14U6-6	A6P1-26
	- 27	ROM B1	A14U6-5	A6P1-27
	- 28	ROM B0 (LSB)	A14U6-2	A6P1-28
	- A	L PIN SELECT 1	A6P1-A	XA4-5 & A14CR18-Cathode
	- B	+18V UNREG	XA3-$\overline{D}$, 26	A6P1-B
	- C	H SNB 1	A6P1-C	XA7-3
	- D	H SNR 1	A6P1-D	XA7-4 & A14U7-13

* L = Low-Active State, H = High-Active State

Table 7-20. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.		SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
XA6 (Cont.)	- E	L YIG 1 FM COIL SEL	A6P1-E	XA10-$\overline{F}$ & A14U7-3
	- F	TRACK FILTER 1	A6P1-F	XA10-$\overline{E}$
	- H	L HET YIG SEL	A6P1-H	XA7-H & XA10-26
	- J	Vacant		
	- K	MOD DRIVER 1	A6P1-K	P14-1
	- L	+5V RETURN	A14 Ground Plane	A6P1-L
	- M	+5V	XA13-T, U, 16, 17	A6P1-M
	- N	YIG 1 BIAS GND SENSE	A6P1-N	P14-2
	- P	A6Q1-E	A6P1-P	P18-1
	- R	A6Q1-C	A6P1-R	P18-2
	- S	A6Q1-B	A6P1-S	P18-3
	- T	YIG 1 COIL (+)	A6P1-T	P14-6
	- U	YIG 1 COIL (-)	A6P1-U	P19-2
	- V	YIG 1 TUNE CONTROL	A6P1-V	P19-3
	- W	YIG 1 TUNE SUPPLY	A6P1-W	P20-3
	- X	ANALOG GND 1	A14 Ground Plane	A6P1-X
	- Y	FC B2	A6P1-Y	XA5-A
	- $\underline{Z}$	FC B3	A6P1-$\underline{Z}$	XA5-B
	- $\underline{A}$	FC BØ (LSB)	A6P1-$\underline{A}$	XA5-C
	- $\underline{B}$	FC B1	A6P1-$\underline{B}$	XA5-D
	- $\underline{C}$	FC B4	A6P1-$\underline{C}$	XA5-E
	- $\underline{D}$	FC B5	A6P1-$\underline{D}$	XA5-F
	- $\underline{E}$	FC B6	A6P1-$\underline{E}$	XA5-H
	- $\underline{F}$	FC B7 (MSB)	A6P1-$\underline{F}$	XA5-J
XA7	- 1	+12/-24V	XA13-W, 19	A7P1-1
	- 2	L HET PIN SEL	XA6-2	A7P1-2
	- 3	H SNB 1	XA6-C	A7P1-3
	- 4	H SNR 1	XA6-D	A7P1-4
	- 5	L RF OFF	XA4-V	A7P1-5
	- 6	L PIN SW OFF	XA4-X	A7P1-6
	- 7	PIN MOD DRIVER	XA4-S	A7P1-7
	- 8	+15V	A0U3-3	A7P1-8
	- 9	-15V	A0U1-3	A7P1-9
	- 10	+5V RETURN	A14 Ground Plane	A7P1-10
	- 11	+5V	XA13-T, U, 16, 17	A7P1-11
	- 12	+10V REF	XA5-S	A7P1-12
	- 13	CW FILTER	XA5-T	A7P1-13
	- 14	F CORR	XA5-U	A7P1-14
	- 15	RF DECK GND	A14 Ground Plane	A7P1-15
	- 16	FCEN/VPF	XA5-W	A7P1-16
	- 17	ΔF >50 MHz	XA5-X	A7P1-17
	- 18	F CEN SIG GND	XA5-$\underline{Z}$	A7P1-18
	- 19	F CEN	XA5-$\overline{A}$	A7P1-19
	- 20	ANALOG GND 1	A14 Ground Plane	A7P1-20
	- 21	ROM B7 (MSB)	A14U6-19	A7P1-21
	- 22	ROM B6	A14U6-16	A7P1-22
	- 23	ROM B5	A14U6-15	A7P1-23
	- 24	ROM B4	A14U6-12	A7P1-24
	- 25	ROM B3	A14U6-9	A7P1-25
	- 26	ROM B2	A14U6-6	A7P1-26
	- 27	ROM B1	A14U6-5	A7P1-27
	- 28	ROM B0 (LSB)	A14U6-2	A7P1-28
	- A	PIN SELECT 2	A7P1-A	A14CR20-Cathode
	- B	+18V UNREG	XA13-$\overline{D}$, 26	A7P1-B
	- C	H SNB 2	A7P1-C	XA8-3
	- D	H SNR 2	A7P1-D	XA8-4 & A14U7-14
	- E	L YIG 2 FM COIL SEL	A7P1-E	XA10-28 & A14U7-4
	- F	TRACK FILTER 2	A7P1-F	XA10-27

* L = Low-Active State, H = High-Active State

Table 7-20. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
XA7 - H	L HET YIG SEL	A6P1-H	XA7-H
(Cont.) - J	Vacant		A7P1-J
- K	MOD DRIVER 2	A7P1-K	P13-1
- L	+5V RETURN	A14 Ground Plane	A7P1-L
- M	+5V	XA13-T, U, 16, 17	A7P1-M
- N	YIG 2 BIAS GND SENSE	A7P1-N	P13-2
- P	A7Q1-E	A7P1-P	P21-1
- R	A7Q1-C	A7P1-R	P21-2
- S	A7Q1-B	A7P1-S	P21-3
- T	YIG 2 COIL (+)	A7P1-T	P13-6
- U	YIG 2 COIL (-)	A7P1-U	P22-2
- V	YIG 2 TUNE CONTROL	A7P1-V	P22-3
- W	YIG 2 TUNE SUPPLY	A7P1-W	P23-3
- X	ANALOG GND 1	A14 Ground Plane	A7P1-X
- Y	FC B2	A7P1-Y	XA5-A
- Z	FC B3	A7P1-Z	XA5-B
- A	FC BØ (LSB)	A7P1-A	XA5-C
- B	FC B1	A7P1-B	XA5-D
- C	FC B4	A7P1-C	XA5-E
- D	FC B5	A7P1-D	XA5-F
- E	FC B6	A7P1-E	XA5-H
- F	FC B7 (MSB)	A7P1-F	XA5-J
XA8 - 1	+12V/-24V	XA13-W, 19	A8P1-1
- 2	Vacant		A8P1-2
- 3	H SNB 2	XA7-C	A8P1-3
- 4	H SNR 2	XA7-D	A8P1-4
- 5	L RF OFF	XA4-V	A8P1-5
- 6	L PIN SW OFF	XA4-X	A8P1-6
- 7	PIN MOD DRIVER	XA4-S	A8P1-7
- 8	+15V	A0U3-3	A8P1-8
- 9	-15V	A0U1-3	A8P1-9
- 10	+5V RETURN	A14 Ground Plane	A8P1-10
- 11	+5V	XA13-T, U, 16, 17	A8P1-11
- 12	+10V REF	XA5-S	A8P1-12
- 13	CW FILTER	XA5-T	A8P1-13
- 14	F CORR	AX5-U	A8P1-14
- 15	Vacant		A8P1-15
- 16	FCEN/VPF	XA5-W	A8P1-16
- 17	ΔF >50 MHz	XA5-X	A8P1-17
- 18	F CEN SIG GND	XA5-Z	A8P1-18
- 19	F CEN	XA5-A	A8P1-19
- 20	ANALOG GND 1	A14 Ground Plane	A8P1-20
- 21	ROM B7 (MSB)	A14U6-19	A8P1-21
- 22	ROM B6	A14U6-16	A8P1-22
- 23	ROM B5	A14U6-15	A8P1-23
- 24	ROM B4	A14U6-12	A8P1-24
- 25	ROM B3	A14U6-9	A8P1-25
- 26	ROM B2	A14U6-6	A8P1-26
- 27	ROM B1	A14U6-5	A8P1-27
- 28	ROM B0 (LSB)	A14U6-2	A8P1-28
- A	PIN SELECT 3	A8P1-A	A14CR22-Cathode
- B	+18V UNREG	XA13-D, 26	A8P1-B
- C	H SNB 3	A8P1-C	XA9-3
- D	H SNR 3	A8P1-D	XA9-4 & A14U7-17
- E	L YIG 3 FM COIL SEL	A8P1-E	XA10-M & A14U7-7
- F	Vacant		A8P1-F
- H	Vacant		A8P1-H
- J	Vacant		A8P1-J
- K	MOD DRIVER 3	A8P1-K	P14-1

* L = Low-Active State, H = High-Active State

Table 7-20. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
XA8 - L	+5V RETURN	A14 Ground Plane	A6P1-L
(Cont.) - M	+5V	XA13-T, U, 16, 17	A6P1-M
- N	YIG 3 BIAS GND SENSE	A8P1-N	P17-2
- P	A8Q1-E	A8P1-P	P28-1
- R	A8Q1-C	A8P1-R	P28-2
- S	A8Q1-B	A8P1-S	P28-3
- T	YIG 3 COIL (+)	A8P1-T	P17-6
- U	YIG 3 COIL (-)	A8P1-U	P29-2
- V	YIG 3 TUNE CONTROL	A8P1-V	P29-3
- W	YIG 3 TUNE SUPPLY	A8P1-W	P30-3
- X	ANALOG GND 1	A14 Ground Plane	A8P1-X
- Y	FC B2	A8P1-Y	XA5-A
- Z	FC B3	A8P1-Z	XA5-B
- $\bar{A}$	FC BØ (LSB)	A8P1-$\bar{A}$	XA5-C
- $\bar{B}$	FC B1	A8P1-$\bar{B}$	XA5-D
- $\bar{C}$	FC B4	A8P1-$\bar{C}$	XA5-E
- $\bar{D}$	FC B5	A8P1-$\bar{D}$	XA5-F
- $\bar{E}$	FC B6	A8P1-$\bar{E}$	XA5-H
- $\bar{F}$	FC B7 (MSB)	A8P1-$\bar{F}$	XA5-J
XA9 - 1	+12/-24V	XA13-$\bar{W}$, 19	A9P1-1
- 2	+18V UNREG	XA13-$\bar{D}$, 26	A9P1-2
- 3	H SNB 3	XA8-C	A9P1-3
- 4	H SNR 3	XA8-D	A9P1-4
- 5	L RF OFF	XA4-V	A9P1-5
- 6	L PIN SW OFF	XA4-X	A9P1-6
- 7	PIN MOD DRIVER	XA4-S	A9P1-7
- 8	+15V	A0U3-3	A9P1-8
- 9	-15V	A0U1-3	A9P1-9
- 10	+5V RETURN	A14 Ground Plane	A9P1-10
- 11	+5V	XA13-T, U, 16, 17	A9P1-11
- 12	+10V REF	XA5-S	A9P1-12
- 13	CW FILTER	XA5-T	A9P1-13
- 14	F CORR	XA5-U	A9P1-14
- 15	Vacant		A9P1-15
- 16	FCEN/VPF	XA5-W	A9P1-16
- 17	ΔF >50 MHz	XA5-X	A9P1-17
- 18	F CEN SIG GND	XA5-Z	A9P1-18
- 19	F CEN	XA5-$\bar{A}$	A9P1-19
- 20	ANALOG GND 1	A14 Ground Plane	A9P1-20
- 21	ROM B7 (MSB)	A14U6-19	A9P1-21
- 22	ROM B6	A14U6-16	A9P1-22
- 23	ROM B5	A14U6-15	A9P1-23
- 24	ROM B4	A14U6-12	A9P1-24
- 25	ROM B3	A14U6-9	A9P1-25
- 26	ROM B2	A14U6-6	A9P1-26
- 27	ROM B1	A14U6-5	A9P1-27
- 28	ROM B0 (LSB)	A14U6-2	A9P1-28
- A	PIN SELECT 4	A9P1-A	A14CR24-Cathode
- B	+18V UNREG	A14R31	A9P1-B
- C	Vacant		A9P1-C
- D	H SNR 4	A9P1-D	A14U7-18
- E	YIG 4 FM COIL SEL	A9P1-E	XA10-L & A14U7-8
- F	Vacant		A9P1-F
- H	Vacant		A9P1-H
- J	Vacant		A9P1-J
- K	MOD DRIVER 4	A9P1-K	P16-1
- L	+5V RETURN	A14 Ground Plane	A9P1-L
- M	+5V	XA13-T, U, 16, 17	A9P1-M
- N	YIG 4 BIAS GND SENSE	A9P1-N	P16-2

* L = Low-Active State, H = High-Active State

Table 7-20. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
XA9 - P	A9Q1-E	A9P1-P	P25-1
(Cont.) - R	A9Q1-C	A9P1-R	P25-2
- S	A9Q1-B	A9P1-S	P25-3
- T	YIG 4 COIL (+)	A9P1-T	P16-6
- U	YIG 4 COIL (-)	A9P1-U	P26-2
- V	YIG 4 TUNE CONTROL	A9P1-V	P26-3
- W	YIG 4 TUNE SUPPLY	A9P1-W	P27-3
- X	ANALOG GND 1	A14 Ground Plane	A9P1-X
- Y	FC B2	A9P1-Y	XA5-A
- Z	FC B3	A9P1-Z	XA5-B
- $\overline{A}$	FC B∅ (LSB)	A9P1-$\overline{A}$	XA5-C
- $\overline{B}$	FC B1	A9P1-$\overline{B}$	XA5-D
- $\overline{C}$	FC B4	A9P1-$\overline{C}$	XA5-E
- $\overline{D}$	FC B5	A9P1-$\overline{D}$	XA5-F
- $\overline{E}$	FC B6	A9P1-$\overline{E}$	XA5-H
- $\overline{F}$	FC B7 (MSB)	A9P1-$\overline{F}$	XA5-J
XA10 - 1	H ATTN 1	XA4-24	A10P1-1
- 2	H ATTN 3	XA4-23	A10P1-2
- 3	Vacant		A10P1-3
- 4	Vacant		A10P1-4
- 5	H EXT FM ENABLE	XA2-Y	A10P1-5
- 6	+5V	XA13-T, U, 16, 17	A10P1-6
- 7	+5V RTN	A14 Ground Plane	A10P1-7
- 8	H 20DB ATTN DRVR (BLACK)	A10P1-8	P31-8
- 9	L 20DB ATTN DRVR (GREEN)	A10P1-9	P31-7
- 10	HA 40DB ATTN DRVR (ORANGE)	A10P1-10	P31-6
- 11	LA 40DB ATTN DRVR (BLUE)	A10P1-11	P31-5
- 12	HB 40DB ATTN DRVR (BROWN)	A10P1-12	P31-4
- 13	LB 40DB ATTN DRVR (WHITE)	A10P1-13	P31-3
- 14	H 10DB ATTN DRVR (PURPLE)	A10P1-14	P31-2
- 15	L 10DB ATTN DRVR (YELLOW)	A10P1-15	P31-1
- 16	TRACK FILTER COIL (RTN)	P16-8	A10P1-16
- 17	FM COIL, WJ (RTN)	P16-10	A10P1-17
- 18	FM COIL, AVANTEK (RTN)	P16-12	A10P1-18
- 19	Vacant		A10P1-19
- 20	FM COIL, AVANTEK (SOURCE)	A10P1-20	P14-13
- 21	FM COIL, WJ (SOURCE)	A10P1-21	P14-11
- 22	TRACK FILTER COIL (SOURCE)	A10P1-22	P14-9
- 23	-15V HC	A0U1-3	A10P1-23
- 24	+15V HC	A0U3-3	A10P-24
- 25	ANALOG GND 1	A14 Ground Plane	A10P1-25
- 26	L HET YIG SEL	XA7-H	A10P1-26
- 27	TRACK FILTER 2	XA7-F	A10P1-27
- 28	YIG 2 FM COIL SEL	XA7-E	A10P1-28
- A	H ATTN 2	XA4-$\overline{B}$	A10P1-A
- B	H ATTN 4	XA4-$\overline{A}$	A10P1-B
- C	Vacant		A10P1-C
- D	H FM DIAG	A10P1-D	A14U8-13
- E	L EOB	A10P1-E	XA2-Z
- F	+5V	XA13-T, U, 16, 17	A10P1-F
- H	+5V RTN	A14 Ground Plane	A10P1-H
- J	Vacant		A10P1-J
- K	Vacant		A10P1-K
- L	L YIG 4 FM COIL SEL	XA9-E	A10P1-L
- M	L YIG 3 FM COIL SEL	XA8-E	A10P1-M
- N	Vacant		A10P1-N
- P	Vacant		A10P1-P
- R	Vacant		A10P1-R
- S	EXT FM INPUT	P34-1	A10P1-S
- T	$\Delta F \leq 50$ MHz RTN	XA5-L	A10P1-T

* L = Low-Active State, H = High-Active State

Table 7-20. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
XA10 - U	ΔF ≤50 MHz	XA5-K	A10P1-U
(Cont.) - V	EXT FM RTN	P34-2	A10P1-V
- W - X	Vacant		
- Y	Spare		A10P1-Y
- Z	Spare		A10P1-Z
- $\overline{A}$	+15V HC	A0U4-3	A10P1-$\overline{A}$
- $\overline{B}$	-15V HC	A0U2-3	A10P1-$\overline{B}$
- $\overline{C}$	ANALOG GND 1	A14 Ground Plane	A10P1-$\overline{C}$
- $\overline{D}$	Vacant		A10P1-$\overline{D}$
- $\overline{E}$	TRACK FILTER 1	XA6-F	A10P1-$\overline{E}$
- $\overline{F}$	L YIG 1 FM COIL SEL	XA6-E	A10P1-$\overline{F}$
XA13 - 1	-165	CR12(-)	A13P1-1
- 2	165V RTN	A14P1-7	A13P1-2
- 3	+165V	A14R16	A13P1-3
- 4	Vacant		
- 5	SHUT DOWN LED	A14DS2-2	A13P1-5
- 6	OVER VOLTAGE/CURRENT	A14Q4-Collector, A14U1-5	A13P1-6
- 7	+12V RTN	A14CR9-Anode, A14CR6-Anode	A13P1-7
- 8	+12V	A14CR7-Cathode, A14CR8-Cathode	A13P1-8
- 9	Vacant		
- 10	Vacant		
- 11 - 12	+5V RTN	A14 Ground Plane	A13P1-11 A13P1-12
- 13	DIGITAL GND SENSE	A14 Ground Plane	A13P1-13
- 14	EARTH GND	A14P1-2	A13P1-14
- 15	EARTH GND	A14P1-2	A13P1-15
- 16 - 17	+5V SOURCE	A13P1-16 A13P1-17	Analog & Digital Circuits
- 18	+12V/-24V RTN	A14 Ground Plane	A13P1-18
- 19	+12V/-24V	A13P1-19	XA6-XA9, Pin 1
- 20	+28V RTN	A14 Ground Plane	A13P1-20
- 21	+28V	A13P1-21	P13-P17, Pin 4
- 22 - 23	-18V	A13P1-22 A13P1-23	A13P2-4 & A0U1-1
- 24 - 25	18V RTN (ANALOG GND)	A14 Ground Plane	A13P1-24 A13P1-25
- 26	+18V	A13P1-26	A14R13, A0U3-1, A0U4-1
- 27	-43V RTN	A14 Ground Plane	A13P1-27
- 28	-43V	A13P1-28	A0Q1-Base, A14CR1-Anode
- A	-165V	CR12(-)	A13P1-A
- B	165V RTN	A14P1-7	A13P1-B
- C	+165V	A14R16	A13P1-3
- D	Vacant		
- E	SHUT DOWN LED	A14DS2-2	A13P1-E
- F	OVER VOLTAGE/CURRENT	A14Q4-Collector, A14U1-5	A13P1-F
- H	+12V RTN	A14CR9-Anode, A14CR6-Anode	A13P1-H
- J	+12V	A14CR7-Cathode, A14CR8-Cathode	A13P1-8
- K			
- L	Vacant		
- M - N	+5V RTN	A14 Ground Plane	A13P1-M A13P1-N
- P	+5V SENSE	Analog & Digital Circuits	A13P1-P

* L = Low-Active State, H = High-Active State

Table 7-20. Motherboard Wire List Connector Order (Continued)

CONNECTOR & PIN NO.	SIGNAL MNEMONIC*	FROM (CONN. & PIN NO.)	TO (CONN. & PIN NO.)
XA13 - R (Cont.) - S	EARTH GROUND	A14P1-2	A13P1-R, A13P1-S
- T, - U	+5V SOURCE	A13P1-T, A13P1-U	Analog & Digital Circuits
- V	+12V/-24V RTN	A14 Ground Plane	A13P1-V
- W	+12V/-24V	A13P1-W	XA6-XA9, Pin 1
- X	+28V RTN	A14 Ground Plane	A13P1-X
- Y	+28V	A13P1-Y	P13-P17, Pin 4
- $\overline{Z}$, - $\overline{A}$	-18V	A3P1-$\overline{Z}$, A3P1-$\overline{A}$	A13P2-4, A0U1-1
- $\overline{B}$	18V RTN	A14 Ground Plane	A13P1-$\overline{B}$
- $\overline{C}$	(ANALOG GROUND)	A14 Ground Plane	A13P1-$\overline{C}$
- $\overline{D}$	+18V	A13P1-$\overline{D}$	A14R13, A0U3-1, A0U4-1
- $\overline{E}$	-43V RTN	A14 Ground Plane	A13P1-$\overline{E}$
- F	-43V	A13P1-28	A0Q1-Base, A14CR1-Anode
XA16 - 1	EXT RAMP IN	EXT SWEEP (Rear Panel Connector)	XA2-B
- 2	ACTIVATE RELAY Return	A14 Ground Plane	PENLIFT OUTPUT Shield
- 3	EXT DWELL	SWEEP DWELL INPUT (Rear Panel Connector)	XA2-D
- 4	EXT TRIGGER PULSE IN	SWEEP TRIGGER INPUT (Rear Panel Connector)	XA2-E
- 5	BANDSWITCH BLANKING +	XA2-2	BANDSWITCH BLANKING +, - Switch
- 6	HORIZ OUTPUT DURING CW	HORIZ OUTPUT DURING CW ON/OFF Switch	U10-17
- 7	SEQ SYNC	XA2-6	SEQ SYNC OUTPUT (Rear Panel Connector)
- 8	VIDEO MARKER	XA3-8	MARKER OUTPUT (Rear Panel Connector)
- 9	RETRACE BLANKING +	XA2-5	RETRACE BLANKING OUTPUT + (Rear Panel Connector)
- 10	HORIZONTAL OUTPUT	XA3-J	HORIZ OUTPUT (Rear Panel Connector)
- 11	+5V RETURN	XA16-11	HORIZ OUTPUT DURING CW ON/OFF Switch
- 12	BANDSWITCH BLANKING -	XA2-3	BANDSWITCH BLANKING +, - Switch
- 13	V/GHZ	XA5-9	1V/GHz Output (Rear Panel Connector)
- 14	RETRACE BLANKING -	XA2-3	RETRACE BLANKING OUTPUT (Rear Panel Connector)
- 15	ACTIVATE RELAY	XA1-H	PENLIFT OUTPUT (Rear Panel Connector)
- 16	Vacant		

* L = Low-Active State, H = High-Active State

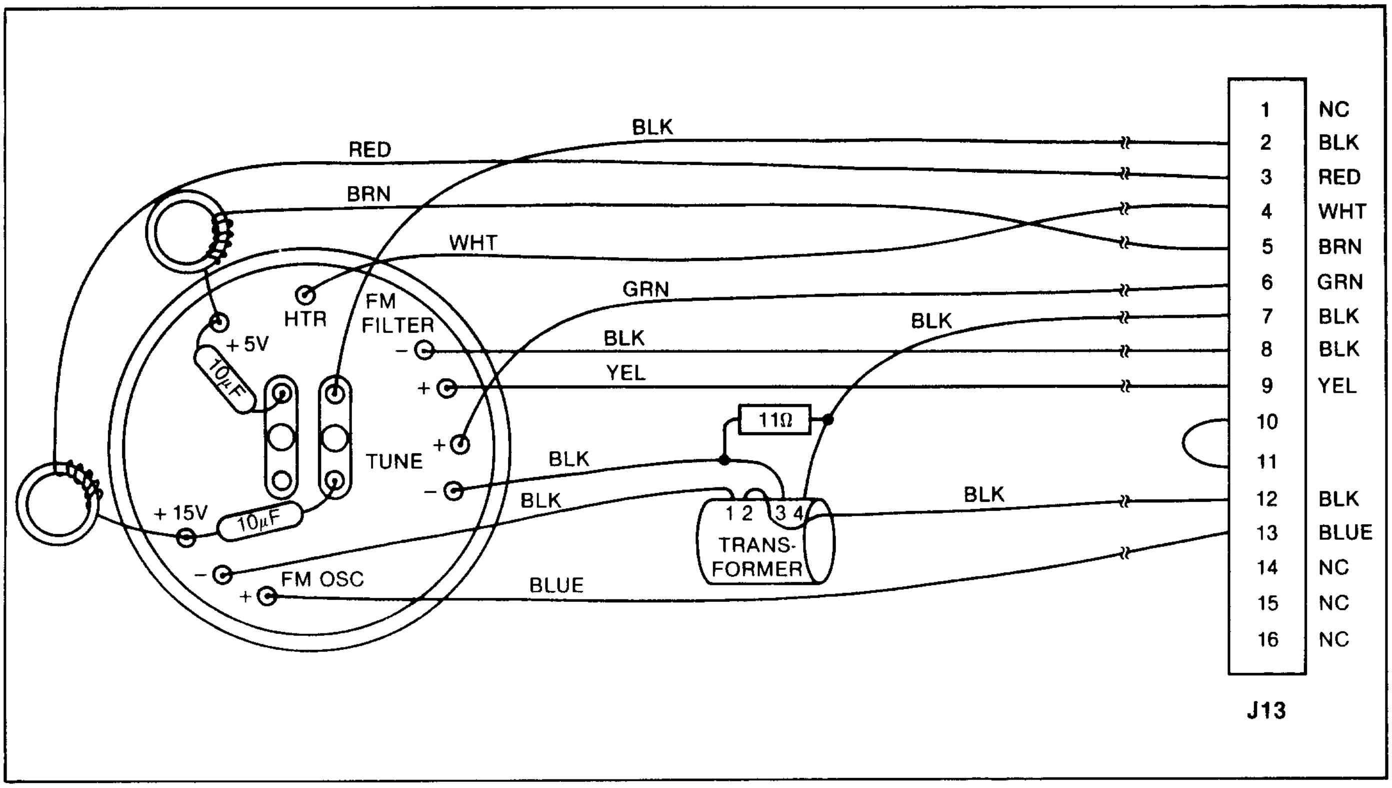


Figure 7-83. Osc 1 Avantek YIG Wiring Diagram

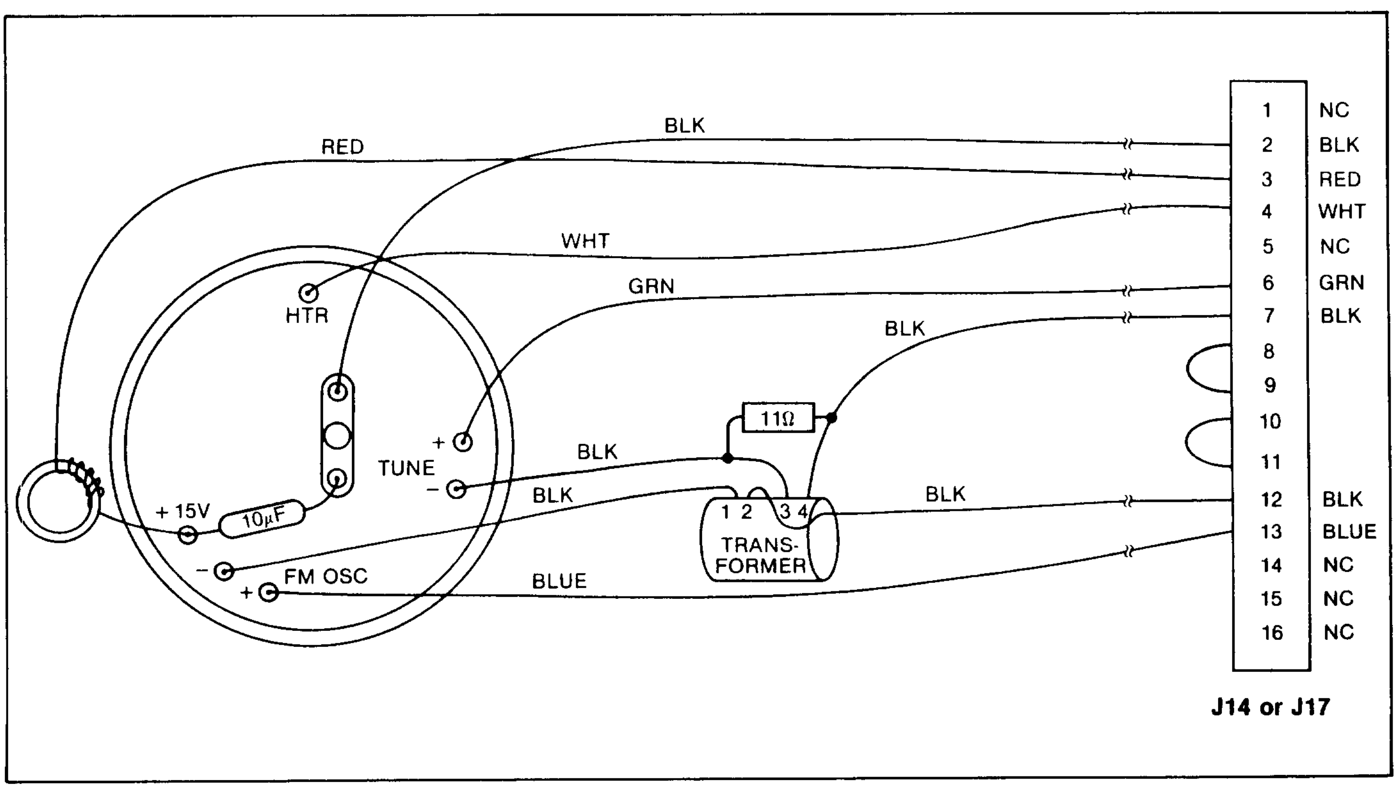


Figure 7-84. Osc 2 and 3 Avantek YIG Wiring Diagram

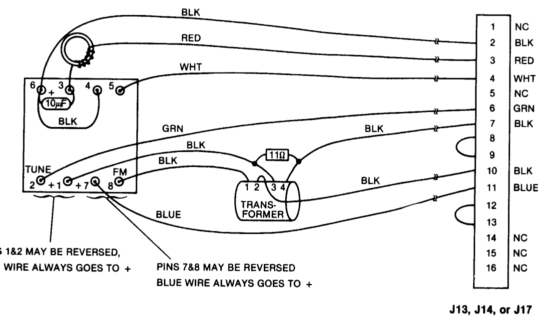


Figure 7-85. Osc 2 and 3 Watkins-Johnson
YIG Wiring Diagram

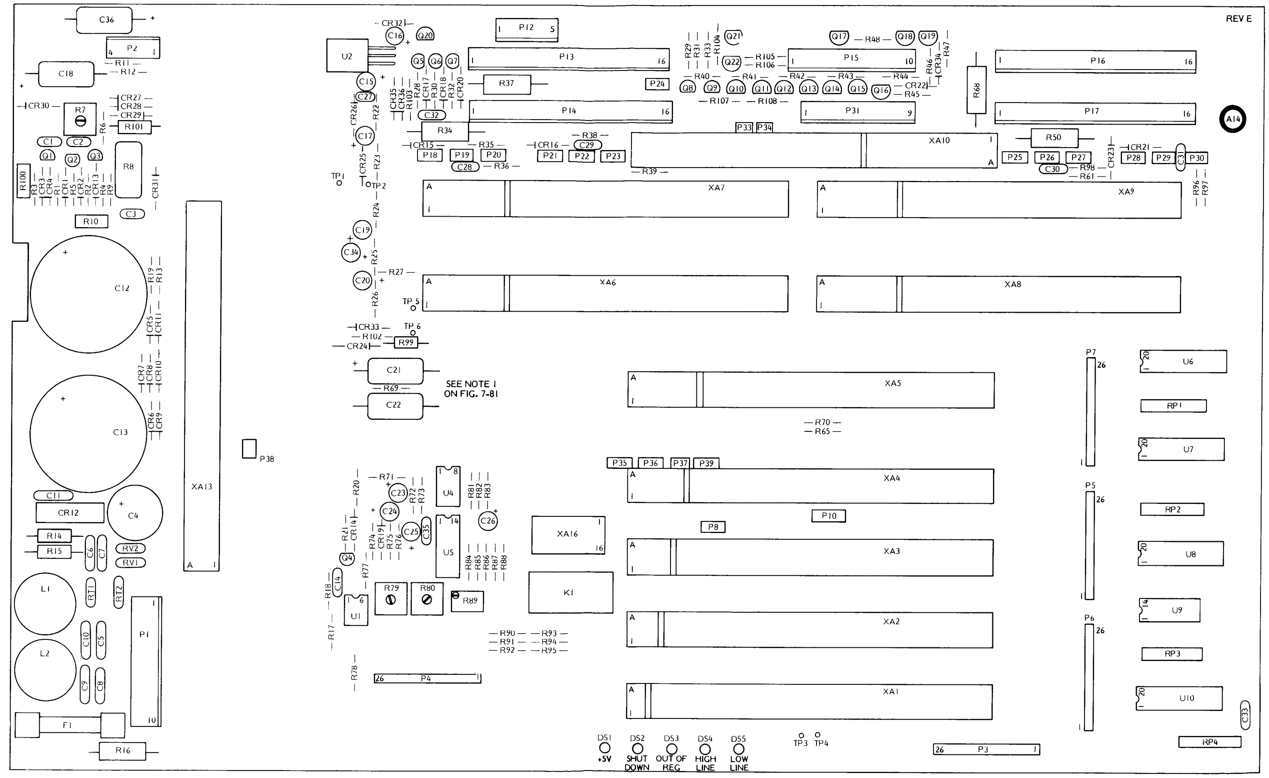


Figure 7-86. A14 Motherboard PCB
Parts Locator Diagram

Figure 7-85.

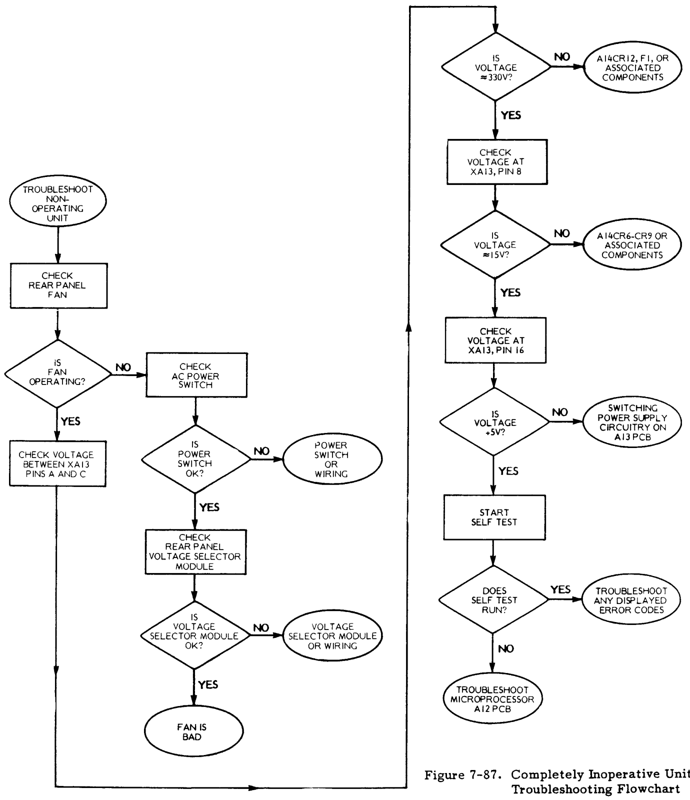


Figure 7-87. Completely Inoperative Unit Troubleshooting Flowchart

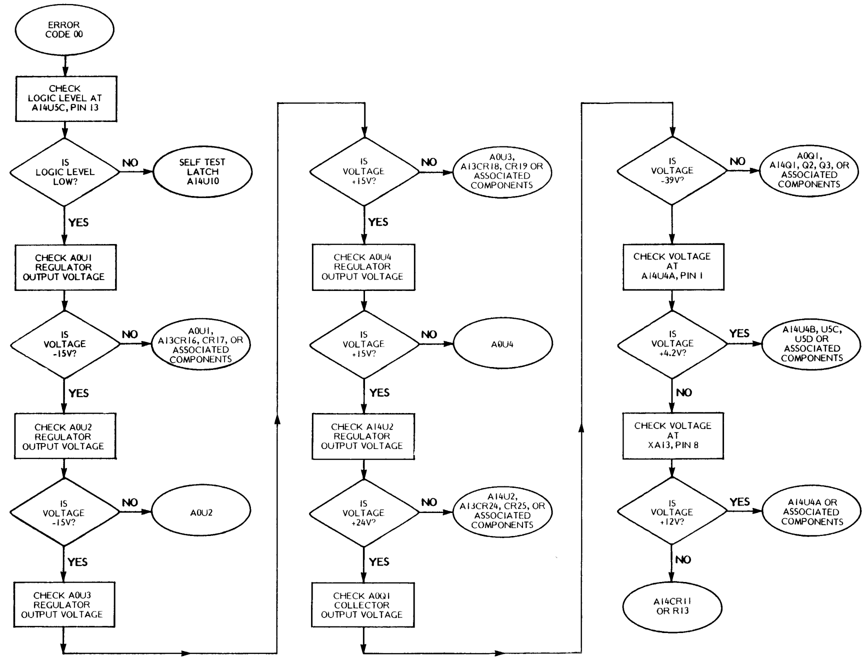


Figure 7-88. Error Code 00 Troubleshooting Flowchart

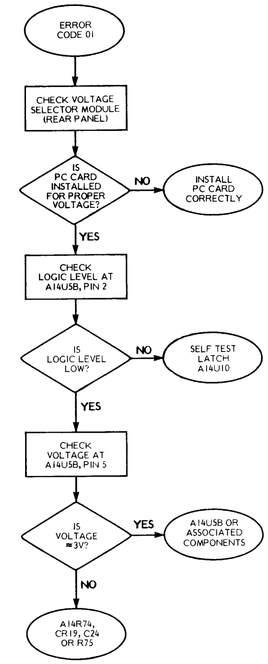


Figure 7-89. Error Code 01 Troubleshooting Flowchart

Figure 7-87.
Figure 7-88.

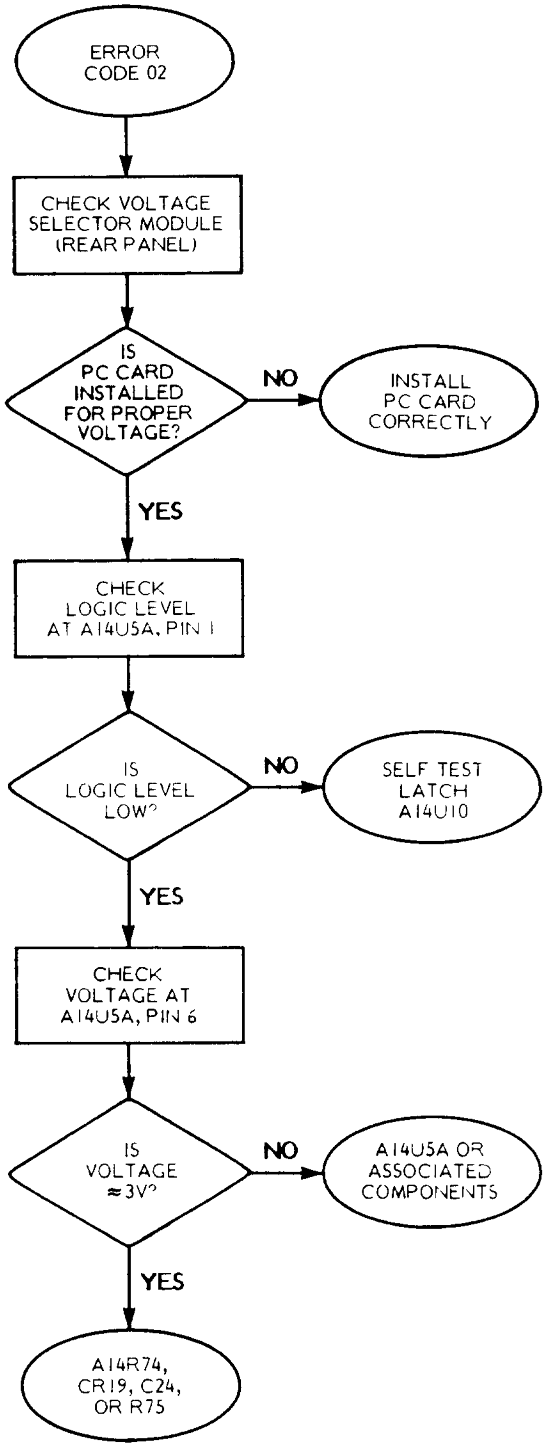


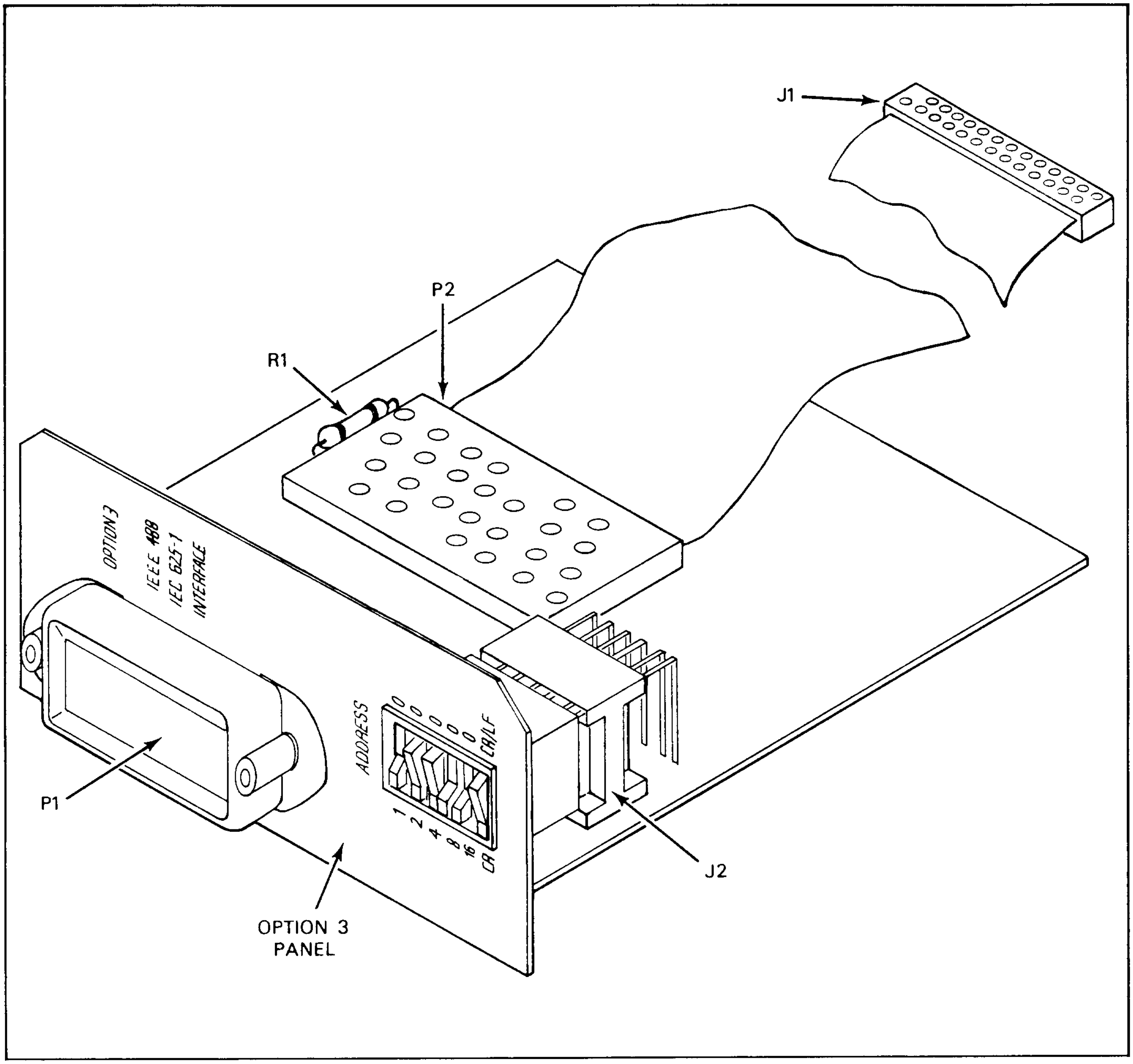
Figure 7-90. Error Code 02 Troubleshooting Flowchart

7-15.3 A13/A14 Switching Power Supply Troubleshooting Information and Data

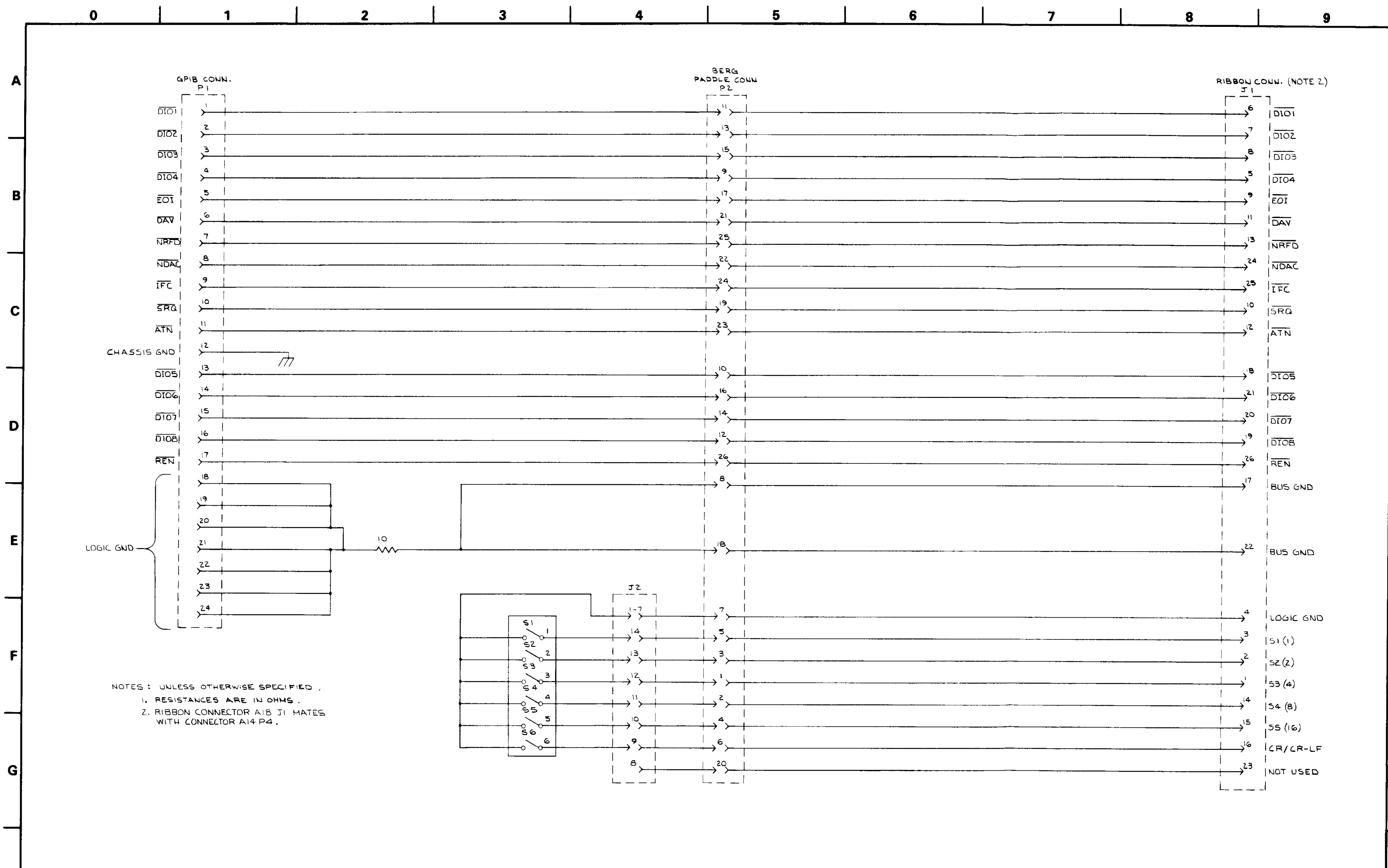
Error Codes 00, 01, and 02 report on the status of the A13/A14 Switching Power Supply circuits. The microprocessor routines associated with these error codes test the power supply for out-of-regulation voltages, and for high-and low-line-voltage conditions. Figures 7-87 through 7-90 provide flowcharts for troubleshooting the switching power supply.

7-16 A18 GPIB CONNECTOR PCB CIRCUIT DESCRIPTION

The A18 GPIB Connector PCB is the connecting plane for the rear panel GPIB connector. The schematic for this PCB is provided in Figure 7-91.



A18 GPIB Parts Locator Diagram



NOTES: UNLESS OTHERWISE SPECIFIED.
1. RESISTANCES ARE IN OHMS.
2. RIBBON CONNECTOR A18 J1 MATES WITH CONNECTOR A14 P4.

Figure 7-91. A18 GPIB Connector PCB Schematic

APPENDIX 1

QUICK REFERENCE DATA

Command Code Index

MNEMONIC	NAME	TABLE NO.
AUT	Auto Trigger	3-7
CFØ	CW Select FØ	3-7
CF1	CW Select F1	3-7
CF2	CW Select F2	3-7
CLR	Clear Keypad	3-7
CM1	CW Select M1	3-7
CM2	CW Select M2	3-7
CNT	Continue Sweep	3-12
CS0	Horizontal Output Off During CW Operation	3-12
CS1	Horizontal Output On During CW Operation	3-12
DB	dB Data Terminator	3-7
DFØ	Sweep Range ΔF F0	3-7
DF1	Sweep Range ΔF F1	3-7
DL1	Detector Leveling	3-7
DLF	Enter ΔF Frequency	3-7
DM	dBm Data Terminator	3-7
DN	Decrement Selected Parameter	3-12
DSØ	Front Panel Displays Off	3-12
DS1	Front Panel Displays On	3-12
DWØ	Dwell at Marker Mode Off	3-10
DW1	Dwell at Marker Mode On	3-10
ESØ	End of Sweep Mode Off	3-10
ES1	End of Sweep Mode On	3-10
EXT	External Trigger	3-7
FØ	Enter Parameter FØ	3-7
F1	Enter Parameter F1	3-7
F2	Enter Parameter F2	3-7
FF	Sweep Range F1-F2	3-7
FLØ	CW Filter Off	3-12
FL1	CW Filter On	3-12
FMØ	Frequency Modulation Off	3-7
FM1	Frequency Modulation On	3-7
FUL	Sweep Range Full	3-7
FVØ	Frequency Vernier Off	3-7
FVS	Set Frequency Vernier	3-7
GH	GHz Data Terminator	3-7
GTD	GET* Mode Execute "DN" Command	3-9
GTN	GET Mode Execute "N" Command	3-9
GTS	GET Mode Trigger Sweep	3-9
GTU	GET Mode Execute "UP" Command	3-9
IL1	Internal Leveling	3-7
IM1	Intensity Marker	3-7
LIN	Line Trigger	3-7
LVØ	Leveling Off	3-7
LVL	Enter Level Parameter	3-7
M1	Enter M1 Parameter	3-7
M2	Enter M2 Parameter	3-7
MAN	Manual Sweep	3-7
MH	MHz Data Terminator	3-7

MNEMONIC	NAME	TABLE NO.
MKØ	Markers Off	3-7
MM	Sweep Range M1-M2	3-7
MS	Millisecond Data Terminator	3-7
N	Go to Next Increment (Digital Sweep)	3-8
ODF	Output ΔF Frequency	3-11
OI	Identify Instrument	3-11
OFØ	Output FØ Frequency	3-11
OF1	Output F1 Frequency	3-11
OF2	Output F2 Frequency	3-11
OFL	Output Low-End Frequency	3-11
OFH	Output High-End Frequency	3-11
OLV	Output RF Level	3-11
OM1	Output M1 Frequency	3-11
OM2	Output M2 Frequency	3-11
OSB	Output Status Byte	3-11
OST	Output Sweep Time	3-11
PEØ	Parameter Entry Error Mode Off	3-10
PE1	Parameter Entry Error Mode On	3-10
PL1	Power Meter Leveling	3-7
RCL	Recall Front Panel Setup	3-12
RFØ	RF Off	3-7
RF1	RF On	3-7
RL	Return to Local	3-12
RM1	RF Marker On	3-7
RSS	Reset Sweep	3-12
RST	Reset Front Panel	3-7
RTØ	RF During Retrace Off	3-7
RT1	RF During Retrace On	3-7
SAV	Save Front Panel Setup	3-12
SEØ	Syntax Error Mode Off	3-10
SE1	Syntax Error Mode On	3-10
SEC	Seconds Data Terminator	3-7
SH	Shift	3-7
SIZ	Increment Size	3-8
SQØ	SRQ Mode Off	3-10
SQ1	SRQ Mode On	3-10
STP	Step Sweep	3-8
STS	Step Select	3-8
SWT	Enter Sweep Time Parameter	3-7
TRS	Trigger Sweep	3-7
TST	Self Test	3-7
ULØ	Unleveled Condition Mode Off	3-10
UL1	Unleveled Condition Mode On	3-10
UP	Increment Selected Parameter	3-12
VM1	Video Marker On	3-7

*Group Execute Trigger

Default Settings

1. Numeric Parameters

   F0 - 10 GHz

   F1 - 2 GHz (Models 6637 & 6638)
   10 MHz (Models 6647 & 6648)

   F2 - 18 GHz

   M1 - 3 GHz (Models 6637 & 6638)
   2 GHz (Models 6647 & 6648)

   M2 - 17 GHz

   ΔF Sweep Width - 1 GHz

   Sweep Time - 50 ms

   Output Power Level - +10 dBm

2. Front Panel Controls

   FREQUENCY RANGE: FULL (low and high-end frequencies are displayed)

   FM AND PHASELOCK: Off

   LEVELING: INTERNAL

   RF ON: On

   RETRACE RF: Off

   TRIGGER: AUTO

   MARKERS: All off

3. Front-Panel-Control-Related Bus Commands

   FULL

   FMØ

   IL1

   RF1

   RTØ

   AUT

   MKØ

APPENDIX 2

STEP SWEEP STEP-TO-FREQUENCY CONVERSION FORMULA

Formula:

$$F = F_{start}\left[+ \frac{N}{4095} \times \left(F_{stop} - F_{start}\right)\right]$$

where F_{start} is the low end of the frequency sweep, as determined by sweep range programming (i.e., Full, F1-F2, M1-M2, etc.)

F_{stop} is the high end of the frequency sweep, as determined by sweep range programming.

N is the step number currently selected. The step number currently selected is found using the following formula:

$$N_{sts} + \left(N_{size} \times \text{number of times the "N" command has been executed}\right)$$

where N_{sts} is the Step Select (STS) Command number.

N_{size} is the Increment Size (SIZ) Command number.

For example, assume the following:

a. Front Panel Control-Related Programming:
   Sweep Range: ΔF, with F0 = 2 GHz and ΔF = 10 MHz
   Command: DF0 F02GH DLF10MH

b. Step Sweep Programming:
   Sweep Start = 0 volts
   Step Size = 819 steps
   No. of Frequency Points: 6
   Command: STP STSE SIZ819E N N N N N

Calculation to Find 1st Frequency Point:

N = 0 + (819 x 0)
F = 1.995 GHz

Calculation to Find 2nd Frequency Point:

N = 0 + (819 x 1)
= 819

$$F = 1.995 \times 10^9 + \left[\frac{819}{4095} \times (2.005 - 1.995)\right] \times 10^9$$

= 1.997 GHz

Calculation to Find 3rd Frequency Point:

N = 0 + (819 x 2)
= 1638

$$F = 1.995 \times 10^9 + \left[\frac{1638}{4095} \times (2.005 - 1.995)\right] \times 10^9$$

= 1.999

Frequencies at 4th, 5th, and 6th Frequency Points:

4th point = 2.001 GHz
5th point = 2.003 GHz
6th point = 2.005 GHz

APPENDIX 3
μP OUTPUT PORTS
(μP-TO-ANALOG INTERFACE)

Sixteen of the twenty-four microprocessor output ports are used to receive data on the analog PCBs. These ports are either octal-latch integrated circuits (ICs) or digital-to-analog converters that contain built-in octal latches. The digital data required for control or implementation of analog functions does not always require eight bits. More or less than eight bits are required for some functions; therefore, certain of the output ports have either:

- one port segmented so that it can be used to latch several different data control-groups of less than 8 bits, or
- two ports combined to latch data control-groups of greater than 8 bits.

The allocation of control-groups with output ports is shown in Table A3-1, and the control-groups are described in Table A3-2.

Table A3-1. Output Port Control Groups, with Correlation between μP Data Bus and Control Group Bits

PORT NO.	CONTROL GROUP	μP DATA BUS BITS WITH CORRESPONDING CONTROL-GROUP DATA BITS							
		B7	B6	B5	B4	B3	B2	B1	B0
0 1	1 LS MS	D7 D15	D6 D14	D5 D13	D4 D12	D3 D11	D2 D10	D1 D9	D0 D8
2	18	D7	D6	D5	D4	D3	D2	D1	D0
3 4	2	D7	D6	D5	D4	D3 D11	D2 D10	D1 D9	D0 D8
4	14				D0				
4	9	D2	D1	D0					
5	4	D7	D6	D5	D4	D3	D2	D1	D0
6 7	3	D7	D6	D5	D4	D3 D11	D2 D10	D1 D9	D0 D8
7	11	D3	D2	D1	D0				
8	5	D7	D6	D5	D4	D3	D2	D1	D0
9	6	D7	D6	D5	D4	D3	D2	D1	D0
10	7	D7	D6	D5	D4	D3	D2	D1	D0
11	8	D7	D6	D5	D4	D3	D2	D1	D0
12	12						D2	D1	D0
12	15			D2	D1	D0			
13 14	13	D7	D6	D5	D4	D3	D2	D1	D0 D8
14	10			D4	D3	D2	D1	D0	
14	23		D0						
14	16	D0							
15	20							D1	D0
15	22						D0		
15	19					D0			
15	17	D3	D2	D1	D0				

Table A3-2. Output Port Control Groups, Descriptions

CONTROL GROUP	NAME	NO. OF BITS	PORT NO.	DESCRIPTION
1	F center DAC	16	0, 1	Negative true logic representing a CW mode frequency or the center frequency in a sweep mode.
2	Step Frequency DAC	12	3, 4	Positive true logic representing the GPIB Step Sweep ramp count.
3	Sweep Width (ΔF) DAC	12	6, 7	Positive true logic representing the width of the frequency sweep.
4	ROM Linearizer Address DAC	8	5	Positive true logic containing the address of the selected linearizer ROM correction frequency.
5	ALC Reference DAC	8	8	Negative true logic representing the front panel LEVEL setting.
6	Marker F0 DAC	8	9	Positive true logic representing the F0 marker frequency.
7	Marker M1 DAC	8	10	Positive true logic representing the M1 marker frequency.
8	Marker M2 DAC	8	11	Positive true logic representing the M2 marker frequency.
9	Sweep Select	3	4	D2 D1 D0 Source of Ramp 0 1 1 A2 PCB ramp output 1 0 1 Step Frequency DAC output 1 1 1 MANUAL SWEEP potentiometer output
10	Trigger Mode	5	14	D4 D3 D2 D1 D0 0 0 0 0 0 Trigger disable 0 0 0 0 1 Auto trigger mode 0 0 0 1 0 Line trigger mode 0 0 1 0 0 Ext/Single Sweep mode 0 ⎍ 1 0 0 Reset ramp ⎍ 0 1 0 0 Trigger ramp from zero
11	Wide/Medium/Narrow/CW	4	7	D2 D1 D0 1 1 1 CW select 0 1 1 Narrow sweep 1 0 1 Medium sweep 1 1 0 Wide sweep D3 0 ΔF≤200 MHz 1 ΔF>200 MHz
12	Marker Inhibit, F0, M1, M2	3	12	D2 D1 D0 1 1 1 All markers on 0 X X F0 marker off X 0 X M1 marker off X X 0 M2 marker off X = Don't care
13	Ramp Rate Select	9	13, 14	Bits D0-D7 are positive true logic bits representing the front panel SWEEP TIME setting. Bit D8 is the > or <1 second control bit. The coding for this bit is as follows: 0 = Sweep speed <1 second, 1 = Sweep speed >1 second.

Table A3-2. Output Port Control Groups, Descriptions (Continued)

CONTROL GROUP	NAME	NO. OF BITS	PORT NO.	DESCRIPTION
14	CW Filter On/Off	1	4	D0 0 CW filter in 1 CW filter out
15	Marker Mode Active	3	12	D2 D1 D0 0 0 0 Markers disabled 0 0 1 RF marker mode 0 1 0 Video marker mode 1 0 0 Intensity marker mode
16	External FM ∅ Lock Enable	1	14	D0 0 Ext FM not enabled 1 Ext FM enabled
17	Programmable Attenuator (Option 2)	4	15	D3 D2 D1 D0 Attenuation 0 0 0 0 0 dB 0 0 0 1 -10 dB 0 0 1 0 -20 dB 0 0 1 1 -30 dB 0 1 0 0 -40 dB 0 1 0 1 -50 dB 0 1 1 0 -60 dB 0 1 1 1 -70 dB 1 1 0 0 -80 dB 1 1 0 1 -90 dB 1 1 1 0 -100 dB 1 1 1 1 -110 dB (0 dB to -70 dB: 70 dB Attn. Range; 0 dB to -110 dB: 110 dB Attn. Range)
18	Frequency Vernier (Freq Ver) DAC	8	2	Where word • equals zero (0000 0000), there is maximum negative frequency correction; • equals 128 (1000 0000), there is no frequency correction; • equals 255 (1111 1111), there is maximum positive frequency correction.
19	RF On/Off	1	15	D0 0 RF off 1 RF on
20	ALC Leveling Mode	2	15	D1 D0 0 0 Unleveled 0 1 Internal leveling 1 0 External detector 1 1 External power meter
21	Not used			
22	Retrace RF	1	15	D0 0 RF on during retrace 1 RF off during retrace
23	Sequential Sync Disable	1	14	When D0 bit is HIGH, the sequential sync pulse is disabled.