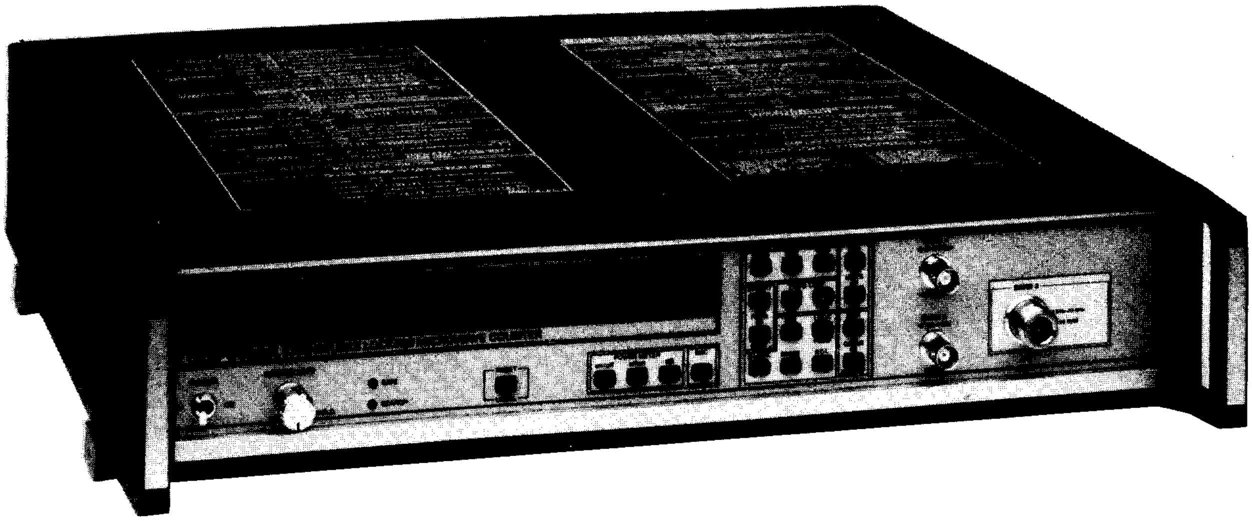

Models 575B & 578B
Source Locking
Microwave Counters

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Manual Part Number: 5580032-01
Printed in U.S.A., February 1988

575B: CCN 1809
578B: CCN 2009

Printing History

New editions incorporate all update material since the previous edition. The date on the title page changes only when a new edition is published. If minor corrections and updates are incorporated, the manual is reprinted but the date and edition number on the title page do not change.

FIRST EDITION .... February, 1988

Certification

EIP Microwave certifies that this instrument was thoroughly inspected and tested, and found to be in conformance with the specifications noted herein at time of shipment from factory.

Warranty

EIP Microwave warrants this counter to be free from defects in material and workmanship for one year from the date of delivery. Damage due to accident, abuse, or improper signal level is not covered by the warranty. Removal, defacement, or alteration of any serial or inspection label, marking, or seal, may void the warranty. EIP Microwave will repair or replace at its option any components of this counter which prove to be defective during the warranty period, provided the entire counter is returned PREPAID to EIP or an authorized service facility. In-warranty counters will be returned freight prepaid; out-of-warranty units will be returned freight COLLECT. No other warranty other than the above warranty is expressed or implied.

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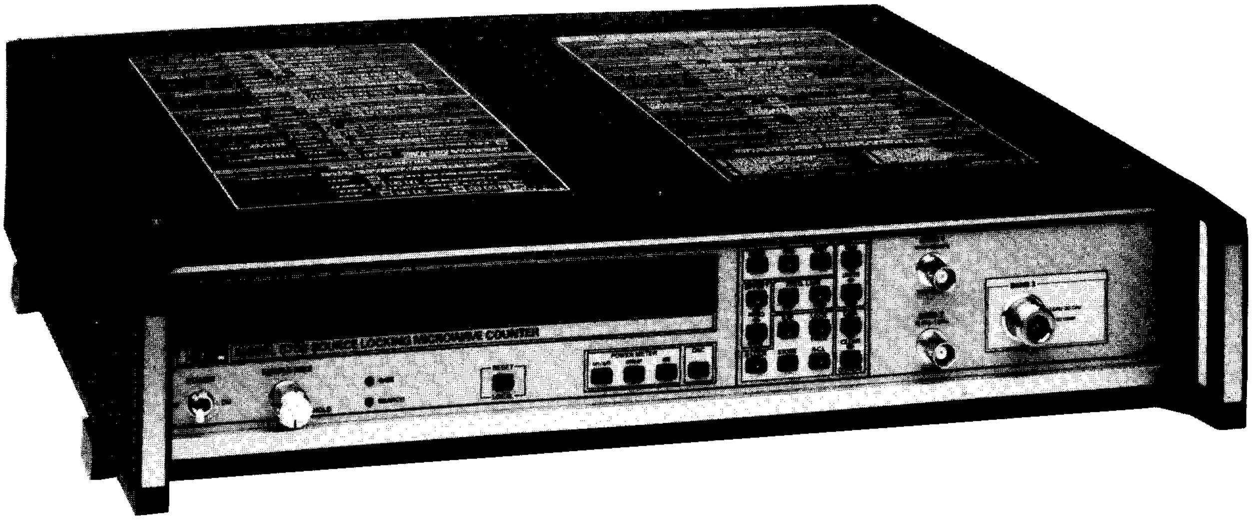
Section 1
General Information



DESCRIPTION

The Model 575B and Model 578B Source Locking Counters are multi-function microprocessor based devices. These counters are not only able to perform frequency and (optionally) power measurement, but can tune and phase lock an external signal source over a wide range of frequencies. The basic frequency range of the 575B is 10 Hz to 20 GHz, while the 578B extends to 26.5 GHz.

When the 578B is equipped with Frequency Extension Capability (Option 06) and used with external accessories such as the Model 590 and a Remote Sensor, the counter is capable of operationg up to 110 GHz.

Frequency counting is divided into 4 bands. Band 1 is a high impedance input (1 M ohm/20 pF) and covers 10 Hz to 100 MHz with a sensitivity of 25 mV RMS. Band 2 is a 50 ohm input operating from 10 MHz to 1 GHz with a minimum sensitivity of -20 dBm. Band 3 is also a 50 ohm input and covers the range of 1 GHz to 20 GHz using the 575B, and 1 GHz to 26.5 GHz using the 578B, with sensitivity to -30 dBm. The 578B has optional frequency coverage that is designated as Band 4, and is subdivided into 5 frequency ranges, each with a typical sensitivity of -25 dBm.

Band 41	26.5 - 40 GHz
Band 42	40 - 60 GHz
Band 43	60 - 90 GHz
Band 44	90 - 110 GHz
Band 42, 43	50 - 75 GHz

An optional power measurement capability (Option 02) is available to supplement Band 3. With this option the counter can simultaneously display frequency to 100 kHz resolution, and power to .1 dB resolution. Typical accuracy of power measurement is 0.5 dB (at 25° C). Range is from sensitivity up to +10 dBm.

The other major feature of the 57XB counters is the ability to tune and phase lock virtually any frequency source that is capable of being electronically tuned. Two output ports are provided, one for coarse tune and one for phase lock. With these outputs a source can be locked from 10 MHz up to the maximum operating frequency of the counter. Frequencies can be selected to a resolution of 10 kHz and maintain the long term accuracy and stability of the internal time base crystal oscillator.

Using the keyboard (or IEEE 488-1978 bus control) the 57XB counters provide not only the major counter functions but a variety of other capabilities such as frequency offsets, power offsets, and a frequency multiple function. Optional capabilities can also include a digital to analog converter (DAC) and three high stability oven oscillators.

SPECIFICATIONS

GENERAL	
RESOLUTION	Front panel keyboard input select .1 Hz to 1 GHz * 0.1 Hz resolution Band 1 only. No frequency offset or multiplier in 0.1 Hz resolution.
MEASUREMENT TIME	1 msec for 1 kHz resolution 1 sec for 1 Hz resolution
DISPLAY	12 digit LED sectionalized
ACCURACY	± 1 count ± time base errors
TEST	Front panel selected diagnostics
SAMPLE RATE	Controls time between measurements variable from 100 msec typ. to 10 sec. Switchable Hold position holds display indefinitely.
RESET	Resets display to zero and initiates new reading
OFFSETS	Keyboard control of frequency offsets (standard) and power offsets (standard with power measurement Option 02). Displayed frequency (power) is offset by entering value to 1 Hz resolution (0.1 dB power).
OPERATION TEMP.	0° C to 50° C
POWER	100/120/220/240/VAC ± 10% (selectable) 50 to 60 Hz, 60 VA typical
WEIGHT, NET	~ 26 lb (11.8 kg)
WEIGHT, SHIPPING	~ 32 lb (14.5 kg)
DIMENSIONS (HWD)	3.5'' x 16.75'' x 14.0'' (89 mm x 425 mm x 356 mm)
ACCESSORIES FURNISHED	Power Cord and Manual

SPECIFICATIONS, continued

BAND 1

RANGE	10 Hz to 100 MHz
SENSITIVITY	25 mV rms
IMPEDANCE	1 M ohm/20 pF
CONNECTOR	BNC (female)
MAX. INPUT LEVEL	120 V rms *
DAMAGE LEVEL	150 V rms *
	* (Above 1 kHz max. input will decrease at 6 dB/octave down to 3.0 V rms.)

BAND 2

RANGE	10 MHz to 1 GHz
SENSITIVITY	-20 dBm
DYNAMIC RANGE	30 dB
IMPEDANCE	50 ohms Nominal
CONNECTOR	BNC (female)
MAX. INPUT LEVEL	+10 dBm
DAMAGE LEVEL	+27 dBm
ACQUISITION TIME	<50 msec

BAND 3

RANGE	1 GHz to 20 GHz (26.5 GHz for model 578B)
SENSITIVITY	-30 dBm: 1 GHz to 12.4 GHz: -25 dBm: 12.4 GHz to 20 GHz: -20 dBm: 20 GHz to 26.5 GHz:
DYNAMIC RANGE	1 GHz to 12.4 GHz, 40 dB 12.4 GHz to 20 GHz, 35 dB 20 GHz to 26.5 GHz, 30 dB
IMPEDANCE	50 ohms Nominal
CONNECTOR	Model 575B: Precision Type N (female) Model 578B: DMS (female)
MAX. INPUT LEVEL	+10 dBm
DAMAGE LEVEL	5 Watts, (+37 dBm)
ACQUISITION TIME	< 200 msec Independent of frequency
AUTO AMPLITUDE DISCRIMINATION	(Automatic amplitude discrimination of two frequencies) 10 dB
FM MODULATION	20 MHz p-p up to 10 MHz rate
VSWR	< 2.5: 1 typical
FREQUENCY LIMIT	Keyboard control of desired limits (standard). Counter will measure largest signal within programmed limits. Signal outside operating band must be separated by at least 100 MHz from either limit. For signal more than 10 dB above desired signal, separation is typically 200 MHz.

TIME BASE

FREQUENCY	10 MHz TCXO
AGING RATE	$<\vert 1 \times 10^{-7} \vert$ per month, $\vert$ 1 x 10 $\vert$ $\vert$ 1×10^{-6} $\vert$per year
SHORT TERM	$<\vert 1 \times 10^{-9} \vert$rms for one second averaging time
TEMPERATURE	$<\vert 1 \times 10^{-6} \vert$ 0° to 50° C when set at 25° C
LINE VARIATION	$<\vert 1 \times 10^{-7} \vert$ ± 10% change.
WARM UP TIME	NONE
OUTPUT FREQUENCY	10 MHz, square-wave, 1 V p-p minimum into 50 ohms.
EXT. TIME BASE	Requires 10 MHz, 1 V p-p minimum into 300 ohms
PHASE NOISE	-95 dBc/Hz at 10 Hz from carrier

BAND 4
Used with 578B/06 Counter and 590 Frequency Extension Kit

OPTION	**91**	**92**	**93**	**94**	**95**	**96**
SELECT BAND	**41**	**42**	**43**	**44**	**42 or 43**	**41 or 42**
Waveguide Band	Ka	U	E	W	V	Q
Range	26.5–40 GHz	40–60 GHz	60–90 GHz	90–110 GHz	50–75 GHz	33–50 GHz
Sensitivity (typ)	–25dBm (–20 dBm min)	–25 dBm	–25 dBm	–25 dBm	–25 dBm	–25 dBm
Waveguide Size	WR–28	WR–19	WR–12	WR–10	WR–15	WR–22
Waveguide Flange	UG–599/U	UG–383/U	UG–387/U	UG–387/U	UG–385/U	UG–383/U
Max. Input (typ)	+5 dBm	+5 dBm	+5 dBm	+5 dBm	+5 dBm	+5 dBm
Damage Level	+10 dBm	+10 dBm	+10 dBm	+10 dBm	+10 dBm	+10 dBm
Aquisition Time (typ)	<1 sec	<1 sec	<1 sec	<1 sec	<1 sec	<1 sec

EXAMPLE: If desired measurement is 60 – 90 GHz, the required equipment is:

Model 578B with Option 06 – Extended Frequency and
Model 590 – Extended Frequency Cable Kit with Option 93 – Remote Sensor

SOURCE LOCK	
FREQUENCY RANGE	10 MHz – Max. capability of counter.
RESOLUTION	10 kHz for phase lock freq. ≥ 50 MHz 2.5 kHz for < 50 MHz
ACCURACY	equal to counter's Time Base
LONG TERM STABILITY	Equal to counter's Time Base
MIN. PHASE LOCK SIGNAL LEVEL	Equal to counter's sensitivity
POLARITY	User select, 10 kHz, 2 kHz, or 500 Hz, or automatically selects widest bandwidth capable of locking.
LOCK TIME (TYP)	
COARSE TUNE	50 m sec + 1 counter acquisition time for source bandwidth greater than 100 Hz, Limited by source tuning speed below 100 Hz.
PHASE LOCK	200 m sec.
RECALLING STORED DATA	1 counter acquisition + 100 m sec. limited by source tunig speed.
OUTPUT DRIVE (MAX)	
COARSE TUNE OUTPUT	+ 10 V into 5 K ohm min.
PHASE LOCK OUTPUT	± 10 V into 5 K ohm min for source gain constant < 64 MHz/V. ± 75 MA into 10 ohm max for source gain constant < 3.2 MHz/MA. ± .6 V into 5 K ohm min for source gain constant ≥ 64 MHz/V. ± 4.5 MA into 10 ohm max for source gain constant ≥ 3.2 MHz/MA.
CAPTURE RANGE	
COARSE TUNE	Entire range of selected counter band limited by maximum output drive.
PHASE LOCK	Source gain constant X maximum output drive.

SPECIFICATIONS, continued

OUTPUT CONNECTOR

COARSE TUNE	Rear panel BNC, female
PHASE LOCK	Rear panel BNC, female

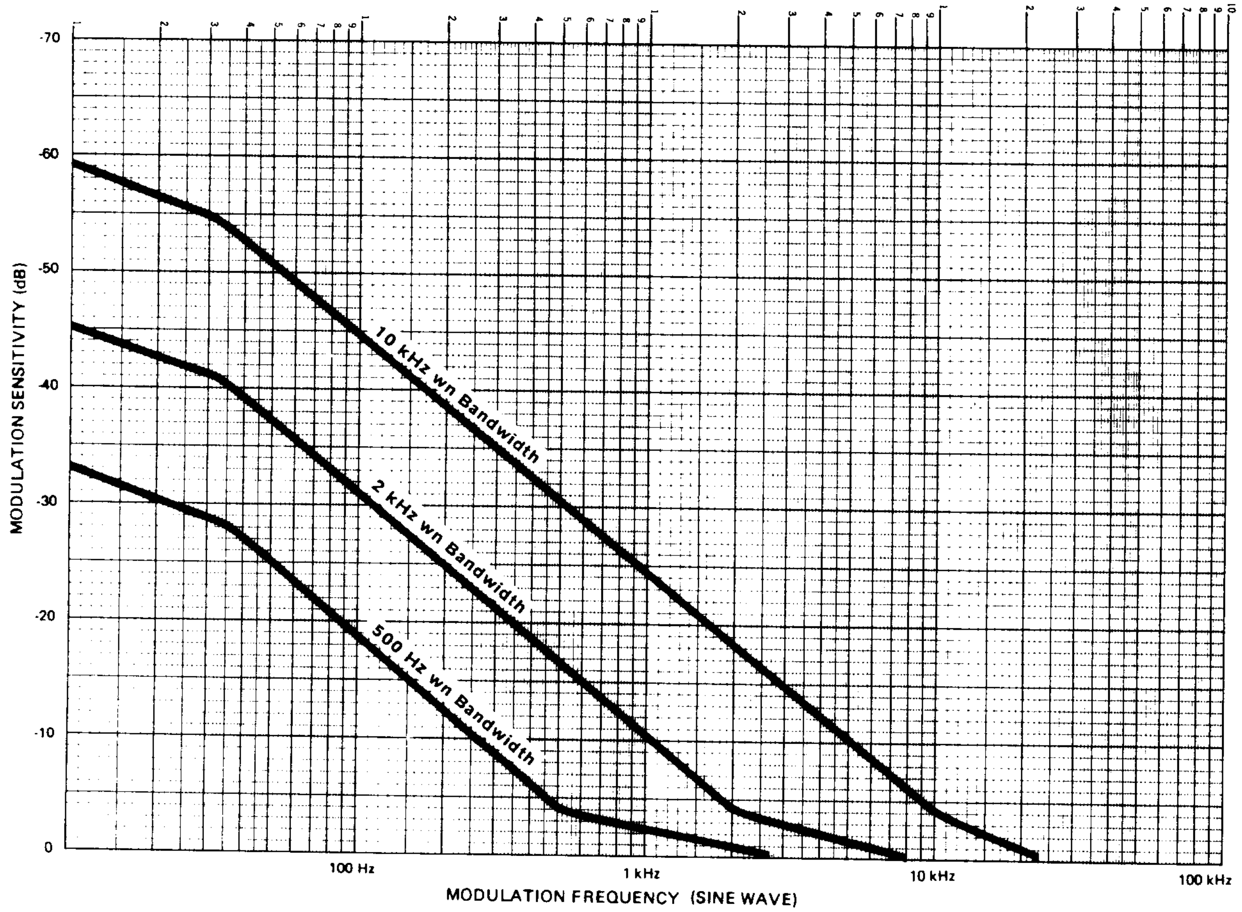
PHASE LOCKED SPECTRUM

NOISE FLOOR vs INPUT FREQUENCY :

The noise floor extends from the carrier to approximately the loop bandwidth. Beyond this the noise floor decreases 12 dB / bandwidth octave. The noise floor is the greater of :

1. NOISE FLOOR = -70 dBC / Hz
2. NOISE FLOOR = (20 log F -65) dBC / Hz
   where F = Input frequency in GHz

NOISE REDUCTION vs MODULATION FREQUENCY :

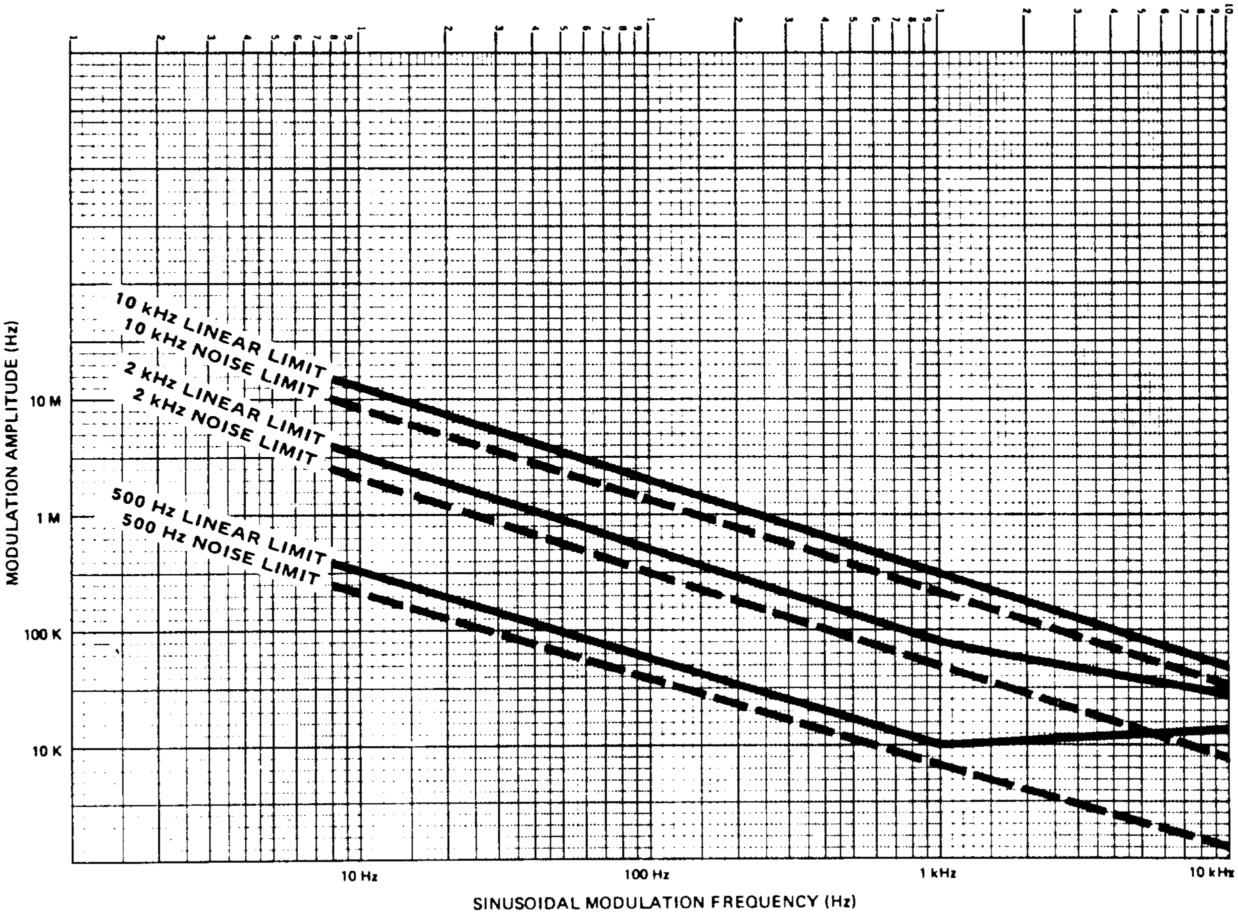


SPECIFICATIONS, continued

SOURCE CHARACTERISTICS (required)	
COARSE TUNE INPUT :	
BANDWIDTH	5 Hz minimum
TUNING SENSITIVITY	10 MHz / V minimum 10 GHz / V maximum
PHASE LOCK (FM) INPUT :	
BANDWIDTH	2 kHz minimum
TUNING SENSITIVITY :	
VOLTAGE DRIVEN INPUT	± 2 MHz / V minimum ± 1000 MHz / V maximum
CURRENT DRIVEN INPUT	± 0.1 MHz / mA minimum ± 50 MHz / mA maximum

MAXIMUM FM

The counter will still frequency stabilize if maximum FM is exceeded, but accuracy and long term stability will not equal the counter's time base.



SPECIFICATIONS, continued

OPTIONS

01 D TO A CONVERTER
DAC will convert any three consecutively displayed digits into an analog voltage output on rear panel.

02 POWER METER
1 to 18/26.5 GHz will measure sine wave amplitude to 0.1 dBm resolution from sensitivity to -20 dBm: 0.2 dBm resolution from -10 dBm to overload and display simultaneously with frequency. Power offset to 0.1 dB resolution, selectable from front panel; will not degrade performance of the counter.

NOTE

Power Meter and Source Locking cannot be active at the same time.

TIME BASE OSCILLATOR OPTIONS:

	03	04	05
AGING RATE/24 HOURS (After 72 hour warm-up)	$<\|5 \times 10^{-9}\|$	$<\|1 \times 10^{-9}\|$	$<\|5 \times 10^{-10}\|$
SHORT TERM STABILITY (1 second average)	$< 1 \times 10^{-10}$ rms	$< 1 \times 10^{-10}$ rms	$< 1 \times 10^{-10}$ rms
0°to +50°C TEMPERATURE STABILITY	$<\|6 \times 10^{-8}\|$	$<\|3 \times 10^{-8}\|$	$<\|3 \times 10^{-8}\|$
± 10% LINE VOLTAGE CHANGE	$<\|5 \times 10^{-10}\|$	$<\|2 \times 10^{-10}\|$	$<\|2 \times 10^{-10}\|$

06 EXTENDED FREQUENCY CAPABILITY – 578B
Use in conjunction with model 590 Frequency Extension Cable kit and a remote sensor.

09 REAR INPUT

10 CHASSIS SLIDES

Section 2

Installation

INSTALLATION

No special installation instructions are required. The counter is a self-contained bench or rack mounted unit and only requires connection to a standard 100/120/220/240V 50-60 Hz power line for operation.

CAUTION

Check current rating of counter fuse and setting of rear panel VAC selector switch before applying power to counter.

COUNTER IDENTIFICATION

This counter is identified by two sets of numbers, the model number 545B or 548B and a serial number that is located on a label affixed to the rear panel. Both numbers must be mentioned in any correspondence regarding this counter.

SHIPPING

Wrap the counter in heavy plastic or kraft paper and repack in original container if available. If the original container cannot be used, use a heavy (275-pound test) double-walled carton with approximately four inches of packing material between the counter and the inner carton. Seal the carton with strong filament tape or strapping. Mark the carton to indicate that it contains a fragile electronic instrument. Ship to the EIP address on the title page of this manual.

PERFORMANCE CHECKOUT PROCEDURE

The following procedure can be performed without special tools or equipment.

1. Turn counter power switch off. Check fuse rating and setting of AC POWER switch on rear panel.

2. Connect power cord to 100/120 or 220/240 V, 50-60 Hz single-phase power source. The ground terminal on the power cord plug should be grounded.

3. Turn POWER switch on. Dashes will be displayed for about one second, followed by all 0's. This indicates that automatic self-check has been completed.

4. Press $\overset{\text{TEST}}{\boxed{\quad}}\ \boxed{0}\ \boxed{1}$. Display should read 200 000 000 ±1.

5. Press $\overset{\text{TEST}}{\boxed{\quad}}\ \boxed{0}\ \boxed{2}$. Display should read all 8's and all annunciators should be lit.

6. Press $\overset{\text{TEST}}{\boxed{\quad}}\ \boxed{0}\ \boxed{3}$. Each display segment should light in turn.

7. Press $\overset{\text{TEST}}{\boxed{\quad}}\ \boxed{0}\ \boxed{4}$. Each digit should light in turn.

8. This completes the performance checkout procedure.

Section 3
Operation

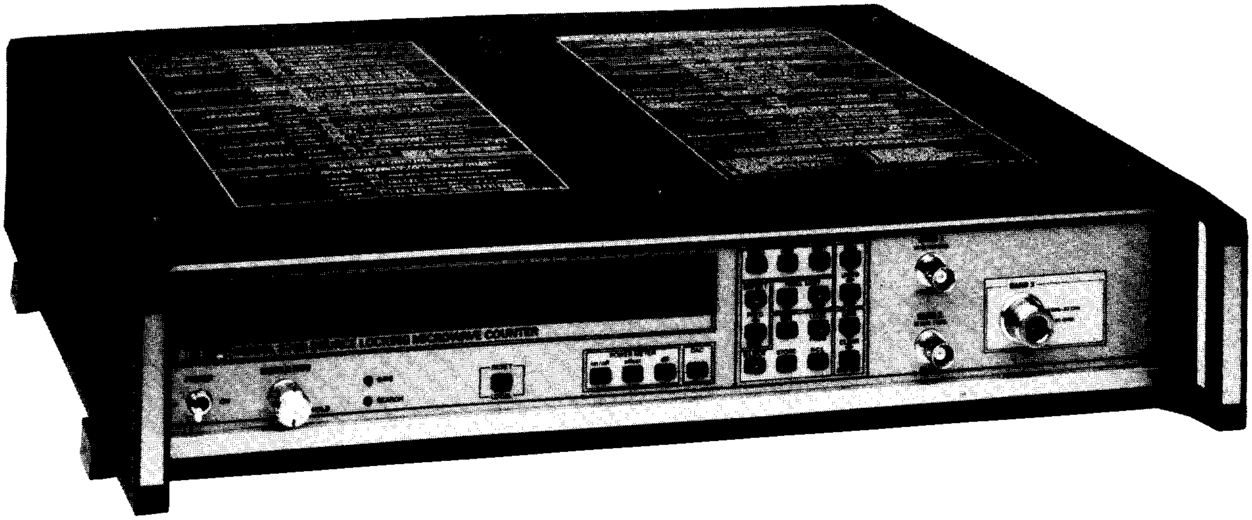


Figure 3-1. Front Panel, Model 575B

FRONT PANEL CONTROLS AND INDICATORS

DISPLAY

- The 12 digit LED display provides a direct numerical readout of a measurement or of an input frequency. The frequency readout is displayed in a fixed position format that is sectionalized in GHz, MHz, kHz and Hz. Power information is displayed in dBm to 0.1 dB resolution, on the three right-most digits. When both power and frequency are displayed, frequency resolution is limited to 100 kHz.

POWER switch turns counter on.

SAMPLE RATE/HOLD varies time between measurements from 0.1 to 10 seconds (nominal). (Gate time is added to sample time, thus the minimum reading for 1 Hz resolution is 1.1 seconds.) The last reading is retained indefinitely in HOLD until Reset is issued.

GATE lights when the signal gate is open and a measurement is being made.

- SEARCH lights when the counter is not locked to an input signal.

RESET manually overrides all controls, resets the counter and converter, and initiates a new reading.

OPERATING STATUS

The operating status of the counter is indicated by a series of LEDs. When the counter is displaying input data, instead of a measurement, the appropriate LED status indicator will flash.

- RMT lights to indicate that front panel controls are disabled, and that the counter is being controlled through the GPIB Bus interface.
- EXT REF lights to indicate the counter is set to an external time base reference.

CAUTION

When EXT REF lights it does NOT indicate that correct signal level has been applied.

- dBm lights to indicate that the Power Meter option (02) is active.
- FRQ LMT, LOW/HIGH lights when frequency limits for Band 3 operation have been selected.
- OFFSET, PWR/FRQ lights when power and/or frequency offsets are stored in the counter memory.
- Band 1, 2, 3, 41, 42, 43, 44 light to indicate which operating range has been selected. When any Band 4 annunciator is lit it indicates that the Extended Frequency Capability option (06) has been selected (Available on 578B only).
- DAC lights to indicate that the Digital-to-Analog Converter option 01 is active.
- MLT lights to indicate the multiplier function is active.
- LCK lights when the counter is phase locked.
- BW lights to indicate a phase lock loop bandwidth has been selected.

POWER METER/DAC OPTION KEYBOARD

Four keys control the operation of these options.

- Power Meter ON/OFF pushbutton activates/deactivates power meter.
- Power Meter OFFSET pus button activates the power offset function.
- dB pushbutton acts as a terminator for the input of power offsets.
- DAC pushbutton, followed by two digits (00–12), activates the DAC option. The number keyed in will select the most significant digit (00 = OFF, 01 = 1 Hz, 12 = 100 GHz).

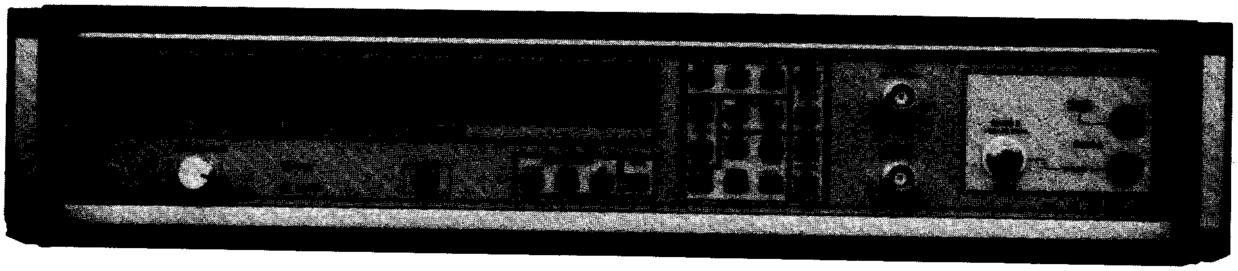


Figure 3-2. Front Panel, Model 578B

SIGNAL INPUT

Band 1 input connector (BCN female) has a nominal input impedance of 1 Meg ohms, shunted by 20 pF. It is used for measurements in the range of 10 Hz to 100 MHz.

Band 2 input connector (BNC female) has a nominal input impedance of 50 ohms. It is used for measurements in the range of 10 MHz to 1 GHz.

Band 3 input connector on the model 575B is a precision type N female. It is used for counter operation in the range of 1 GHz to 20 GHz. Model 578B has an APC-3.5 female connector that is used for operation in the range of 1 GHz to 26.5 GHz.

- Band 4 is used in conjunction with the Extended Frequency capability option (06), the Model 590 Frequency Extension Cable kit and a remote sensor. Remote sensors are options to the Model 590 and cover waveguide bands from 26.5 to 110 GHz.

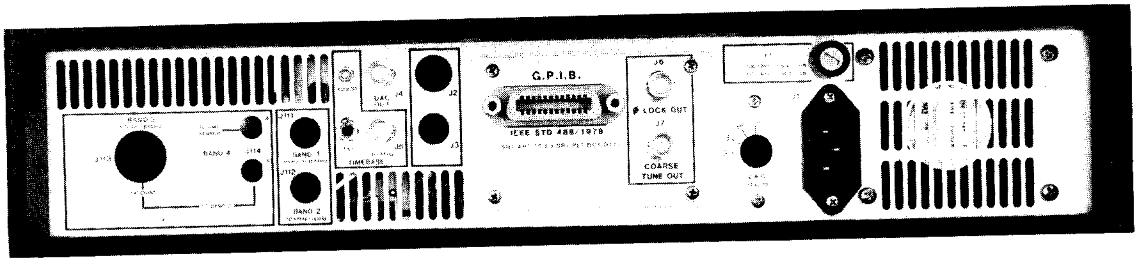


Figure 3-3. Rear Panel

REAR PANEL CONTROLS AND CONNECTORS

- Spaces labeled BAND 1, BAND 2, BAND 3, BAND 4, and TO REMOTE SENSOR are used for those connectors in instruments equipped with Option 09, Rear Panel Input.
- TIME BASE ADJUST control is used with options 03, 04, or 05 only. Screwdriver adjustment allows precise setting of the internal ovenized crystal oscillator.

TIME BASE INT/EXT switch selects either the internal time base or an external 10 MHz reference.

TIME BASE connector (BNC female) allows monitoring of internal 10 MHz time base, or input of an external 10 MHz reference.

- DAC OUT connector provides a voltage analog to any specified three digits of frequency displayed, in instruments equipped with Option 01, D to A Converter.

GPIB connector is used with the IEEE 488 - 1978 General Purpose Interface Bus.

PHASE LOCK OUT connector (BNC female).

- COARSE TUNE OUT connector (BNC female).

FUSE provides overload protection. Use a 1 amp slow-blow MDL type fuse for 100/120 V operation. Use a .50 amp slow-blow FST type fuse for 220/240 V operation.

VAC SWITCH sets the operating voltage of the counter to match power line. There are 4 settings: 100, 120, 220, and 240 VAC. Counter will operate at voltages within ±10% of selected line voltage, at frequencies of 50 to 60 Hz.

CAUTION

Switch setting and fuse rating must match power line voltage.

AC POWER connector accepts the power cord supplied with the counter.

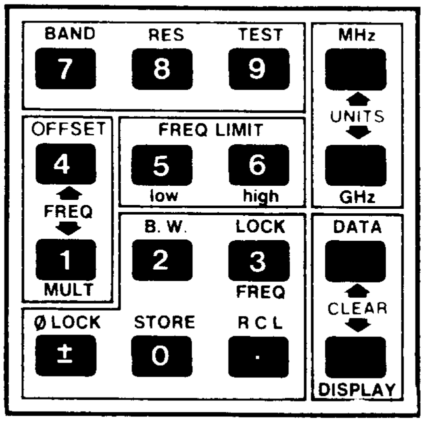
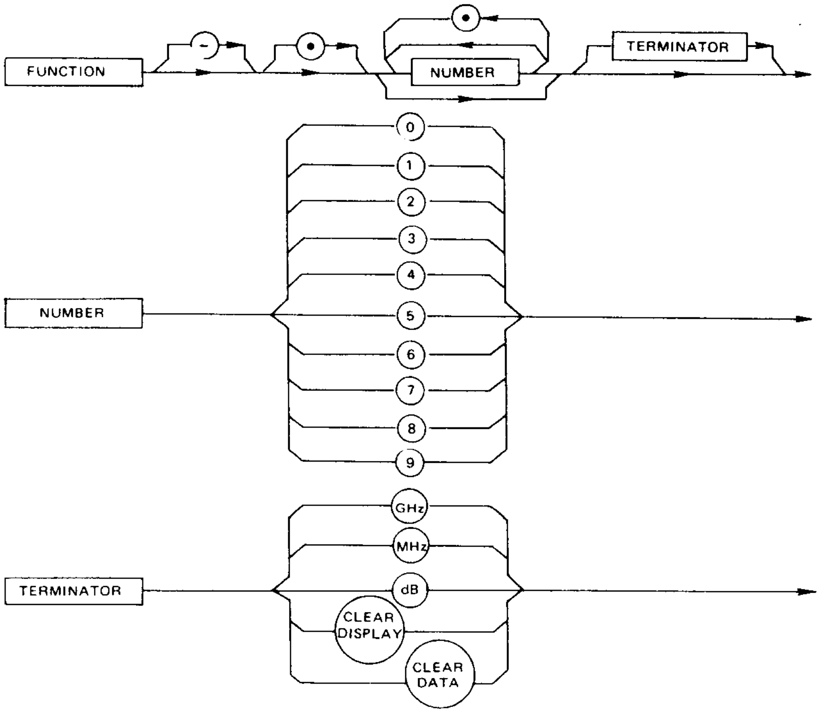


Figure 3-4. Keyboard

KEYBOARD

The keyboard consists of 16 pushbuttons that control major functions of the counter. Twelve keys are used for numerical data entry—the digits 0 through 9, the decimal point and the minus sign. Two keys (MHz and GHz) act as terminators for the input of frequency offset, frequency limits, or phase lock frequency. The CLEAR DATA and CLEAR DISPLAY keys are used to clear stored or displayed data. Twelve of the keys are also used to select the band, resolution, test function, frequency offset, frequency limits, multiplier, band width, lock frequency, phase lock, store, and recall functions.

The keyboard operation syntax is:



UNITS (MHz/GHz)

PRESS: MHz Completes Entry Sequence

PRESS: GHz Completes Entry Sequence

PRESS: dB Completes Entry Sequence

CLEAR (DATA/DISPLAY)

Press: DATA CLEAR Return "STORED" data of selected function to Power On state. Clears Limits (Low/High), Offsets, DAC, multiplier, band width, lock frequency, and stored phase lock information.

Press: CLEAR DISPLAY Clears display. Does not affect stored data. Restores counter to display measurement. Clears entry if counter is in data entry mode.

COUNTER CONTROL FUNCTIONS

BAND SELECTION

The ''BAND'' KEY followed by a numeric key enables the following band selection on model 575B or 578B.

PRESS: BAND 1 10 Hz - 100 MHz Input

PRESS: BAND 2 10 MHz - 1 GHz Input

PRESS: BAND 3 1 GHz - 20 GHz (Model 575B) 26.5 GHz (Model 578B)

Notice annunciator flash and selected band number will light when chosen. This feature allows multiple inputs to be connected and selected in turn.

On the model 578B equipped with Option 06, a 590 cable kit and appropriate optional remote sensor, Band 4 is selected by:

PRESS: BAND 4 X

X should be a number between 1 and 4.

RESOLUTION/GATE TIME SELECTION

The "RESOL" key followed by a numeric key enables following resolutions.

PRESS: RESOL 0 1 Hz RESOLUTION

PRESS: RESOL 1 10 Hz RESOLUTION

PRESS: RESOL 2 100 Hz RESOLUTION

PRESS: RESOL 3 1 KHz RESOLUTION

PRESS: RESOL 4 10 KHz RESOLUTION

PRESS: RESOL 5 100 KHz RESOLUTION

PRESS: RESOL 6 1 MHz RESOLUTION

PRESS: RESOL 7 10 MHz RESOLUTION

PRESS: RESOL 8 100 MHz RESOLUTION

PRESS: RESOL 9 1 GHz RESOLUTION

0.1 HZ RESOLUTION

In order to extend the resolution to 0.1 Hz in Band 1, the gate time inside the counter is increased to 10 seconds. Therefore, if the count chain reads 11 after the 10-second gate period, then the frequency displayed is 1.1 Hz.

The significance of the digits on the front panel is shifted left three digits. If the frequency of the input signal is 9 MHz, the counter displays 9 GHz.

If the user changes the resolution during the 10-second gate period, the counter still has to wait for the 10-second gate to complete before it changes the gate time accordingly.

To change the counter gate time to 10-seconds through front panel:

1. Select "band 1".
2. Enter "res", ".1".

To change the counter gate time to 10-seconds via GPIB:

1. Command the counter "B1R.1"

To change the counter gate time to 10-seconds via MATE (Option 13), enter the following commands:

1. "CLS :CH01"
2. "FNC ACS FREQ :CH01 SET FRES 0.1".

RESET

When the RESET key is pushed, the counter will reset the converter and basic counter. All stored information will not be altered. When the key is released, the counter will reacquire the input signal. It will take one reading after reacquisition even if the counter is in the hold mode.

PRESS:	RESET LOCAL	To reset converter and basic counter.

FREQUENCY LIMITS

Enables entry of frequency limits to 10 MHz resolution. The converter is reset after the entry sequence.

TO INPUT FREQUENCY LIMITS

PRESS:	FREQ LIMIT low	Notice flashing annunciator and frequency low limit last entered.
PRESS:	#	Number keys corresponding to desired frequency low limit to 10 MHz resolution.
PRESS:	MHz or GHz	To terminate input sequence. Notice FRQ LMT LOW annunciators solidly lit after terminator key is released.
PRESS:	FREQ LIMIT high	Notice flashing annunciator and frequency limit high last entered.
PRESS:	#	Number keys corresponding to desired frequency high limits to 10 MHz resolution.
PRESS:	MHz or GHz	To terminate input sequence. Notice FRQ LMT HI annunciator solidly lit after terminator key is released.

TO RECALL STORED LIMITS:

PRESS:	FREQ LIMIT low or FREQ LIMIT high	Stored frequency limit low/high is displayed on front panel.
PRESS:	CLEAR DISPLAY	Returns counter to display measurements.

TO REMOVE FREQUENCY LIMITS

PRESS:	FREQ LIMIT low	CLEAR DATA	OR	FREQ LIMIT high	CLEAR DATA

NOTE: High and low limits should be separated by at least 100 MHz.

DATA MANIPULATION FUNCTIONS

FREQUENCY OFFSET

Frequency offset function enables the entry of a positive or negative frequency offset to 1 Hz resolution. The offset will be incorporated into the frequency measurement after the next gate.

TO INPUT FREQUENCY OFFSETS

PRESS: FREQ OFFSET Notice flashing annunciator and frequency offset last entered.

PRESS: # Number keys corresponding to desired offset frequency to 1 Hz resolution.

PRESS: MHz OR GHz To terminate input sequence. Notice OFFSET FRQ annunciator solidly lit after terminator key is released.

TO RECALL STORED OFFSETS

PRESS: FREQ OFFSET Stored offset is displayed.

PRESS: CLEAR DISPLAY Returns counter to display measurements.

TO REMOVE FREQUENCY OFFSETS

PRESS: FREQ OFFSET DATA CLEAR OR FREQ OFFSET 0 GHz OR FREQ OFFSET GHz

MULTIPLY FUNCTION

The multiply function multiples the measured frequency by a positive integer up to 99. The result is displayed to 1 KHz resolution. The multiplier will be incorporated into the frequency measurement after the next gate.

TO ENTER A MULTIPLIER

PRESS: FREQ MULT Notice flashing annunciator and multiplier last entered.

PRESS: # # Number keys corresponding to desired multiplier.
Notice MLT annunciator solidly lit after second key is released.

EXAMPLE: FREQ MULT 0 2 FOR MULTIPLIER = 2

TO CLEAR THE MULTIPLIER FUNCTION

PRESS FREQ MULT DATA CLEAR OR FREQ MULT 0 1

TO RECALL MULTIPLIER

PRESS: FREQ ☐ MULT — Stored frequency multiplier is displayed on front panel.

PRESS: CLEAR ☐ DISPLAY — Returns counter to display measurements.

mX ±B

By using the frequency offset and multiply functions the counter can automatically perform mX ±B calculations.

The equation for the function performed is:

Displayed Reading = mX ±B where m = Multiplier (0 to 99) entered from keyboard.

X = Input frequency.

±B = Frequency offset entered from the keyboard.

To do mX ±B calculation for m = 2, b = 70 MHz

PRESS: FREQ ☐ MULT [0] [2] AND FREQ ☐ OFFSET [7] [0] MHz ☐

SOURCE LOCKING FUNCTIONS

PHASE LOCK FREQUENCY

Enables entry of phase lock frequency to 10 kHz resolution if phase lock frequency is above or equal to 50 MHz, and 2.5 kHz resolution if it is below 50 MHz. The counter will attempt to phase lock after the entry sequence is terminated. The phase lock operation will terminate if the RESET key is pressed while the counter is attempting to phase lock.

TO ENTER PHASE LOCK FREQUENCY

PRESS: LOCK ☐ FREQ — Notice flashing annunciator and phase lock frequency last entered.

PRESS: [#] — Number keys corresponding to desired phase lock frequency.

PRESS: MHz ☐ or ☐ GHz — To terminate input sequence. Notice LCK annunciator continues to flash while counter is attempting to phase lock. LCK annunciator will light solidly if phase lock is successful. If not, the LCK annunciator will continue to flash until lock is achieved or until the sequence is manually terminated.

TO RECALL STORED PHASE LOCK FREQUENCY

PRESS: LOCK ☐ FREQ — Stored phase lock frequency is displayed on front panel.

PRESS: CLEAR ☐ DISPLAY — Returns counter to display measurements.

TO REMOVE PHASE LOCK FREQUENCY

PRESS: LOCK ☐ FREQ DATA ☐ CLEAR OR LOCK ☐ FREQ 0 ☐ GHz OR LOCK ☐ FREQ ☐ GHz

After phase lock frequency is cleared, the coarse tune output will return to +5V and the phase lock output will return to 0V.

NOTE

When the counter is attempting to phase lock, the information displayed on the front panel is the frequency the counter is attempting to phase lock to. During the phase lock process, if the RESET key is pressed, the counter will abort the process and return to regular measurement mode.

The coarse tune output is returned to +5V only if the source lock frequency is cleared, otherwise it will stay at the same voltage it was last at. The phase lock output is returned to 0V when the counter is in phase lock mode.

PHASE LOCK KEY

Enables the counter to attempt to phase lock to the frequency last entered through the PHASE LOCK FREQUENCY function. The front panel displays the frequency the counter is trying to phase lock, and the annunciator flashes. If the phase lock process is successful, the annunciator will be solidly lit; if not, the annunciator will continue to flash until the function is manually terminated.

The PHASE LOCK KEY is also used in conjunction with the RECALL function to enable the user to phase lock stored frequency expeditiously. (See description of RECALL function.)

BAND WIDTH

The BW key followed by a numeric key enables the following bandwidth selections.

PRESS: BW ☐ 1 500 Hz loop bandwidth

PRESS: BW ☐ 2 2 kHz loop bandwidth

PRESS: BW ☐ 3 10 kHz loop bandwidth

PRESS: BW ☐ 0 Automatic loop bandwidth selection.

Bandwidth 0 enables the counter to automatically select the phase lock loop bandwidth. When in BW0, the counter, during the phase lock process, will try to close the phase lock loop in the 10 kHz, 2 kHz and 500 Hz bandwidth sequentially. It will stop at the first bandwidth in which it can close the phase lock loop.

TO RECALL STORED BANDWIDTH

PRESS: BW ☐ Notice flashing annunciator, and last selected bandwidth number followed by the bandwidth in Hz.

CLEAR ☐ DISPLAY Returns counter to display measurements.

STORE

Enables the storage of the current phase lock frequency, along with other important information. This function can be activated only after the counter has been phase locked. An error will occur if the function is activated when the counter is not phase locked. The other information stored is used to reduce the time required to phase lock when the stored phase lock frequency is recalled. There are a total of nine storage registers.

PRESS:	STORE ☐	Notice flashing annunciator and current phase lock frequency to 100 Hz resolution.
PRESS:	#	Number key corresponds to the storage register in which the phase lock information is to be stored. The number should be between 1 and 9 inclusively.

RECALL

Enables the counter to perform one of these functions:

1. To display one of the stored phase lock frequencies;
2. To phase lock to one of the stored phase lock frequencies; or
3. To clear a stored phase lock frequency.

TO DISPLAY A STORED PHASE LOCK FREQUENCY

PRESS:	RCL ☐	Notice flashing annunciator and the word **rcl** displayed on the front panel.
PRESS:	#	Number key corresponds to the storage register to be recalled. Notice the stored phase lock frequency to 100 Hz resolution, followed by the storage register number.
PRESS:	CLEAR ☐ DISPLAY	Returns counter to display measurements.

TO PHASE LOCK TO A STORED PHASE LOCK FREQUENCY

PRESS:	RCL ☐	Notice flashing annunciator and the word **rcl** displayed on the front panel.
PRESS:	#	Number key corresponds to the storage register to be recalled. Notice the stored phase lock frequency to 100 Hz resolution, followed by the storage register number.
PRESS:	ø LOCK ☐	The counter will attempt to phase lock to the recalled frequency. If the recalled frequency is outside the frequency range of the current band, the phase lock frequency register will not be altered. Otherwise, the phase lock frequency register will be updated with the recalled frequency.

TO REMOVE A STORED PHASE LOCK FREQUENCY

PRESS:	RCL ☐	Notice flashing annunciator and the word **rcl** displayed on the front panel.
PRESS:	#	Stored phase lock frequency is displayed to 100 Hz resolution followed by the storage register number.
PRESS:	DATA ☐ CLEAR	Stored phase lock frequency is cleared.

TEST SELECTION

The following tests will verify proper operation of most functional areas of the counter. At power on, the counter performs a RAM and PROM check. During these checks dashes are displayed until the checks have been completed.

RAM AND PROM CHECKS:

The processor writes a sequential bit pattern to each RAM location, then independently reads that pattern. Thus each bit in each location is checked. If the RAM check fails the display will show all "E's." This indicates that the RAM or the RAM decoding is faulty.

The PROM check verifies the PROM bit pattern. If the PROM check fails an error message will be displayed. This indicates that the PROM's or the PROM decoding is faulty.

If both RAM and PROM checks are passed, the counter will begin normal operation about one second after turn on. The counter will now display all 0's.

200 MHz SELF TEST

PRESS: [TEST] [0] [1]

Notice display is 200 MHz. This verifies operation of the time base reference and it's associated circuits, the signal selection, the count chain, and the local oscillator.

LED TEST

PRESS: [TEST] [0] [2]

Notice all LED segments and yellow annunciators are lit. This verifies operation of all visual indicators.

LED SEGMENT TEST

PRESS: [TEST] [0] [3]

Notice each segment of each display digit is lit in turn. The sample rate pot will change the rate, and may be adjusted. This checks the segment drivers.

DISPLAY DIGIT TEST

PRESS: [TEST] [0] [4]

Notice all segments of each digit are lit in turn to verify that each digit operates independently. The sample rate pot will change the rate, and may be adjusted.

KEYBOARD TEST

PRESS: [TEST] [0] [5]

Notice display is 05. Press any key and display will indicate a two digit number showing the position of that key within the keyboard matrix thus checking keyboard operations.

TO EXIT TESTS

PRESS: [CLEAR DISPLAY]

To exit a test and return to normal operation.

To exit tests 1 through 4, 6 and 7 one can press any function key. This will exit the test and enter the function selected.

Tests 6 through 11 and 21 are used for calibration and troubleshooting.

MUTUALLY EXCLUSIVE FUNCTIONS

There exists in the counter some functions that are mutually exclusive, i.e., when one is active, the others cannot be active at the same time. The following is a list of such functions.

1. When self test is active, all other functions are inactive. The exception is in TEST 01, the RESOLUTION function continues to stay active. If any key is pushed when the counter is in self test, the TEST function will automatically be terminated.
2. The POWER METER function will be terminated whenever BAND1, 2, or 4 is selected.
3. The SOURCE LOCK function will be terminated when the RESET functions is activated.
4. The counter is not able to phase lock a source and take power readings at the same time. For the SOURCE LOCK and POWER METER functions, the last function to be activated will override the other function. For example, if the POWER METER function is on, and then the SOURCE LOCK function is activated, the POWER METER function will be turned off.

GENERAL PURPOSE INTERFACE BUS

The GPIB interface of the 575B/578B counters is fully compatible with the IEEE 488-1978 standard. With the GPIB interface, the counter can respond to remote control instructions and can output measurement results via the IEEE 488-1978 Bus interface. At the simplest level the counter can output data to other devices such as the HP 5150A Thermal Printer. In more sophisticated systems a calculator or other system controller can remotely program the counter, trigger measurements, and read results. Of course, a calculator or computer adds other benefits to a GPIB based measurement system. The calculator can manipulate data to compute the mean and standard deviation, check for linearity, and compare results to limits, or perform many other functions.

GPIB FUNCTIONS IMPLEMENTED

The GPIB interface function subsets implemented are:

INTERFACE FUNCTION	SUBSET	DESCRIPTION
SOURCE HANDSHAKE	SH1	complete capability
ACCEPTOR HANDSHAKE	AH1	complete capability
TALKER	T5	basic talker, serial poll, Talk Only mode, unaddress if MLA
LISTENER	L3	basic listener, Listen Only mode, unaddress if MTA
SERVICE REQUEST	SR1	complete capability
REMOTE LOCAL	RL1	complete capability
DEVICE CLEAR	DC1	complete capability
DEVICE TRIGGER	DT1	complete capability

REMOTE LOCAL FUNCTION

When the counter changes from LOCAL to REMOTE or vice-versa, all the stored information is retained. The counter will operate in the same state as it was before the change. The only exception is when the counter is in the TEST mode, the TEST function is automatically terminated. When the counter is in REMOTE and LOCAL LOCKOUT is not active, the RESET key on the front panel keyboard acts as the return to local key.

DEVICE CLEAR FUNCTION

When DEVICE CLEAR or SELECTED DEVICE CLEAR GPIB bus command is received, the counter will revert to its power on state. For the counter's power on state, please see section on PROGRAM CODE SET.

DEVICE TRIGGER FUNCTION

When DEVICE TRIGGER GPIB bus command is received, the counter will initiate a new frequency reading cycle. The converter will not be reset. If the counter does not have a converter lock, the DEVICE TRIGGER will not be performed until a converter locked condition exists.

SETTING ADDRESS SWITCH

The counter employs a decimal address switch located inside the unit. This is set for decimal address 19 at the factory. To verify the switch setting without removing the top of the counter, simply initiate test 10; enter 9C04 and read the address on the display. After reading the address, terminate the test by pushing the clear display key.

The address switch is also used to put the counter in the Talk Only (to) or Listen Only (lo) mode. To put the counter in the Listen Only mode simply set the address switch to any number 41 or higher.

The counter can be put in four different modes of operation in the Talk Only mode. The following is a list of the address settings for entering these modes.

ADDRESS	MODE OF OPERATION
32	Continuous output determined by SAMPLE RATE control. Exponent in scientific format.
33	Continuous output - fast active. SAMPLE RATE control inactive. Exponent in scientific format.
34	Continuous output determined by SAMPLE RATE control. Exponent in zero output format.
35	Continuous output - fast active. SAMPLE RATE control inactive. Exponent in zero output format.

NOTE

In the Talk Only or the Listen Only mode, the address of the counter is always automatically set to decimal 0.

DEVICE DEPENDENT DATA INPUT

It takes a specific amount of time for the counter to process the input data (error checking, formatting, changing the mode of operation, etc.). To prevent the data rate of the bus from slowing down while the counter is doing input data processing, the data is accepted as soon as it is available on the bus, and it is temporarily stored in memory. The size of the storage memory is 100 characters.

The users of the GPIB interface need to be aware of the difference between accepting data and complying with it. If the counter is asked to output a reading before it has finished processing the input data, the output will be in error if the operator makes the assumption that the counter is in the mode that was just programmed. To prevent this, sufficient programmed delays must be provided, or use must be made of the counter's Service Request status byte. See Service Request (SR) command description.

GPIB INSTRUCTION FORMAT

<OP CODE> <NUMBER> <TERMINATOR>

OPERATION CODE or OP CODE can take any of the following formats:

<LETTER> <LETTER> or <LETTER> <DIGIT>

Example: FH (Frequency limit high) or B3 (band 3)

The NUMBER portion of the statement can take the form of any of the following:

<SIGN> <DIGIT STRING>

Example: −2457

<SIGN> <DIGIT STRING> · <DIGIT STRING>

Example: −3.483

NOTE: Spaces within the <OP CODE> and <NUMBER> portions of the instructions are always ignored.

The TERMINATOR allows the operator to choose the scale of an input number as well as implement special functions.

TERMINATOR = G/M/K/H/D/P/C/L

G, M, K, H, represent GHz, MHz, kHz and Hz respectively
D = dB, P = clear data, (equivalent to "clear data" key on keyboard)
C = clear display (equivalent to "clear display" key on keyboard)
L = phase lock (equivalent to "ØLOCK" key on keyboard)

FORMAL DEFINITION OF INSTRUCTIONS

<OP CODE> <NUMBER> <TERMINATOR>

<OP CODE> :: = <LETTER> <LETTER> | <LETTER> <DIGIT>

<NUMBER> :: = <SIGN> <DIGIT STRING> |
<SIGN> <DIGIT STRING> · <DIGIT STRING> |
NULL

<TERMINATOR> :: = G | M | K | H | D | P | C | L | NULL

<SIGN> :: = + | − | NULL

<DIGIT STRING> :: = <DIGIT> <DIGIT> <DIGIT> · · · · · · ·

<LETTER> :: = A | B | C | D | E | F | G | H | I | J | K | L | M | N |
O | P | Q | R | S | T | U | V | W | X | Y | Z

<DIGIT> :: = 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 0

PROGRAM CODE SET

Codes underlined indicate start-up conditions. These conditions are set by the device clear or selected device clear, or power on.

DISPLAY

DA - Display Active: Output Frequency Reading to Front Panel and Bus
DP – Display Passive: Output Frequency Reading to Bus only
DN – Display Normal

BAND

B1 – Band 1: 10Hz - 100MHz
B2 – Band 2: 10MHz - 1GHz
B3 – Band 3: 1GHz - 20 GHz (Model 575B /26.5 GHz (Model 578B)
B4 – Band 4: (Model 578B / Option 06)

RESOLUTION

R0 – Resolution 0 = 1Hz
R1 – Resolution 1 = 10Hz
R2 – Resolution 2 = 100Hz
R3 – Resolution 3 = 1KHz
R4 – Resolution 4 = 10KHz
R5 – Resolution 5 = 100KHz
R6 – Resolution 6 = 1MHz
R7 – Resolution 7 = 10MHz
R8 – Resolution 8 = 100MHz
R9 – Resolution 9 = 1GHz

MEASUREMENT FUNCTIONS

FA – Fast Active (Ignore sample rate Pot)
FP – Fast Passive (Terminates FA)
RS – Reset Basic Counter and Converter. Take a new reading after reset.
HA – Hold Active
HP – Hold Passive

DATA MANIPULATION FUNCTIONS

FO – Frequency Offset. Take a new reading after data entry if counter not in hold.
PO – Power Offset. Take a new reading after data entry if counter not in hold.
*OA – Offset Active:
–Add Frequency Offset to Frequency Reading
–Add Power Offset to Power Reading if Power Meter Function is active
OP – Offset Passive (Terminates OA)
ML – Multiplier. Multiplies frequency readings by an integer number.

*In Start-up Condition, although OA is Active, "0" (zero) Frequency and Power Offsets are programmed.

POWER METER

PA – Power Meter Option Active. Initiate a new gate.
PP – Power Meter Option Passive (Terminates PA)

*MEASUREMENT PARAMETERS

FH – Frequency Limit High. Basic counter and converter will be reset after data entry.
FL – Frequency Limit Low. Basic counter and converter will be reset after data entry.

SOURCE LOCKING FUNCTIONS

PF – Phase lock frequency. Counter attempts to phase lock after data entry.
PL – Initiates phase lock sequence. Equivalent to PHASE LOCK key on keyboard.
BW – Bandwidth. Selects phase lock loop bandwidth.
ST – Store. Equivalent to STORE key on keyboard.
RC – RECALL. Equivalent to RECALL key on keyboard.
CA – Coarse tune active. Source lock process operates normally.
CP – Coarse tune passive. Source lock process bypasses coarse tune process for faster source lock time.

SELF-TEST FUNCTIONS

TA – Test Active.
TP – Test Passive. (clear test function)

DATA FORMAT

EZ – Exponent Zero
ES – Exponent Scientific

DATA OUTPUT

BR – Output both frequency and power readings
FR – Output frequency readings only
PR – Output power readings only

SERVICE REQUEST

SR – Service request enable

DAC OPTION

DC – Select DAC option

---

*Measurement parameters: Standard Software
Limits of 950MHz (LOW) and 18.5GHz (HIGH) (27GHz for Model 578) are featured in each counter at turn on.

DESCRIPTION OF AVAILABLE COMMANDS

DISPLAY

DA — Display Active - Outputs readings to both front panel and GPIB bus.

DP — Display Passive - Outputs readings to GPIB bus only. It will decrease the cycle time of the counter.

DN — Display Normal - Resets display only; used for clearing error messages on the display. Cannot be used after verifying preprogrammed data such as Frequency Offsets or Frequency Limits. This OPCODE affects only the display.

BAND

B1 — Selects Band 1.
B2 — Selects Band 2.
B3 — Selects Band 3.
B4 — Selects Band 4. See Option 06.

RESOLUTION

R0 thru
R9 — Resolution 0 thru 9 — Picks the front panel resolution from 1Hz to 1GHz. Also chooses gate time which is related to resolution: 1Hz = 1 Sec, 10Hz = 100 Sec. 100Hz = 10 msec. 1kHz to 1GHz = 1 msec.

MEASUREMENT FUNCTIONS

FA — Fast Active - Causes the counter to go into the fast cycle mode of operation. In this mode, the front panel sample rate/hold control is inactive and the fastest sample rate is attained. The counter will not go into the Fast Active mode of operation until Hold Active is disabled.

FP — Fast Passive - Terminates FA.

RS — Reset Basic Counter and Converter - Reacquires input signal and takes a new reading. Has the same function as manual reset button.

HA — Hold Active - The counter stops taking readings and the last frequency and power readings are displayed and held. The counter can be directed to take one reading when it is in this mode by sending Device Trigger or Selected Device Trigger GPIB bus command to the counter. It will also update the reading if the RS mnemonic is received.

HP — Hold Passive - Terminates HA.

DATA MANIPULATION FUNCTIONS

FO — Frequency Offset - Enables entry of frequency offsets. (1 Hz resolution available.) A new gate will be initiated after data entry if counter is not in HOLD.

PO — Power Offset - (See option 02.)

OA — Offset Active - Add frequency offset to frequency readings. Add power offset to power readings if power meter function is active.

OP — Offset Passive - Does not add frequency and power offset to readings.

ML — Multiplier - Enables entry of a 2-digit frequency readings multiplier. The multiplier must be an integer between 00 and 99. The results are to 1kHz resolution. A new reading will be initiated after the data entry if the counter is not in HOLD. If the results of the multiplications are larger than, or equal to 999.999, 999, 000 GHz, the counter will output 999.999, 999, 000 GHz to the bus if asked to output readings.

POWER METER

PA – Power Active (See option 02).

PP – Power Passive (See option 02).

MEASUREMENT PARAMETERS

FH – Frequency Limit High - Enables entry of frequency limit high (10 MHz resolution available). The basic counter and converter will be reset after the data entry.

FL – Frequency Limit Low - Enables entry of frequency limit low (10 MHz resolution available). The basic counter and converter will be reset after the data entry.

SELF-TEST FUNCTIONS

TA – Test Active – Enables the counter to perform the selected test function by entering TA followed by two digits. When Test 05, 08, 09, or 10 is active and the counter is being asked to output data, the data that is displayed on the front panel is the data being output.

The output data format is as follows:

XXXXXXXXXXXXCRLF

X = alpha-numeric
CR = carriage return
LF = line feed

For detailed descriptions of tests 01 through 09 and test 11, see the section on Keyboard Controlled Circuit Tests.

Test 10 operates in the following manner:

1. To activate Test 10 input TA10.
2. To read the data stored in a specific memory location, input the address of the memory location in a four digit hexadecimal number. Enable the counter to talk and then read data from the counter.
3. To alter the data stored in a certain memory location:

   If 2. has been performed - input the desired data for that memory location.

   If 2. has not been performed - input the memory address, followed by a two digit hexadecimal number.

TP – Test Passive - Terminates test function.

SOURCE LOCKING FUNCTIONS

PF – Phase lock frequency. Enables entry of phase lock frequency to 10 kHz resolution if phase lock frequency is above or equal to 50 MHz, and 2.5 kHz resolution if it is below 50 MHz. The counter will attempt to phase lock after data entry.

PL – Initiates phase lock sequence. The counter will attempt to phase lock to the frequency specified in the phase lock frequency register.

BW – Bandwidth. Enables the selection of the phase lock loop bandwidth. To select the desired bandwidth, input BW followed by one decimal digit. The digit has to be between 0 and 3 inclusively.

BW 0 = automatic loop bandwidth selection.
BW1 = 500 Hz loop bandwidth.
BW2 = 2 kHz loop bandwidth.
BW3 = 10 kHz loop bandwidth.

In BW0, the counter will try to close the phase lock loop in 10 kHz, 2 kHz and 500 Hz loop bandwidth sequentially. It will select the first bandwidth in which it is able to close the phase lock loop.

ST – Store. Enables the storage of the current phase lock frequency along with other important information related to phase locking that frequency. To store the current phase lock frequency, input ST followed by one decimal digit between 1 and 9 inclusively. The function can be activated only after the counter has been phase locked.

RC – Recall. Enables the recall of the information in one of the storage registers. Inputting RC, followed by one decimal digit between 1 and 9 inclusively, and terminating the string by the terminator L, enables the counter to attempt to phase lock to the frequency stored in one of the storage registers. Terminating the string by the terminator P will clear that storage register.

CA – Coarse tune active. Source lock process operates normally. The counter first goes through the coarse tune process to move the signal source's output to within 5 MHz of the desired frequency. Then the phase lock process takes over to attempt to close the phase lock loop. In this mode, the counter will perform properly even if the coarse tune output of the counter is not connected to the signal source.

CP – Coarse tune passive. Source lock process bypasses the coarse tune process for faster source lock time. This mode can be used if the source's output is close to the desired frequency.

DATA FORMAT

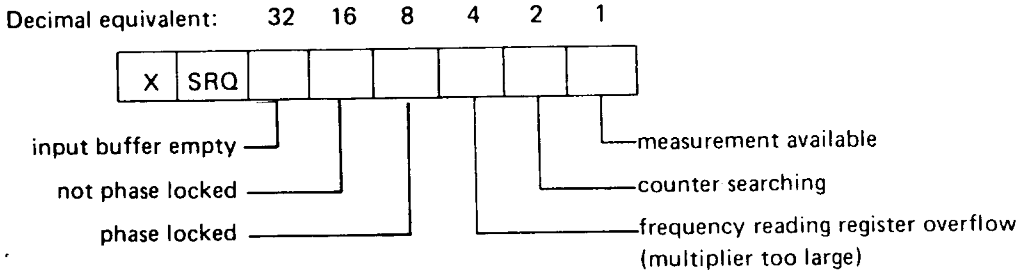
EZ – Exponent Zero - output format.
ES – Exponent Scientific - output format.

DATA OUTPUT

BR – Output both frequency and power readings. (See section on output data format.)
FR – Output frequency readings only. (See section on output data format.)
PR – Output power readings only. (See section on output data format.)

SERVICE REQUEST

SR – Service Request Enable - Enables the counter to send Service Request to the bus when a certain event has taken place in the counter. To enable the function, input SR followed by two decimal digits. The two digits are the decimal equivalent of the content of the eight bit status register. More than one bit of the status register can be set.



To disable the Service Request function, input SR00.

NOTE

Even when the Service Request function is disabled, the Service Request status byte will still be continuously altered to reflect the internal states of the counter.

EXAMPLE: To enable service request on measurement available or input buffer empty, send SR33.

DAC OPTION

DC – DAC Option (See option 01).

DATA OUTPUT FORMAT

The 575/578 transmit the following string of characters to output a measurement.

Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Format																		
EZ (Exponent Zero)	ƀ	±	D	D	D	D	D	D	D	D	D	D	D	D	E	0	CR	LF
ES (Exponent SCI)*	±	D	D	D	D	D	D	D	D	D	D	D	D	D	E	D	CR	LF
Power**	ƀ	ƀ	ƀ	ƀ	ƀ	ƀ	ƀ	ƀ	ƀ	ƀ	±	D	D	D	.	D	CR	LF

Freq. + Power
- FREQ in EZ mode: ƀ ± D D D D D D D D D D D D E 0 , ƀƀƀƀƀƀƀƀƀƀ ± D D D . D CR LF
- FREQ in ES mode: ± D D D D D D D D D D D D D E D , ƀƀƀƀƀƀƀƀƀƀ ± D D D . D CR LF

When the counter is in Test 05, 08, 09, or 10, the output will reflect the data on the display. The format is as follows:

XXXXXXXXXXXXCRLF.

ƀ = Blank
D = Digit
X = Alpha-numeric
CR = Carriage Return
LF = Line Feed

*in Exponent Scientific one digit represents the position of the decimal point. Exponent digit can be either 0, 3, 6, or 9.

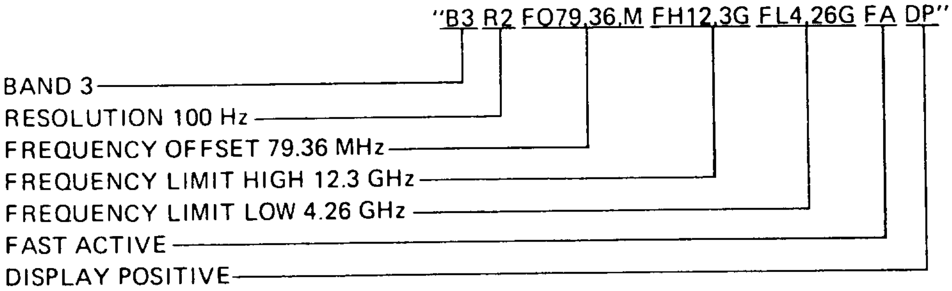
**The power information always have the decimal point fixed for 0.1dB resolution.

Under different output modes, the following counter outputs can be expected by a listener.

OUTPUT MODE	COUNTER OPERATING MODE	OUTPUT
BR	PA	FREQ + PWR
	PP	FREQ
	TA01	FREQ
FR	PA	FREQ
	PP	FREQ
	TA01	FREQ
PR	PA	PWR
	PP	−999.9
	TA01	−999.9
BR, FR or PR	TA 05, 08, 09, or 10	Data on front panel display

PROGRAM EXAMPLES

The examples given here assume an address setting of decimal 19 or ASCII talk address "S" and listen address "3" for the counter. By addressing the counter to listen and sending the following program string, it sets up the following measurement conditions.



"B3 R2 FO79.36.M FH12.3G FL4.26G FA DP"

BAND 3
RESOLUTION 100 Hz
FREQUENCY OFFSET 79.36 MHz
FREQUENCY LIMIT HIGH 12.3 GHz
FREQUENCY LIMIT LOW 4.26 GHz
FAST ACTIVE
DISPLAY POSITIVE

The following programs illustrate how controllers function with the counter. These programs cause the counter to make a series of frequency measurements. The calculators read the measurements into memory and print the results. The programs assume the counter Talk and Listen address is decimal "19."

```
HP 9825A   0:   dim A (10)
           1:   rem 7
           2:   wrt 719, "B3R2FO-4.55M"
           3:   wait 300
           4:   for I = 1 to 10
           5:   red 719, A (I)
           6:   prt A (I)
           7:   next I
           8:   end
HP 9845A  10:   OUTPUT 719, "B3R2FO - 4.55M'
          15:   WAIT 300
          20:   INPUT 719, A
          30:   PRINT "Frequency minus offset equals," A
          40:   GOTO 20
TEK 4051  10:   PRINT @ 19: "B3R2FO - 4.55M"
          20:   INPUT @ 19: A
          30:   PRINT "Frequency minus offset equals, "A
          40:   GOTO 20
```

The 9825A program will cause the counter to take a series of ten readings, print them on the 9825A paper tape and stop. Notice that an offset of 4.55 MHz is subtracted from each reading.

The program shown for the 9845A and TEK 4051 cause the counter to make a frequency measurement and print that measurement. To end the program, initiate a "STOP" command. This is accomplished on the 9845A with the key labeled "STOP." On the TEK 4051 use the key labeled "BREAK." To restart the program enter the RUN statement followed by the line number that is printed in the INTERRUPT message.

READING A MEASUREMENT

To read a measurement from the counter to a calculator, the counter must first be addressed to talk and the calculator to listen. The examples below indicate how a calculator may read a measurement from the counter.

```
10 red 719, A    }                10 INPUT @ 19:A  }
                 }  HP 9825A                       }  TEK 4051
20 prt A         }                20 PRINT A       }

10 ENTER 719, A  }
                 }  HP 9845A
20 PRINT A       }
```

The EIP counters can use two different modes. HA which takes one reading then waits for a reset command or a Device Trigger GPIB Bus Command. In this condition the counter is sent a reset or Device Trigger and (when addressed to talk) a new reading is output to the BUS. The counter will hold that particular reading on the display until another reset command or Device Trigger command is received. The other mode is HP or HOLD PASSIVE. In this mode data is read out in a normal BUS fashion. The display automatically updates corresponding to the sample rate chosen. In this condition successive readings can be output without generating a reset or Device Trigger command each time.

** ADDRESS CHARACTERS		ADDRESS CODES					
Listen	Talk	binary					decimal
		5	4	3	2	1	*
SP	@	0	0	0	0	0	00
!	A	0	0	0	0	1	01
''	B	0	0	0	1	0	02
#	C	0	0	0	1	1	03
$	D	0	0	1	0	0	04
%	E	0	0	1	0	1	05
&	F	0	0	1	1	0	06
'	G	0	0	1	1	1	07
(	H	0	1	0	0	0	08
)	I	0	1	0	0	1	09
*	J	0	1	0	1	0	10
+	K	0	1	0	1	1	11
,	L	0	1	1	0	0	12
–	M	0	1	1	0	1	13
.	N	0	1	1	1	0	14
/	O	0	1	1	1	1	15
0	P	1	0	0	0	0	16
1	Q	1	0	0	0	1	17
2	R	1	0	0	1	0	18
3	S	1	0	0	1	1	19
4	T	1	0	1	0	0	20
5	U	1	0	1	0	1	21
6	V	1	0	1	1	0	22
7	W	1	0	1	1	1	23
8	X	1	1	0	0	0	24
9	Y	1	1	0	0	1	25
:	Z	1	1	0	1	0	26
;	[	1	1	0	1	1	27
<	/	1	1	1	0	0	28
=	]	1	1	1	0	1	29
>	∧	1	1	1	1	0	30

* Decimal Talk/Listen Address is provided as a cross reference for those controllers which use decimal address.

** Address characters in ASCII code.

Figure 3-5. Allowable Address Codes

DISPLAY ERROR MESSAGES

When an error occurs an error number will be displayed. The probable cause of each error is listed below.

OPERATOR ERRORS

The following error messages indicate an operator error.

01 Illegal Key Sequence.

02 A resolution number was not entered.

03 A band number was not entered; or the number entered was too large.

04 No power reading in current band.

05 Frequency limit high >18.5 GHz, 27 GHz (578B)

06 (Freq Limit Hi) – (Freq Limit Lo) <100 MHz

07 Frequency Limit Low <.95 GHz (575B/578B).

08

09 Illegal test mode key sequence.

10 Illegal DAC key sequence.

11 Illegal Multiplier key sequence.

12 SERVICE REQUEST condition input error (GPIB only).

13 Option not installed.

14 Phase lock frequency out of range of current band.

15 Cannot store phase lock information. Counter not phase locked.

16 Storage register 0 does not exist.

17 Illegal BANDWIDTH key sequence.

NEW ERROR MESSAGES

ERROR 19 : function not allowed in 0.1 resolution.

ERROR 20 : access to TEST 10 or TEST 90 without privilege.

ERROR 30 : EEPROM error.

ERROR 40 : DAC table error, cannot find YIG frequency.

ERROR 41 : calibration frequency error.

ERROR 42 : signal not found.

COUNTER ERRORS

The following error messages indicate a malfunction within the counter.

31	Check sum error	Section 1 PROM	C000-CFFF	A105, U14
32	Check sum error	Section 2 PROM	D000-DFFF	A105, U13
33	Check sum error	Section 3 PROM	E000-EFFF	A105, U17

Section 4
Theory of Operation

GENERAL

The 575B and 578B counters automatically measure and display the frequency of an input signal within the range of 10 Hz to 20 GHz for the 575B, and 10 Hz to 26.5 GHz for the 578B. They are also able to phase lock the input to the accuracy and stability of the counter's internal time base oscillator. In both models the frequency is divided into three bands.

BAND 1 operates from 10 Hz to 100 MHz. An impedance converter provides an input impedance of 1 M ohm, shunted by 20 pF.

BAND 2 operates from 10 MHz to 1 GHz, using a heterodyne down converter which converts the input signal into an output signal with a range of 10 MHz to 190 MHz.

BAND 3 operates in the microwave range of 1 to 20 GHz (or 26.5 GHz) and uses a YIG tuned heterodyne converter to translate the input frequency downward to an intermediate frequency (IF) of 127 MHz.

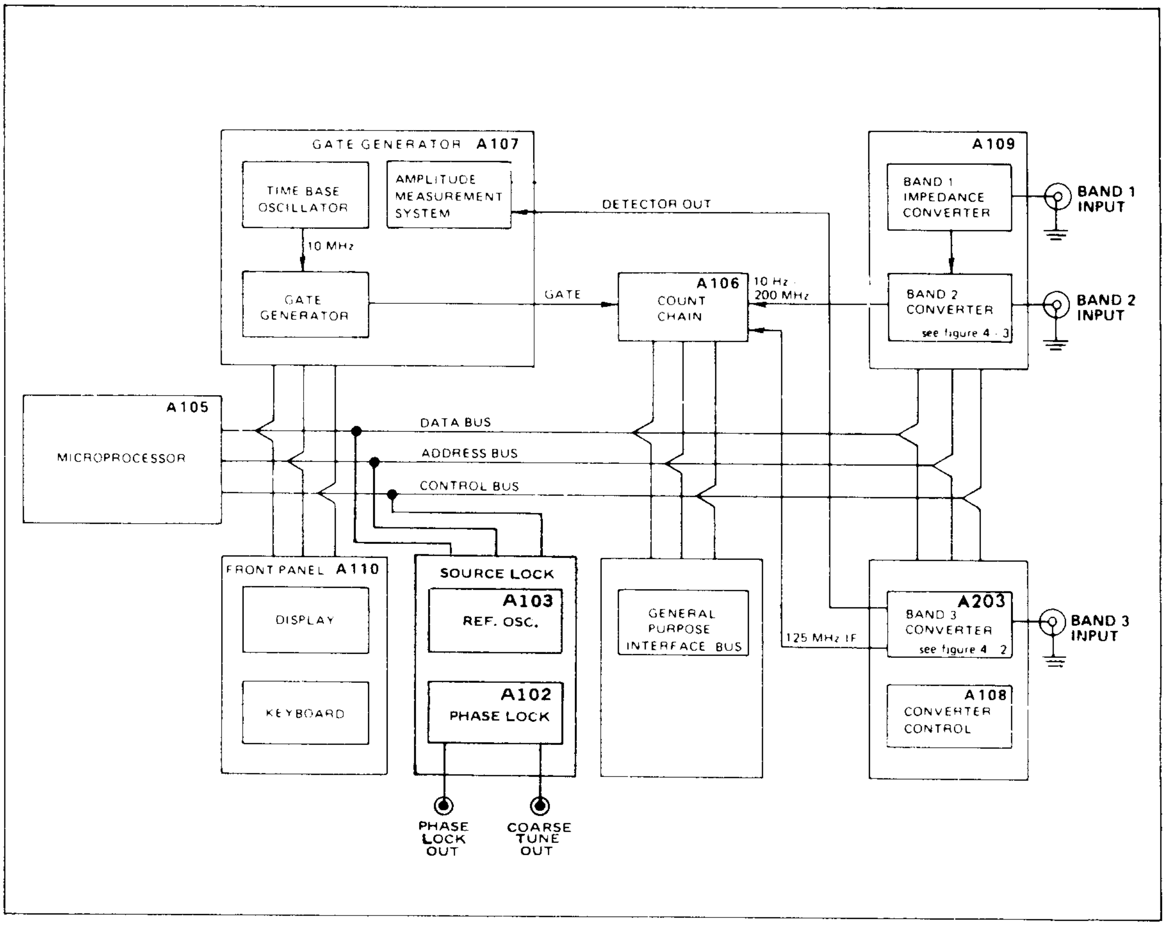


Figure 4-1. Counter Block Diagram, Simplified

BASIC COUNTER

Overall operation is controlled by the Microprocessor Assembly A105. This assembly contains an eight bit microprocessor, its control logic, and the system memory. It communicates with all other assemblies in the instrument by means of a triple bus system: the data, address, and control bus. On each assembly there is a Peripheral Interface Adaptor (PIA) which provides the interface between the bus system and the instrument hardware.

Frequency measurements are performed by comparing an unknown signal to a reference frequency, namely the time base. A 10 MHz crystal oscillator is used as the internal reference and is a part of the Gate Generator Assembly A107. For increased accuracy and stability, ovenized oscillator options are available, or the user may select an external 10 MHz reference.

A frequency measurement is made by generating a time interval (Gate Time) consisting of a number of cycles of the reference. This Gate Time is then used as an interval during which the input signal is counted by the Count Chain Assembly A106.

Initially, the microprocessor selects one of several available inputs to the Count Chain Assembly and the appropriate Gate Time based on user input information; band selection, resolution, etc. The microprocessor then initiates the measurement cycle by resetting the Count Chain to zero and allowing a gate to be generated. During the gate interval, the Count Chain accumulates the number of cycles of the input signal. At the end of the gate time, the microprocessor reads the stored information in the Count Chain and performs any required calculations necessary to convert the measurement into a direct reading of the unknown frequency. The front panel display is then updated with the new measurement results. Figure 4-1 shows a simplified block diagram of the counter.

BAND 2 CONVERTER

An input signal is applied to the mixer along with an appropriate local oscillator (L.O.) to generate an IF frequency in the range of 10 MHz to 190 MHz. This signal is filtered and amplified to a level suitable for direct measurement by the Count Chain.

The L.O. frequency is generated by the Voltage Controlled Oscillator (VCO) of the Band 3 Converter. This frequency is phase locked to the counter's time base and controlled by the microprocessor. A VCO multiplier serves to either pass along the signal directly or double it. It can also turn off the signal and pass only a DC bias to the mixer.

Two detectors provide outputs proportional to the amplitudes of both the applied RF signal and the resulting IF signal. These outputs are compared in the Signal Comparator, which provides a digital output when the IF amplitude exceeds the RF amplitude.

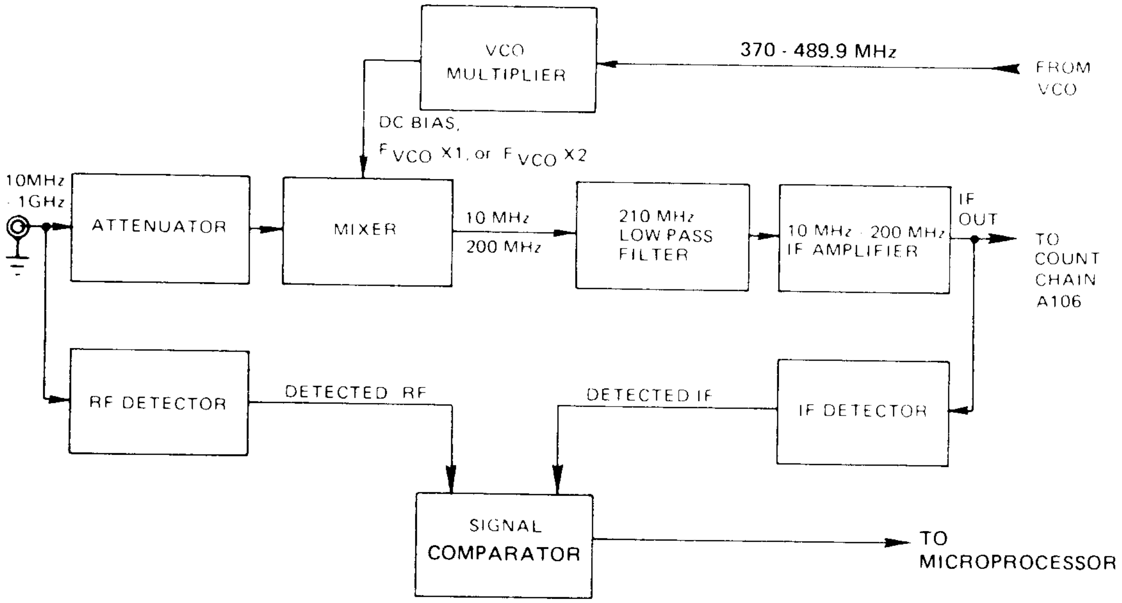


Figure 4-2 Band 2 Converter Block Diagram, Simplified

The output frequency of the system is the difference between the input signal and the L.O. applied to the mixer. Since the L.O. frequency is a harmonic (N) of the VCO frequency, the unknown input frequency can be expressed as $F_{IN}=N\ F_{VCO} \pm F_{IF}$. There are three primary functions of the software operating the converter:

- To select the appropriate harmonic number N.
- To select an appropriate VCO frequency.
- To determine whether the IF frequency is added to, or subtracted from the L.O. frequency.

These functions are accomplished by selecting N and F_{VCO} and looking for an IF signal of the appropriate amplitude and frequency. Overall system gain is such that whenever the correct L.O. frequency is applied, the IF power will exceed the RF power. This is the primary information used in determining the correct VCO frequency and harmonic number. Once an IF is obtained, the harmonic number is verified and the +/- sign in the equation is determined by shifting the VCO frequency and observing the magnitude and direction of the resulting IF shift. Converter operation is diagrammed in figure 4-3.

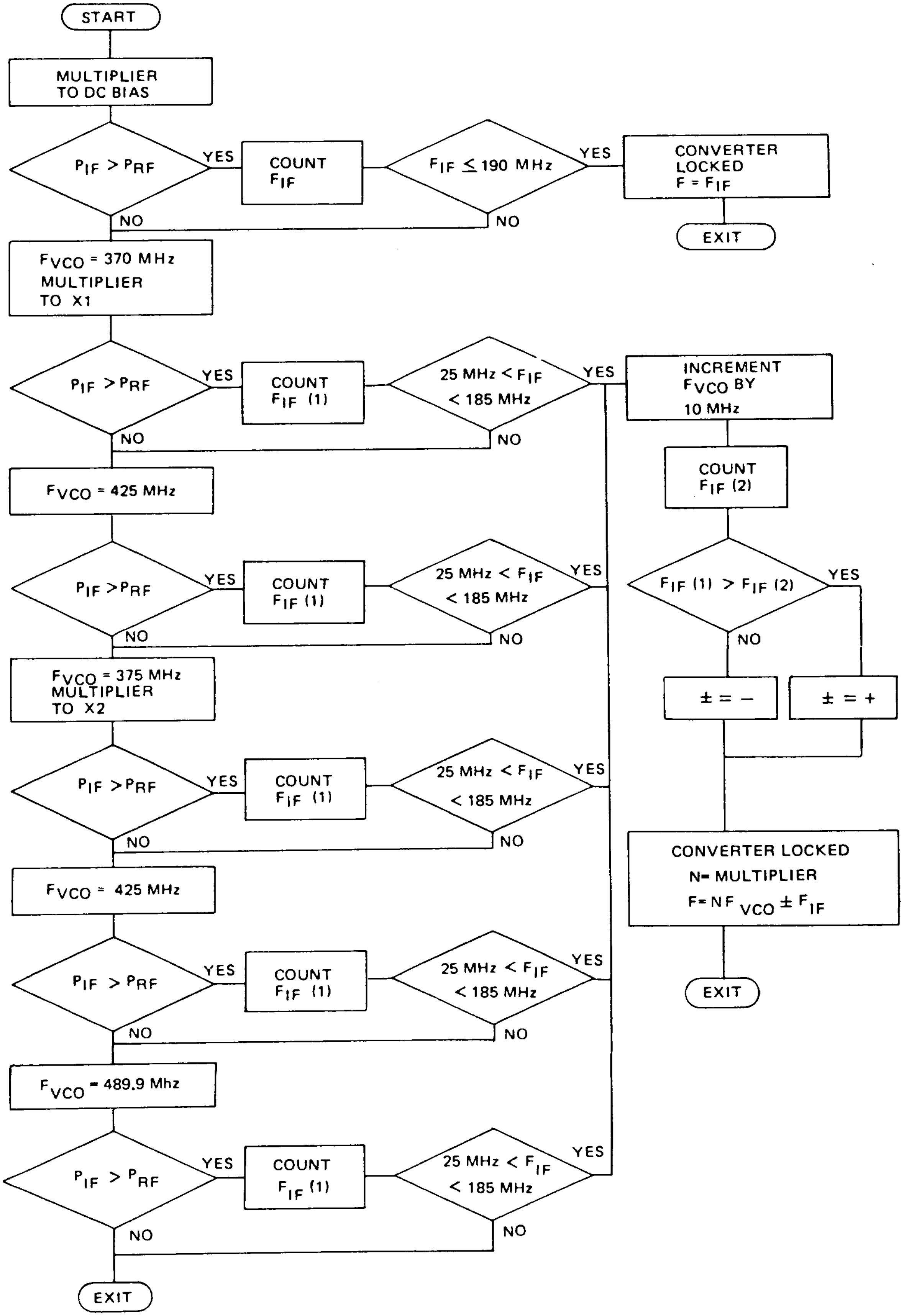


Figure 4-3. Band 2 Converter Operation

The L.O. frequencies being used, except the range of direct counting (< 190 MHz), have been selected so only IF frequencies from 25 MHz to 185 MHz are required. Since the counter can count signals less than 10 MHz, the restricted operating range provides margin for frequency modulation on the input signal, and for incrementing the VCO frequency.

Figure 4-4 shows the operating ranges for the various harmonics and VCO frequencies used.

Input Frequency Range F_{IN}(MHz)	VCO Frequency F_{VCO}(MHz)	Harmonic Number N	IF Frequency Range F_{IF}(MHz)
10 - 190	–	0	10 - 190
185 - 345	370	1	185 - 25
345 - 400	425	1	80 - 25
400 - 560	375	1	25 - 185
560 - 610	425	1	135 - 185
610 - 725	375	2	140 - 25
725 - 825	425	2	125 - 25
825 - 935	375	2	75 - 185
935 - 1035	425	2	85 - 185
1035 - 1164.8	489.9	2	55.2 - 185

Figure 4-4. Band 2 Operating Ranges

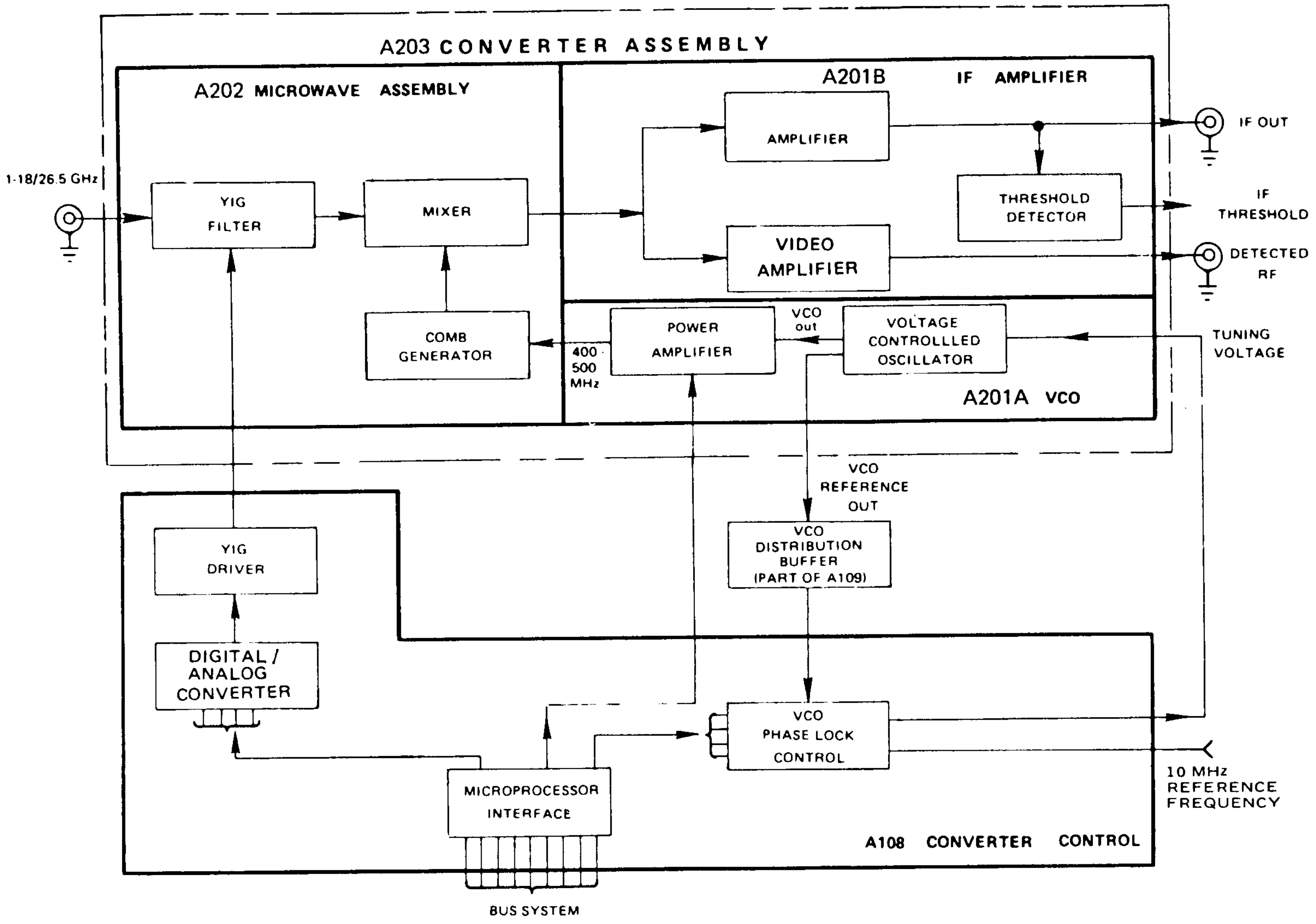


Figure 4-5 Band 3 Converter, Simplified.

BAND 3 CONVERTER

Measurement of a signal in Band 3 is accomplished by down converting from the microwave range to approximately 127 MHz. This is accomplished by mixing the input signal with a known reference frequency which is a harmonic of the VCO. The VCO frequency (400-500 MHz) can be selected in 50 kHz increments by using a microprocessor controlled phase lock system while retaining the accuracy and stability of the counter's time base reference.

A simplified diagram of the Band 3 converter is shown in figure 4-5. There are two major assemblies. The Converter Control assembly (A108) and the Converter Assembly (A203).

CONVERTER CONTROL A108

The Converter Control assembly contains the interface between the microprocessor bus system and the Converter (A203). A digital-to-analog converter and a precision current driver provide a 2 MHz frequency resolution for setting the YIG filter of A202.

A108 also contains the programmable VCO phase lock control system. This system lets the microprocessor interface select any VCO frequency between 400 and 500 MHz, in increments of 50 kHz.

CONVERTER A203

The Converter assembly consists of three subassemblies.

- A201A, Voltage Controlled Oscillator (VCO) Assembly
- A201B, IF Amplifier Assembly
- A202, Microwave Assembly (yig)

The A202 Microwave Assembly contains the YIG filter, mixer and comb generator.

The input signal (1 GHz - 20 GHz/26.5 GHz) passes through a YIG filter on A202. The filter is an electronically tunable bandpass filter, with an operating frequency proportional to its tuning current. This filter determines the approximate frequency of the input signal, and filters out any undesired signals, making it possible to count a signal at one frequency even if a larger signal is present at another frequency.

When tuning the YIG filter to the input signal, the mixer is used as an RF detector, and its output is amplified in the video amplifier on the IF assembly .

The output of the Video amplifier is maximum when the YIG filter is tuned to the input signal. In the case of multiple input signals, the video amplifier output determines which signal is largest.

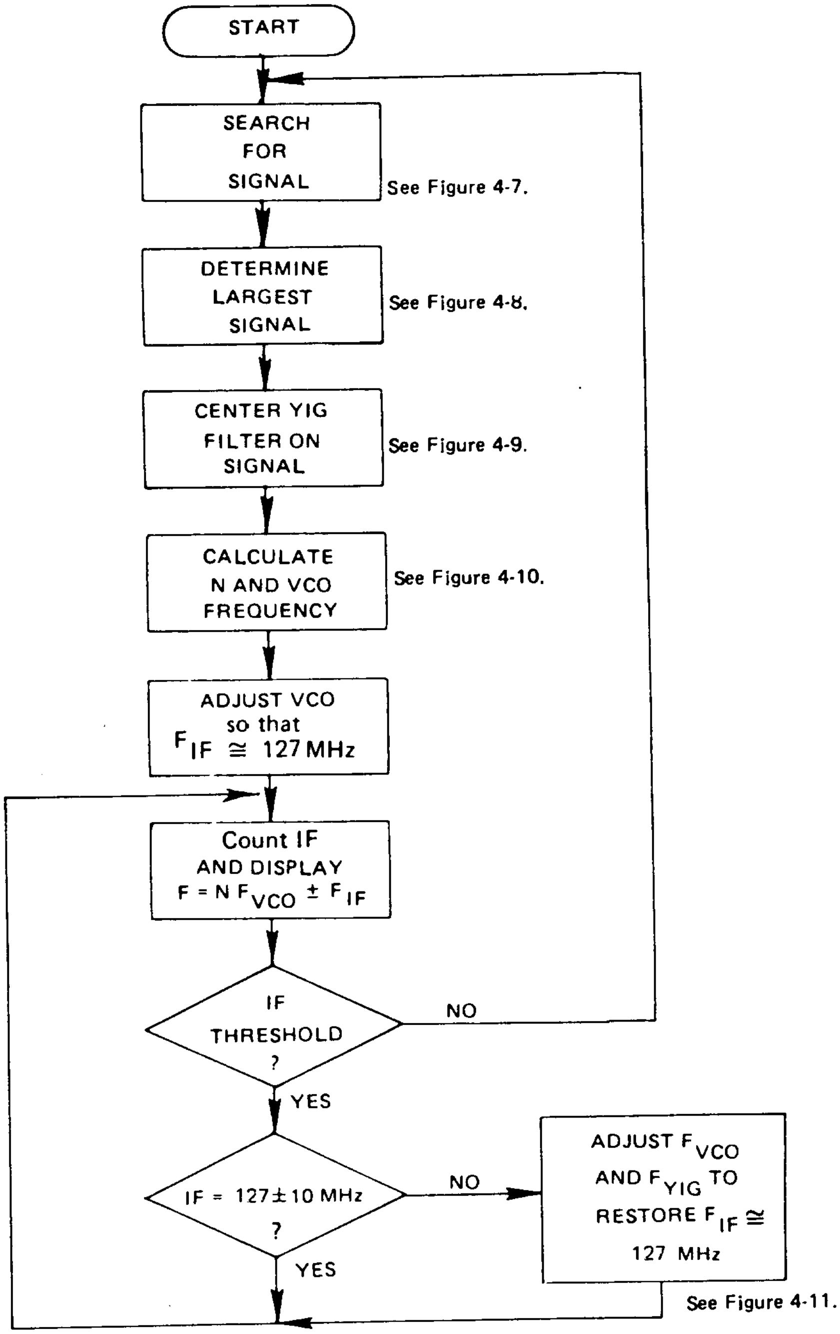


Figure 4-6. Band 3 Operation, Simplified.

On units equipped with the Power Measurement Option (02), accurate frequency correction factors are stored in the counter's memory. This allows absolute power calibration of the video amplifier output.

Once the YIG filter is tuned to the input signal, the appropriate harmonic number (N) and VCO frequency (F_{VCO}) are selected to produce an IF frequency (F_{IF}) at approximately 127 MHz. The input signal is found by using:

$$F_{IN} = N\,F_{VCO} \pm F_{IF}$$

The IF frequency produced in the mixer is amplified by the high gain IF amplifier and sent to the count chain (A106). The IF threshold detector (A201B) insures sufficient IF amplitude for count accuracy.

OPERATION

First the YIG filter is stepped in 64 MHz steps from its low to high limits. During this search the RF detected output is fed, through a microprocessor controlled step attenuator to a threshold detector. After each step the threshold detector is checked. If triggered, the search mode is halted until the amplitude of the signal is determined. This is done by stepping the filter back and forth through the signal and stepping the attenuator until the signal is attenuated below the threshold. The counter then returns to the search mode to look for any larger signals. After searching the entire frequency range, it returns to the largest signal and begins to center the YIG filter precisely on the input frequency. See Figure 4-6 for a simplified diagram of Band 3 operation. For more detailed descriptions of Band 3 operation see Figures 4-7 through Figure 4-11.

The centering process consists of slowly stepping the YIG filter down in 2 MHz increments until a level of 3-6 dB below the peak is reached. This frequency is stored and the process is repeated from the other side by stepping the filter up in 2 MHz steps. The average of the two frequencies obtained is the center of the passband. This is the frequency which is used to determine the N and F_{VCO}.

After centering, N is determined from $N = \frac{F_{YIG} - 127}{500}$ and then rounded up to the next higher integer. From this, F_{VCO} is calculated using $F_{VCO} = \frac{F_{YIG} - 127}{N}$. Should this yield $F_{VCO} < 400$ MHz, then F_{VCO} is recalculated using $F_{VCO} = \frac{F_{YIG} + 127}{N}$.

Since F_{YIG} is only approximately equal to F_{IN}, the IF frequency will not be exactly 127 MHz. Therefore, the next step in the operation is a VCO frequency adjustment to shift F_{IF} into the middle of the IF passband.

VCO frequency correction is achieved by counting F_{IF} and changing F_{VCO} by $\pm \frac{F_{IF} - 127}{N}$. If the error is large enough to be outside the IF passband (IF threshold is not triggered) then a series of steps (shifting the IF in ± 20 MHz increments) are taken until the signal falls within the passband.

Once the VCO corrections have been made, the converter has acquired the signal and the counter is ready to count and display the input frequency.

After each measurement, the frequency of the IF is examined. If the input frequency has shifted more than 10 MHz, new frequencies for the YIG and VCO are calculated to restore the IF to 127 MHz. This method provides rapid tracking of a signal being tuned.

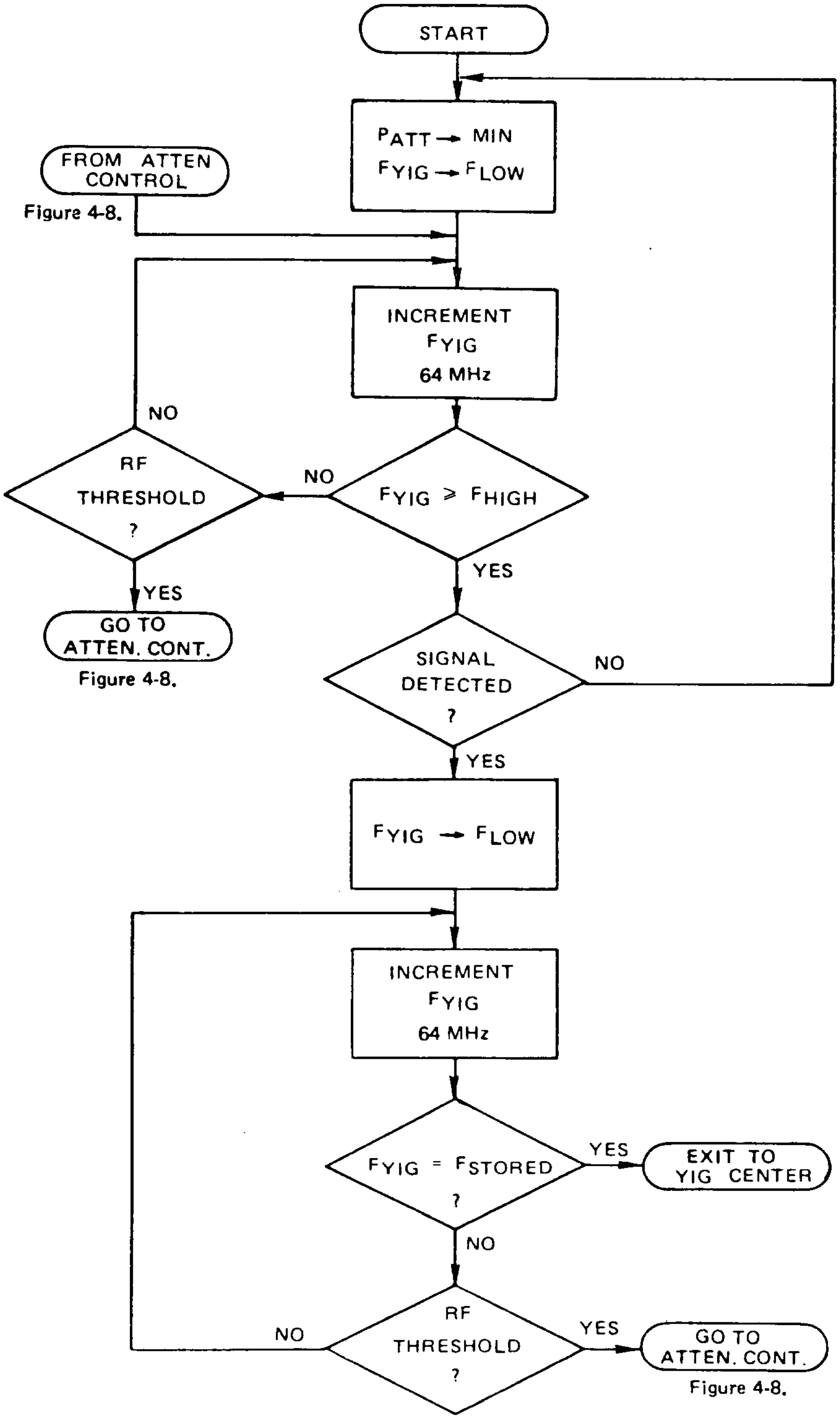
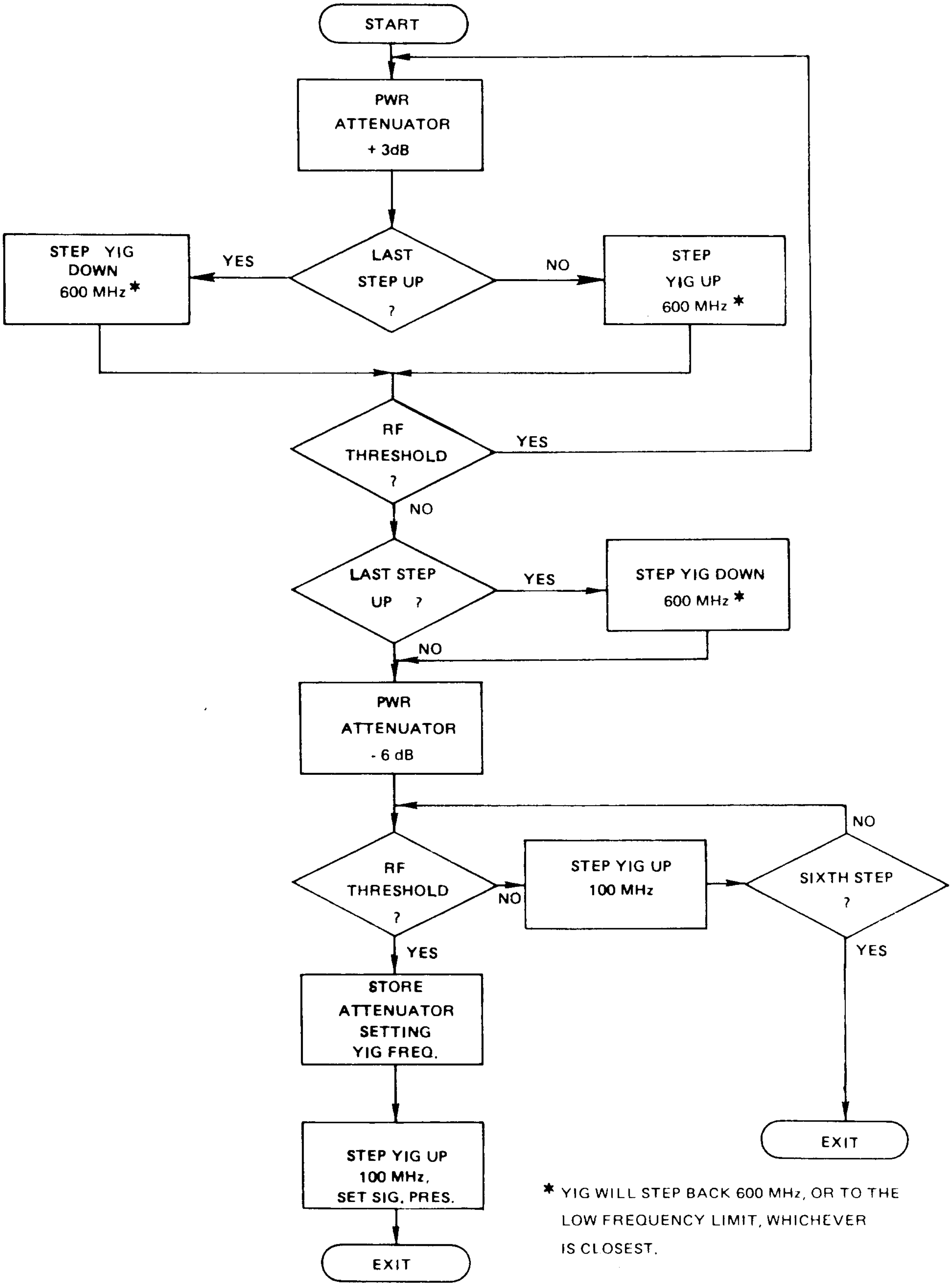


Figure 4-7. Band 3 Search For Signal



* YIG WILL STEP BACK 600 MHz, OR TO THE LOW FREQUENCY LIMIT, WHICHEVER IS CLOSEST.

Figure 4-8. Determine Largest Signal

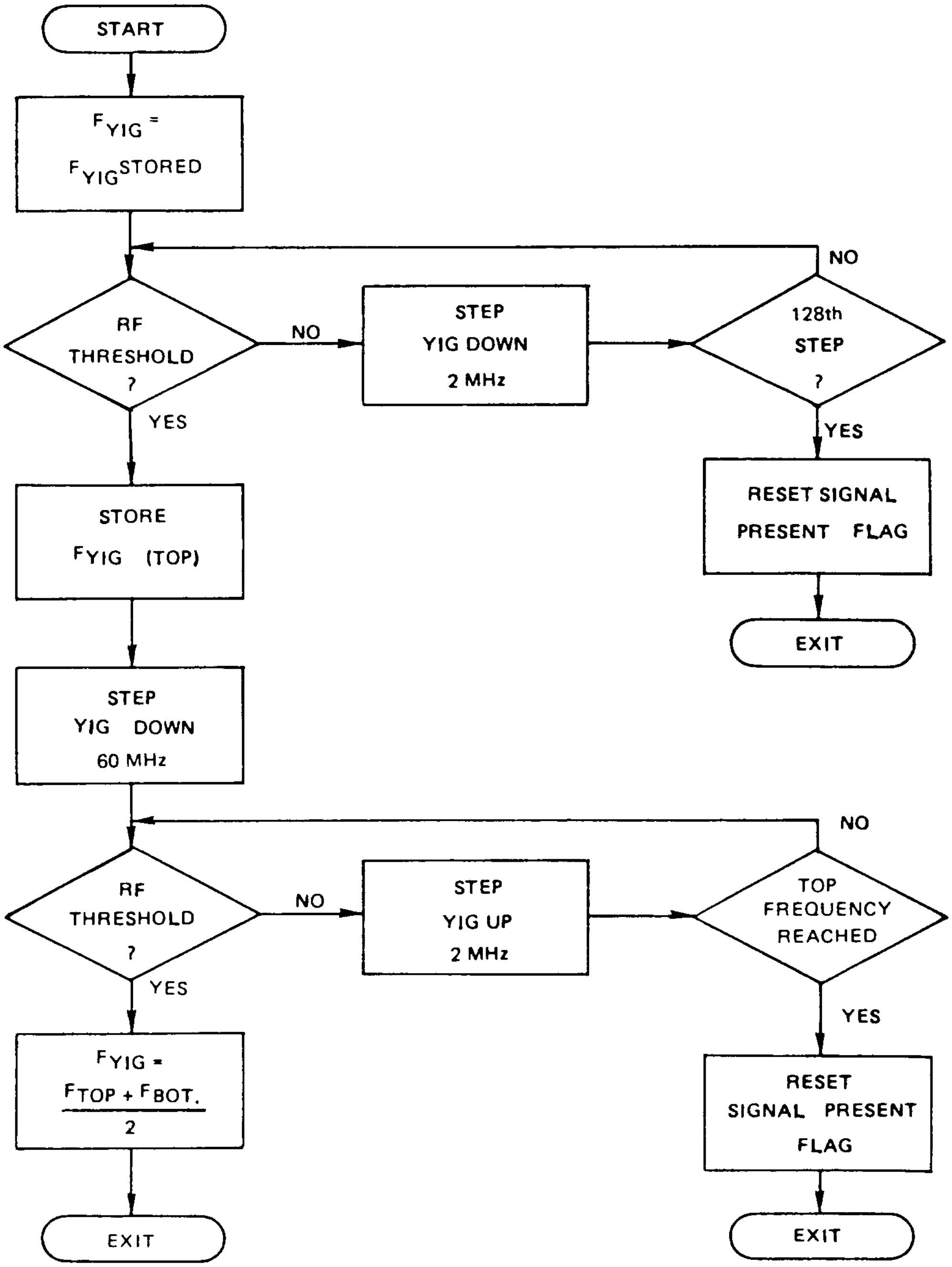


Figure 4-9. YIG Centering

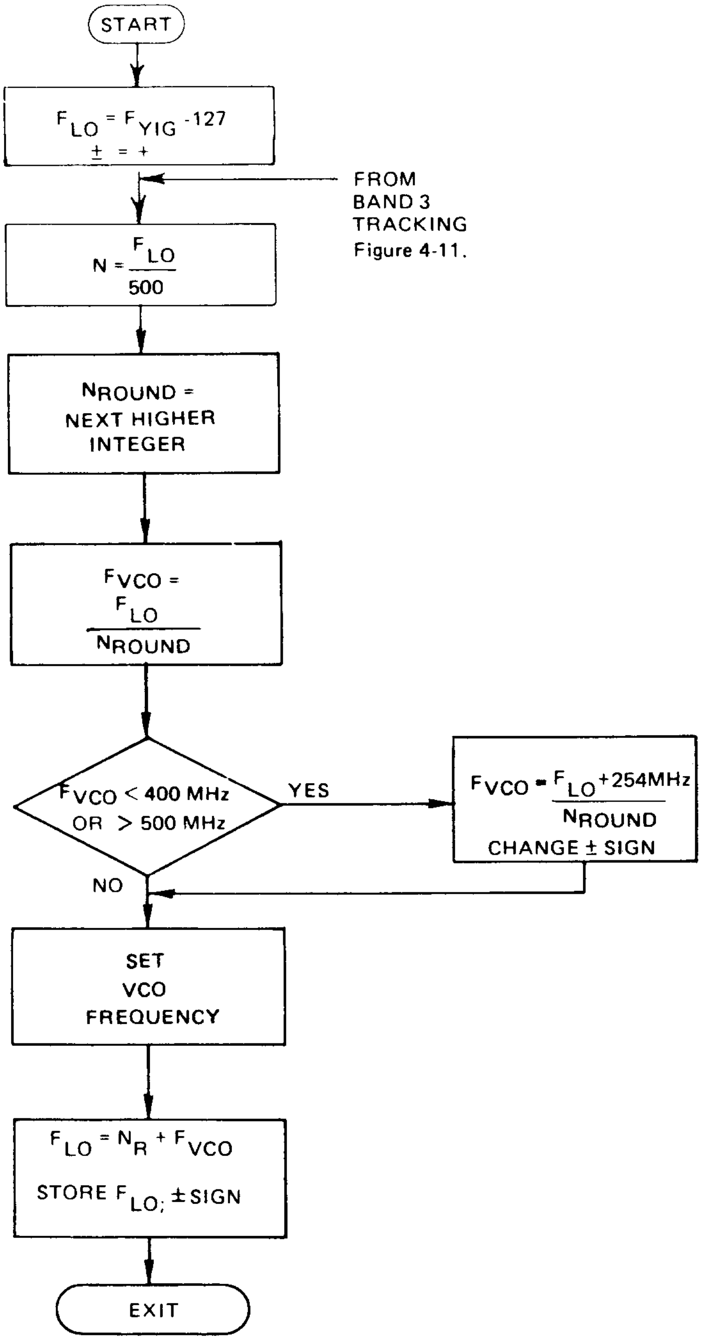


Figure 4-10. Calculate N and VCO Frequency

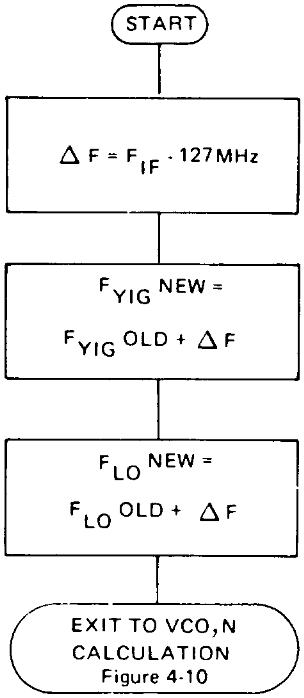


Figure 4-11. Band 3 Signal Tracking

SOURCE LOCK

The counter source locks in two main steps: coarse tune and phase lock. Coarse tune sets the input frequency within 5 MHz of the desired phase lock frequency. Phase lock then locks the input to the time base oscillator. A block diagram of the source lock system is shown in figure 4-12.

REFERENCE LOOP

The reference loop provides the reference frequency to the phase lock board. The reference loop output is phase locked to the counter's time base. The microprocessor sets the reference loop between 10 and 50 MHz with a 2.5 kHz resolution.

COARSE TUNE

The 14 bit coarse tune DAC is driven directly by the microprocessor and provides an output voltage variable from 0 to 10.2 V.

PHASE LOCK

The phase detector compares the I.F. frequency to the reference frequency and provides an output voltage relative to the phase difference of the two inputs. To keep the I.F. to the phase detector between 10 and 50 MHz a ÷ 4 is switched in at frequencies greater than 50 MHz. The phase detector output drives a programmable attenuator, used to compensate for different source gain constants. The integrator sets one of three bandwidths, selected by the microprocessor.

The output driver was designed to be a resistive voltage source, capable of driving ± 10 V into a high impedance or ± 75 MA into a low impedance.

SHALLOW SEARCH

The Source Lock process requires the microprocessor to directly vary the output voltage. To accomplish this the phase lock loop is disconnected and the integrator is connected to the 8 bit shallow search DAC.

SOFTWARE

The Source Lock software contains two main routines called by the Source Lock Driver. They are Coarse Tune and Phase Lock. In addition the Source Lock Driver controls recall of stored data and loss of source lock routines (See figure 4-13).

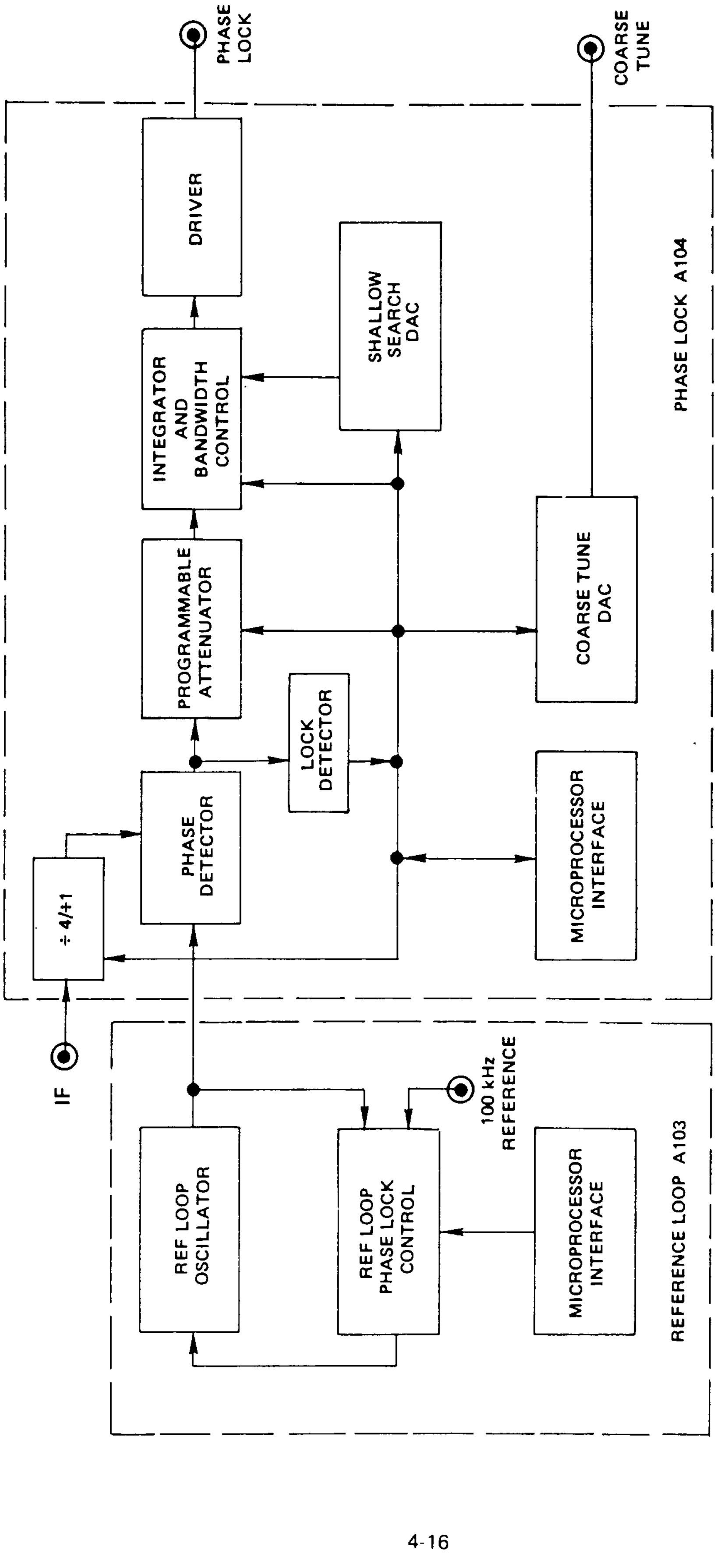


Figure 4-12. Source Lock Block Diagram

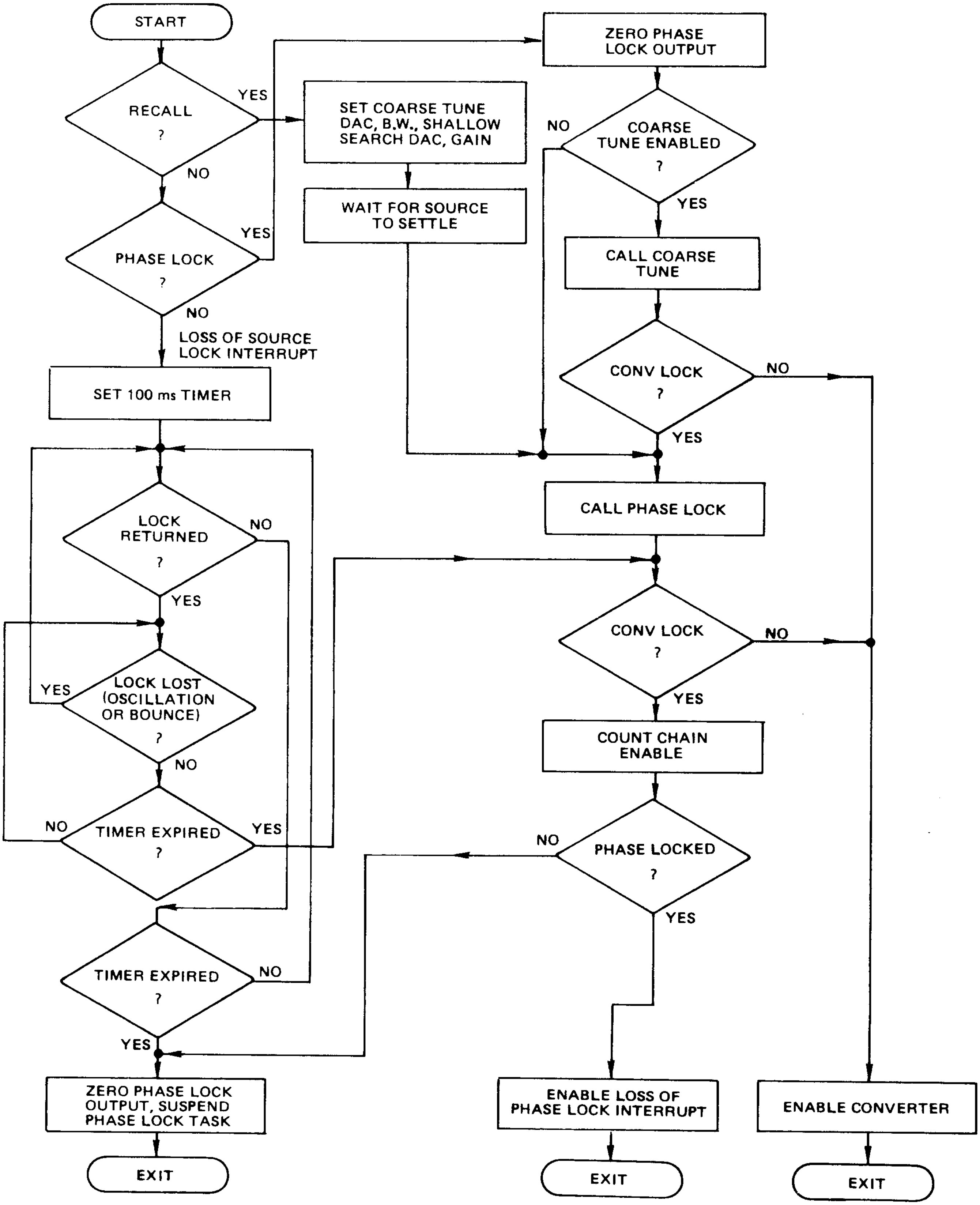
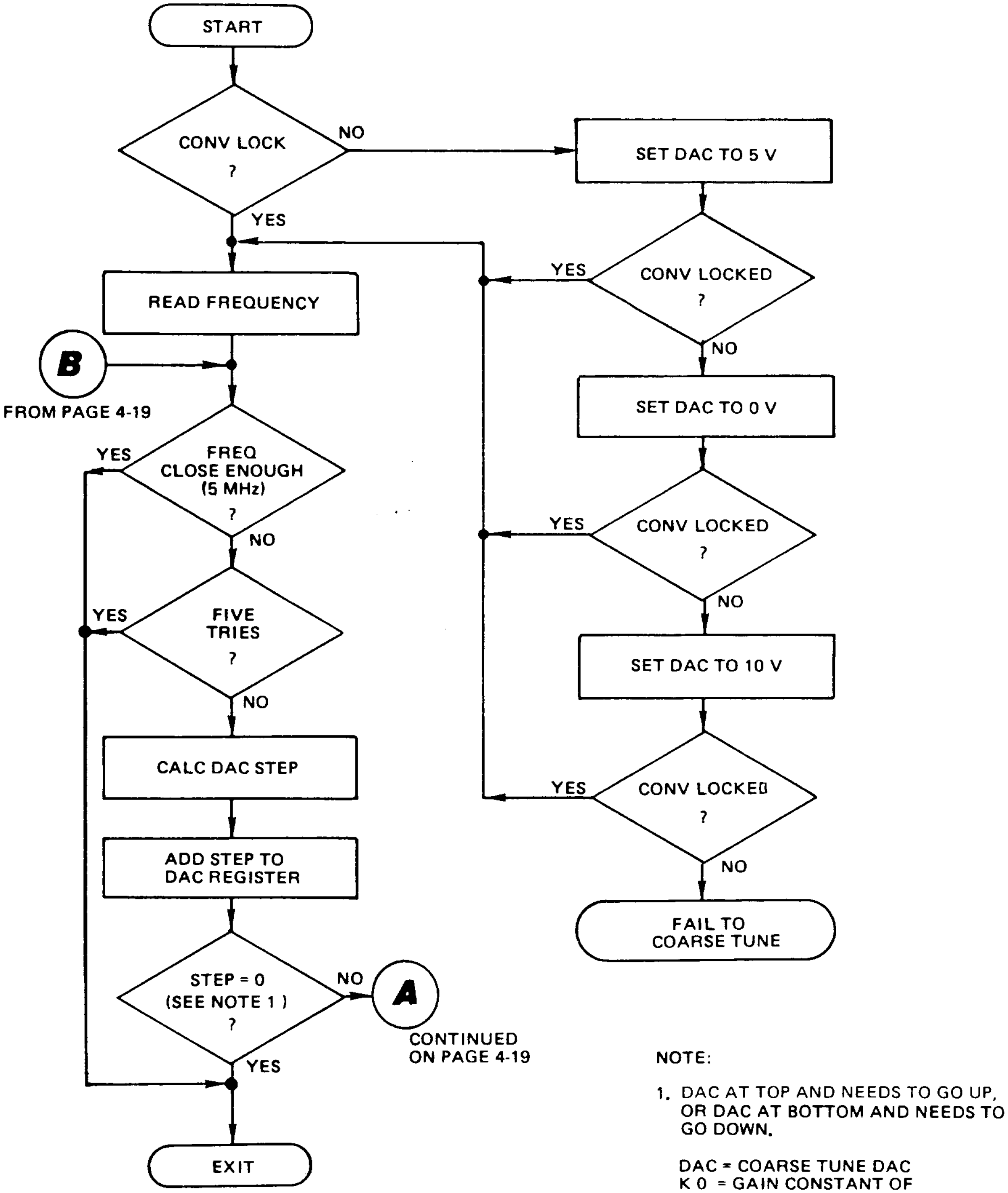


Figure 4-13. Source Lock Driver



NOTE:

1. DAC AT TOP AND NEEDS TO GO UP, OR DAC AT BOTTOM AND NEEDS TO GO DOWN.

DAC = COARSE TUNE DAC
K 0 = GAIN CONSTANT OF COARSE TUNE INPUT ON SOURCE

Figure 4-14. Coarse Tune Flow Diagram

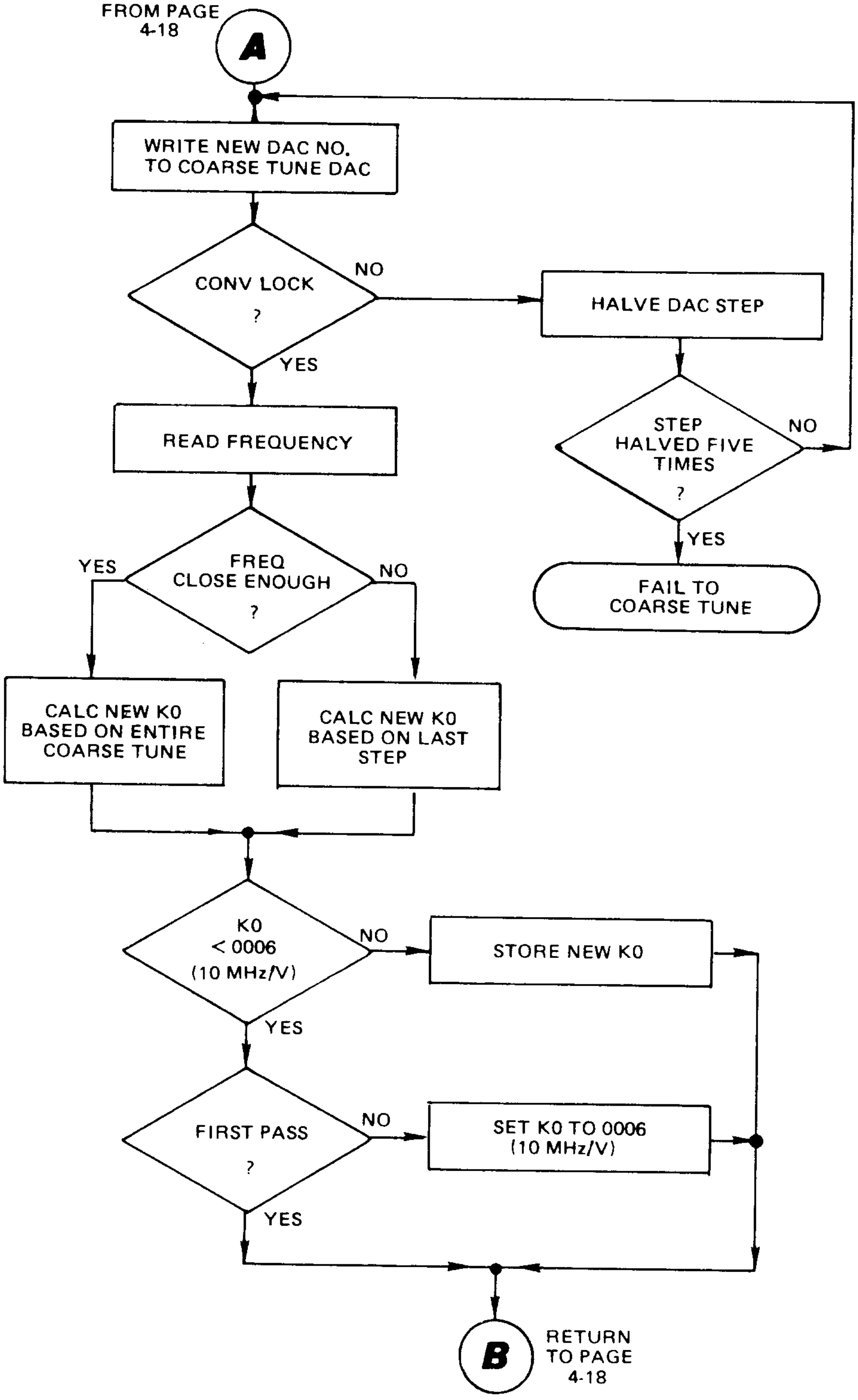


Figure 4-14. Coarse Tune Flow Diagram, continued

COARSE TUNE

Coarse Tune will set the frequency of the source within 5 MHz of the desired frequency.

When called, coarse tune first checks for converter lock (Aquisition of valid signal). If no converter lock exists, the coarse tune DAC is set to 5 V, 0 V, and 10 V respectively. If no converter lock can be achieved the lock sequence is aborted.

When converter lock is acquired the input frequency is read. If the input frequency is within 5 MHz of the desired frequency coarse tune returns to the Driver Program. If not, the step size is calculated using the following formula:

$$\frac{Fd - Fb}{K0} = \text{DAC STEP}$$

Where:
Fd = Desired Source Lock Frequency
Fb = Beginning Frequency
K0 = Source gain constant calculated by last coarse tune step.

If the coarse tune output is maximum and the step is calculated to be positive, or the coarse tune output is zero and the step is calculated to be negative, coarse tune is aborted. The lock sequence, however, is not aborted. If the step is valid, the output is stepped and the counter waits for the source to settle to the new frequency. If, after waiting, converter lock cannot be achieved (the source stepped out of range, or into a dead band) the DAC step is halved and the process repeated.

After the source has settled to a new, valid frequency the gain constant is calculated using the following formula:

$$\frac{Fn - Fb}{\text{DAC STEP}} = K0$$

Where:
Fn = New Frequency
Fb = Beginning Frequency
K0 = New Source gain constant to be used in next coarse tune step.

The gain constant is justified to be greater than 10 MHz/V and less than 25 GHz/V and the entire process is repeated.

Using this process the coarse tune routine can learn the gain constant of the source, requiring minimum amount of time to coarse tune linear sources, but still maintaining the capability to coarse tune non-linear sources.

PHASE LOCK

The Phase Lock portion of the source lock software performs the following tasks sequentially:

1. Checks if input signal is within 50 MHz of desired frequency. Tunes source with the shallow search DAC if input signal is not close enough.
2. Determines the dynamic gain constant and polarity of the source.
3. Sets the YIG and local oscillator of the counter to the desired frequency.
4. Sets the phase lock loop attenuator and reference loop.
5. Tunes the source with the shallow search DAC until an IF exists.
6. Sets the loop bandwidth and polarity of the phase lock loop.
7. Closes the phase lock loop. Checks for phase locked condition.

Detailed descriptions of each step in the phase lock process are as follows:

INPUT SIGNAL FREQUENCY CHECK

Under normal conditions, converter lock should exist when the phase lock program is activated. In cases where converter lock does not exist, the phase lock program will try to obtain a converter lock by enabling the converter lock program. If converter lock cannot be achieved, the phase lock process will be repeated indefinately until cancelled.

If the coarse tune input is connected and the counter is in the COARSE TUNE ACTIVE mode, the input frequency to the counter should be within 5 MHz of the desired phase lock frequency when this portion is entered. The phase lock software will not attempt to phase lock unless the input frequency can be tuned to within 50 MHz of the desired frequency. Under circumstances where this portion of the program is entered, with the input frequency more than 50 MHz from the phase lock frequency, the software will attempt to tune the source with the shallow search DAC.

The program initially assumes the source DC gain constant is 1024 MHz/V (maximum gain constant). With this assumption, the phase lock software calculates the number of DAC steps needed to tune the source to the desired frequency. When the source has settled, after stepping the DAC, the program checks if the frequency change is more than 1.5 MHz. If it is, a new DC KO and polarity will be calculated. The frequency of the source is checked again to see if it is within 50 MHz of the desired frequency. If this condition is true, the software will start the phase lock process. If not, the process of stepping the shallow search DAC is repeated utilizing the calculated DC KO and polarity.

After stepping the DAC, if the change in frequency is less than 1.5 MHz, the current KO is divided by 32 and the stepping process is repeated. KO will be defaulted to 2 MHz/V if the result of the division is less than 2 MHz/V.

If the source output frequency cannot be tuned to within 50 MHz of the phase lock frequency in five tries, the phase lock process will be repeated indefinately until cancelled

DYNAMIC KO AND POLARITY DETERMINATION

This is the first step of the actual phase lock process. If the source has been tuned, the state of the divide-by 16 will be retained throughout the phase lock process. That is, the dynamic KO checked in this step is 1024 MHz/V to 32 MHz/V for the divide-by 16 on; and 64 MHz/V to 2 MHz/V for the divide-by 16 off. If the source has not been tuned, the full range of KO will be checked (i.e. 1024 MHz/V to 2 MHz/V).

The software determines the dynamic KO of the source by first assuming it equals the largest KO in the range to be checked. The shallow search DAC is stepped to produce a 5 MHz change in frequency under that assumption. The new frequency is read within 2.5 ms and the actual change in frequency is determined. If the actual change in frequency is less than 1.5 MHz, the current KO is divided by 4. The DAC is returned to where it was before it was stepped, and the DAC stepping process is repeated. This process is continued until the change in frequency is more than 1.5 MHz, and the actual dynamic KO is calculated, or all KO's in the range have been checked, and the phase lock process is restarted. During this step, converter lock must exist.

YIG AND LOCAL OSCILLATOR FREQUENCY DETERMINATION

In this step, the software goes through different calculations for different bands.

- For BAND 1, this step is skipped.
- For BAND 2, only the local oscillator frequency needs to be determined.
- For BAND 3 and BAND 4, both the YIG and the local oscillator frequencies are determined.

The YIG and local oscillator frequencies are determined from the desired phase lock frequency. The YIG and local oscillator are set according to the calculation.

SET PHASE LOCK LOOP ATTENUATOR AND REFERENCE LOOP

The loop attenuator is set according to the dynamic KO determined. With divide-by 16 on, a KO of 32 MHz/V corresponds to minimum attenuation; and with divide-by 16 off, 2 MHz/V corresponds to minimum attenuation. The reference loop is set to the same frequency as the IF. It is calculated by subtracting the local oscillator frequency (determined in the previous step) from the desired phase lock frequency.

TUNE SOURCE

The software will check for an IF threshold in this step. If IF exists, the program will proceed to the next step. If IF does not exist, the program will step the shallow search DAC to change the source frequency in 10 MHz steps. The size of the DAC step is determined by using the dynamic KO. The phase lock process will be restarted if IF does not exist within six tries.

SET BANDWIDTH AND POLARITY

The loop bandwidth is selected by the user through the keyboard or GPIB. If Bandwidth 0 is selected, the software will try to close the phase lock loop in the 10 kHz, 2 kHz and 500 Hz bandwidths sequentially. It will stop at the first bandwidth in which it can close the phase lock loop successfully.

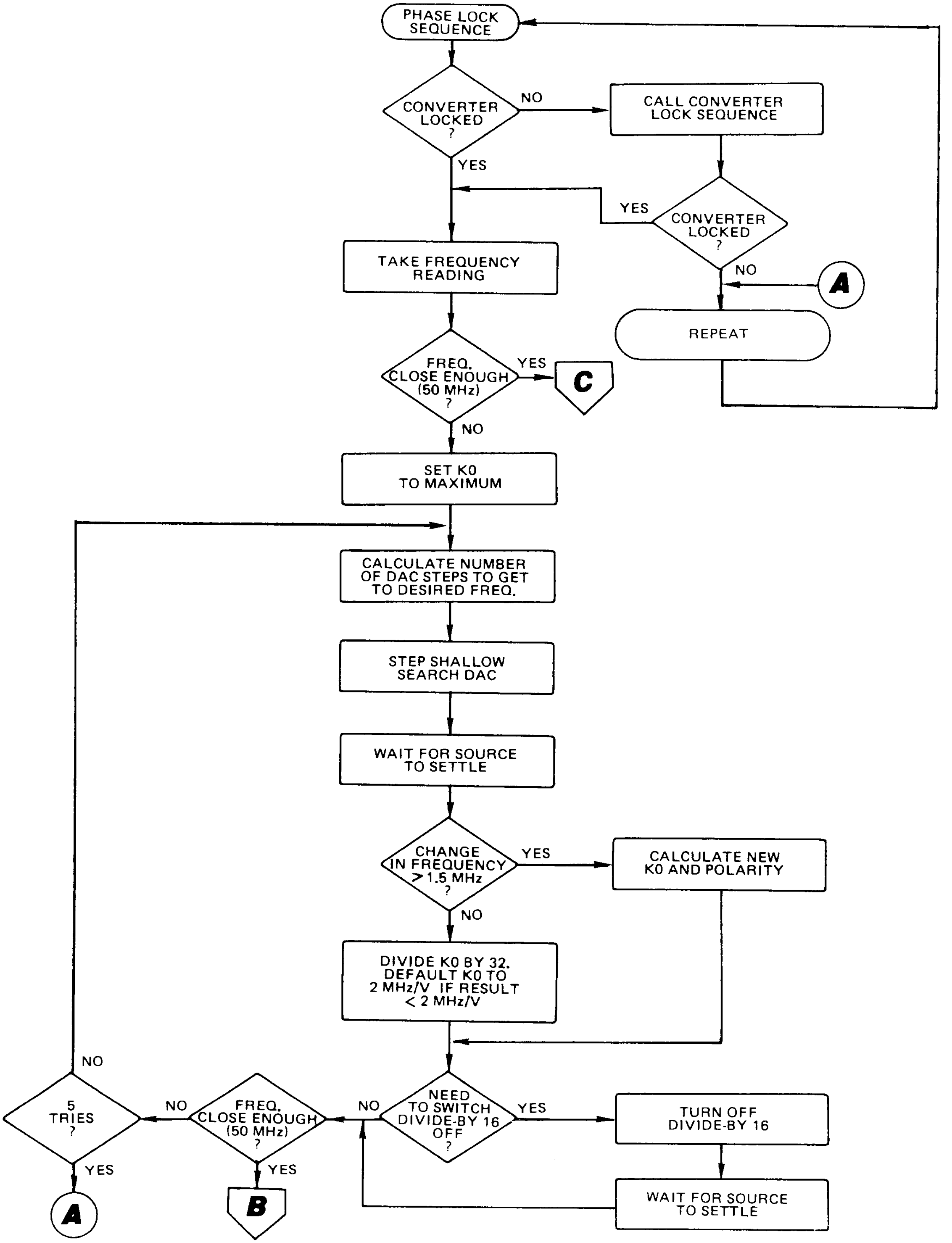


Figure 4-15. Phase Lock Flow Diagram.

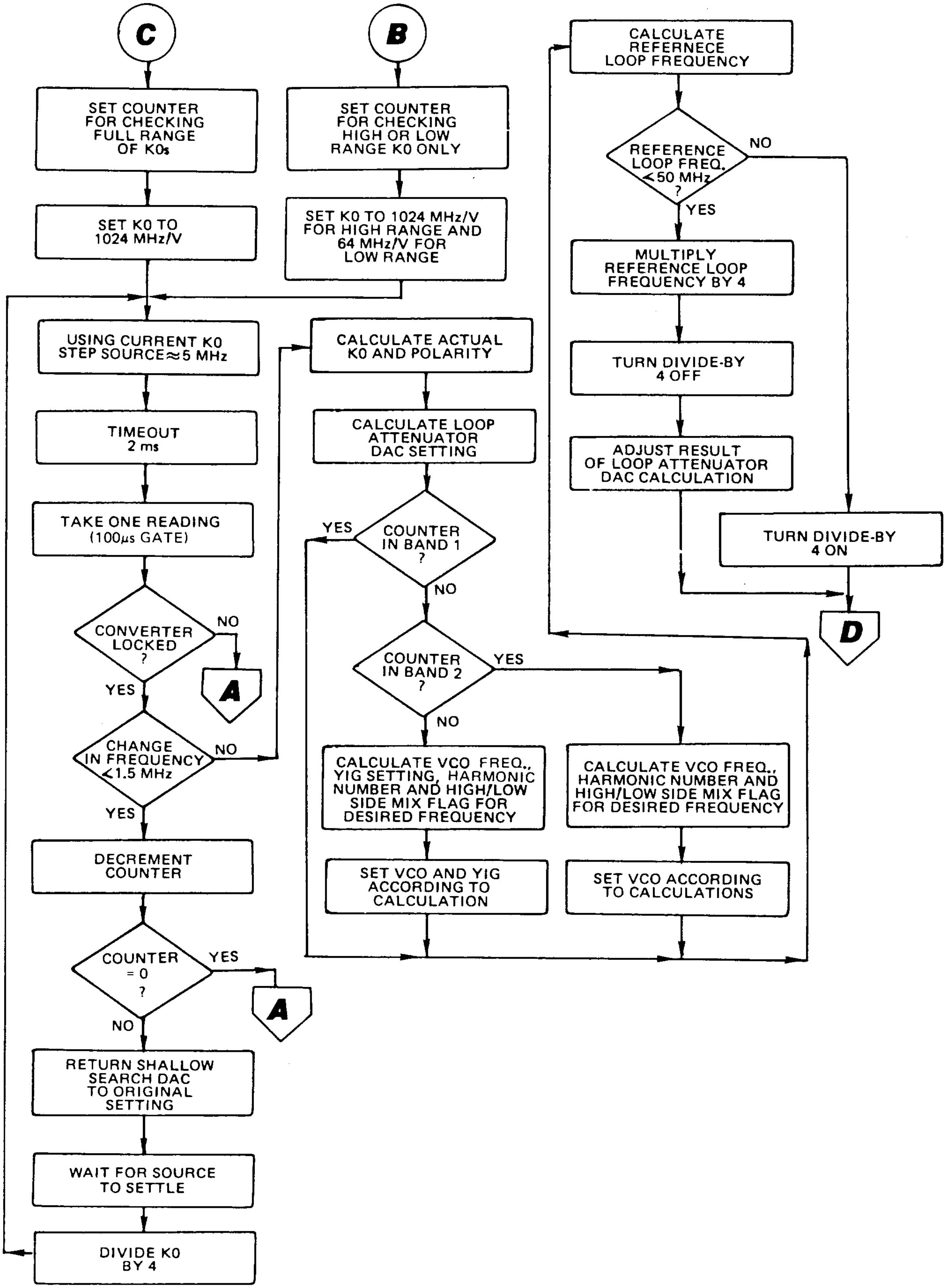


Figure 4-15. Phase Lock Flow Diagram, continued.

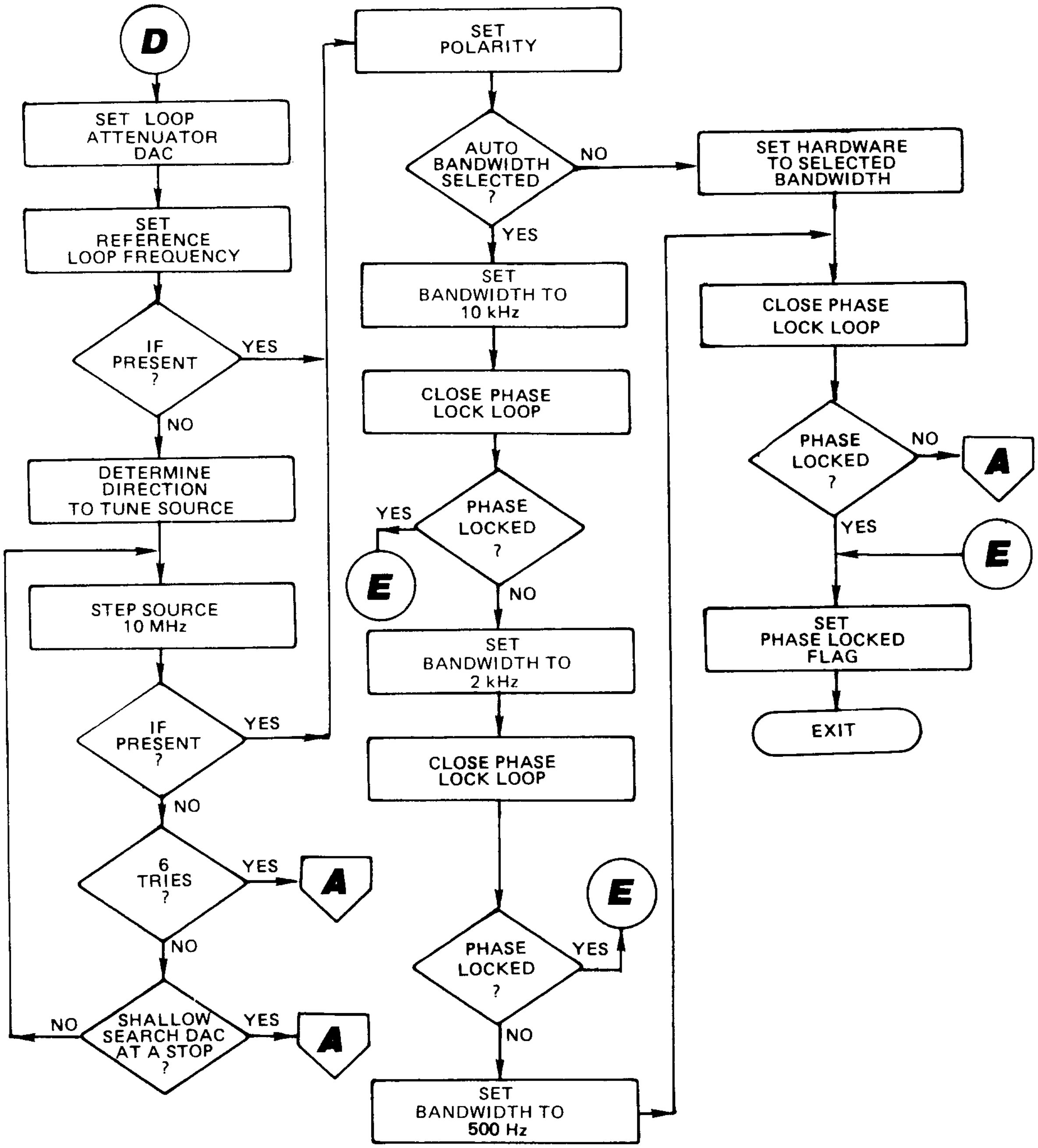


Figure 4-15. Phase Lock Flow Diagram, continued

CLOSE PHASE LOCK LOOP

After the polarity and bandwidth have been set, the program will close the phase lock loop by disconnecting the shallow search DAC and connecting the loop attenuator to the output driver. It will wait a maximum of 200 ms for the phase lock detector to indicate a phase lock condition if BW1 is selected. The software will wait a maximum of 50 ms if BW2 or BW3 is selected. If the wait period expires with phase lock condition not present, the phase lock process will be restarted.

STORING AND RECALLING DATA

When the store function is activated the counter will store the source lock frequency, the coarse tune DAC setting, the B.W. setting, the phase lock gain constant setting, and the shallow search DAC setting.

When recalling stored data the program restores all these settings, waits for the source frequency to settle, then closes the phase lock loop.

LOSS OF SOURCE LOCK INTERRUPT

If source lock is lost, the program is interrupted and the loss of lock routine is called. The loss of lock routine will check for 100 ms to see if source lock returns. If source lock is re-acquired and maintained the routine simply returns. If source lock is not re-acquired, or not maintained for 100 ms the phase lock output is set to zero volts and the source lock light will flash and the phase lock process will be restarted.

Section 5
Maintenance and Service

This section contains instructions and information to maintain your counter.

FUSE REPLACEMENT

The counter uses one fuse. It is located on the rear panel next to the voltage select switch.

- For 100/120VAC operation use a 1.0A slow-blow MDL type fuse.
- For 220/240VAC operation use a 0.50A slow-blow FST type fuse.

The voltage select switch should be set to the proper line voltage. To change line voltage:

1. Be sure the counter is disconnected from the power line.
2. With a flat edged screwdriver, rotate the voltage select switch until the arrow points to the desired line voltage.
3. Change to a fuse with the value specified for the line voltage selected.

NOTE:
Always be sure that the fuse is the type and value specified for, and that the voltage select switch is set to correspond to the AC power input voltage, or the counter may be damaged.

AIR CIRCULATION

Air circulates through the vents in the rear panel of the counter. These vents must not be obstructed or the temperature inside the counter may increase enough to reduce the counter stability and shorten the component life.

PERIODIC MAINTENANCE

No periodic preventive maintenance is required. To maintain accuracy, it is recommended that the counter be recalibrated every six months.

CAUTION

Do not attempt repair or disassembly of the Microwave Converter or Time Base Oscillator Assemblies. Contact EIP or your sales representative.

If the following assemblies are repaired or replaced, the counter may require recalibration for proper operation.

- Power Supply (A101)
- Gate Generator (A107)
- Converter Control (A108)
- Microwave Converter (A203)

Care should be taken when removing any assemblies to prevent damage to components or cables.

FACTORY SERVICE

If the counter is being returned to EIP for service or repair, be sure to include the following information with the shipment.

1. Name and address of owner.
2. Model and complete serial number of counter.
3. A COMPLETE description of the problem (Under what conditions did the problem occur? What was the signal level? What equipment was attached or connected to the counter? Did that equipment experience failure symptoms?).
4. Name and telephone number of someone familiar with the problem who may be contacted by EIP for further information, if necessary.
5. Shipping address to which the counter is to be returned. Include any special shipping instructions.
6. Pack the counter for shipping (Refer to Section 2).

FIELD SERVICE

EIP has an assembly exchange program. All plug-in assemblies, modules, and the front panel assembly may be exchanged.

After you have identified a faulty assembly, call EIP with the assembly number and shipping information. A replacement can be shipped within 24 hours. After receiving the replacement assembly, return the faulty assembly to EIP for credit.

Section 6
Troubleshooting

This section defines troubleshooting aids that are incorporated in the 575B/578B counter. They are:

- Signature analysis
- Self diagnostics
- Keyboard controlled circuit tests

The procedures and tables are provided for troubleshooting to a functional circuit level.

SIGNATURE ANALYSIS

Signature analysis is a technique used to troubleshoot complex logic circuitry. It uses data compression to reduce any data pattern to a 4 character alpha-numeric word.

The start and stop inputs define the measurement window. Each time a transition within the measurement window occurs on the clock input, the probe is sampled, and the logic level is shifted into the analyzer. This information is used to generate a signature unique to that data string. That signature can then be compared to a reference signature, taken from a known good product, to determine if the data string is correct. The counter implements signature analysis in either a free running or program controller manner.

FREE RUNNING

This mode of signature analysis is essential for troubleshooting problems that could prevent the program from running. A CLRB instruction can be forced by breaking the data bus at A105 JMP1 and grounding A105 TP5, effectively "free running" the microprocessor. "Free running" means forcing a simple instruction (such as NOP or CLRB) on the data bus, which the microprocessor sees at every address location. This causes the microprocessor to continually cycle through its entire address range, accessing everything on the address bus as it does. By strategically placing the start and stop connections the entire bus system can be probed for bad signatures.

	START	STOP	CLOCK
CONNECTIONS	A105 TP4	A105 TP4	A105 TP3
BUTTONS	IN	IN	IN

LINE	SIGNATURE	LINE	SIGNATURE
A0 (P1 Pin 54)	UUUU		
A1 (P1 Pin 53)	FFFF		
A2 (P1 Pin 52)	8484		
A3 (P1 Pin 51)	P763		
A4 (P1 Pin 50)	1U5P		
A5 (P1 Pin 49)	0356		
A6 (P1 Pin 48)	U759		
A7 (P1 Pin 47)	6F9A		
A8 (P1 Pin 46)	7791		
A9 (P1 Pin 45)	6321		
A10 (P1 Pin 44)	37C5		
A11 (P1 Pin 43)	6U28		
A12 (P1 Pin 42)	4FCA		
A13 (P1 Pin 41)	4868		
A14 (P1 Pin 40)	9UP1		
A15 (P1 Pin 39)	00001		
U3 (P1 Pin 7)	76AC		
U5 (P1 Pin 8)	0000		
TP6	854F		
TP7	PACH		
TP8	755F		
TP9	755H		
U8 (P1 Pin 19)	U3P7		
U9 (P1 Pin 18)	0003		
U10 (P1 Pin 18)	0003		
U17 (P1 Pin 1)	9F14		
U17 (P1 Pin 2)	9F17		

+ 5V 0003, phase 2 0003 *

* Due to the synchronous qualities of the signature analyzer, phase 2 will read the same as + 5V but the logic probe will be flashing. Likewise, anything gated with phase 2 may have the same signature as the ungated signal.

Figure 6-1. Microprocessor Free Running Signatures

PROGRAM CONTROLLED

If the counter is working sufficiently to access the test functions, program controlled signature analysis can be used. In program controlled signature analysis the start and stop (and therefore the signature) are controlled by software. This allows the signature analyzer to be used, in many cases, to troubleshoot the hardware outside the bus system.

SELF DIAGNOSTICS

At turn-on, the counter performs several internal diagnostic checks, checking the RAM, PROM, and the associated decoding circuitry. The display shows dashes during these checks. If the counter passes the test it then enters the normal operating mode. If it fails RAM check the display will show all Es. If the counter fails any of the PROM checks an error message will be displayed. Please refer to Figure 6-3.

The counter generates PROM error signatures only during the power up diagnostics check. It is necessary to turn the power off, and then on again, while the signature analyzer is connected, to get a signature.

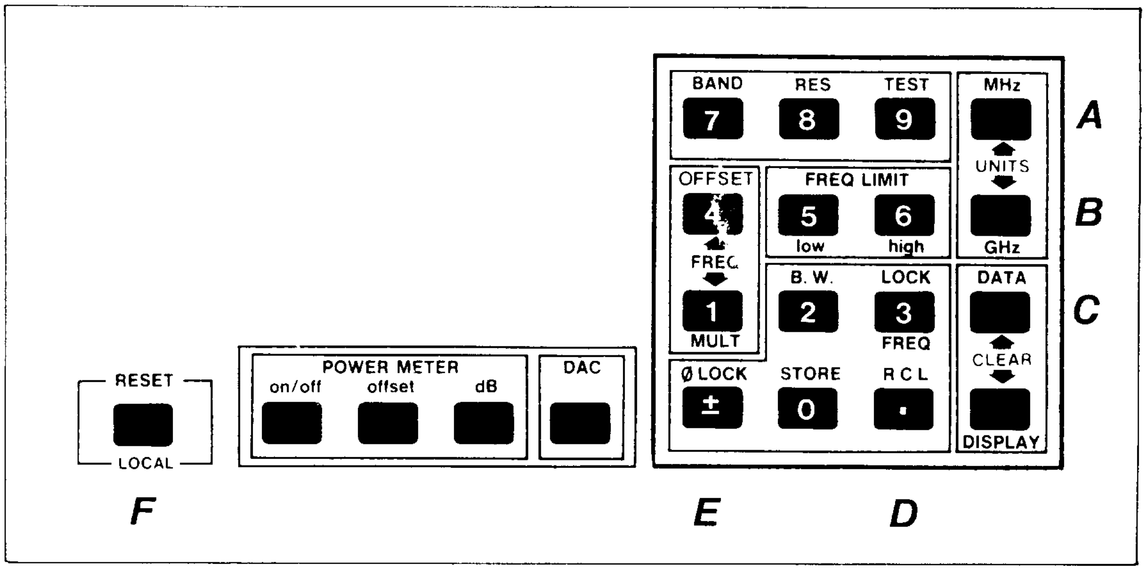
	START	STOP	CLOCK	PROBE
CONNECTION BUTTONS	A106 TP5 OUT ↑	A106 TP5 IN ↓	A105 TP8 IN ↓	A105 TP6 (+5V)

PROBLEM	ERROR
RAM Bad	All E's
A105 U11 (Basic Program) Bad	31
A105 U12 (Basic Program) Bad	32
A105 U13 (Basic Program) Bad	33

Figure 6-2. Self Diagnostic Error Indications

KEYBOARD CONTROLLED CIRCUIT TESTS

There are 11 keyboard controlled circuit tests (01 thru 11). All tests are accessed by pressing TEST ☐ and then the two digit test number. Tests which do not require keyboard inputs to function (tests 01, 02, 03, 04, 06, 07) can be exited by pressing any key. The counter will exit the test and enter the function selected. Tests which use the keyboard in their operation (tests 05,08,09,10,11) can be exited by pressing any key not used by the test. All tests can be exited by pressing CLEAR ☐ DISPLAY. The counter will return to normal operation. Some tests require hexadecimal coded keyboard inputs (tests 08, 09, 10, 11). For those tests the keyboard is defined in Figure 6-4.



KEY	HEX EQUIV.	KEY	HEX EQUIV.
0	0	9	9
1	1	MHz	A
2	2	GHz	B
3	3	CLR DATA	C
4	4		
5	5	●	D
6	6	+/–	E
7	7	RESET	F
8	8	CLR DISPLAY	EXITS TEST

Figure 6-3. Keyboard Configuration For Tests Requiring Hexidecimal Inputs.

	START	STOP	CLOCK	PROBE
CONNECTION	A106 TP5	A106 TP5	A105 TP8	A105 TP6 (+5 V)
BUTTONS	OUT ↑	IN ↓	IN ↓	

BUTTON	COORDINATES	SIGNATURE
Reset	47	U68C
Power Meter ON/OFF	46	U7HA
Power Meter Offset	36	20P6
dB	16	U2F9
DAC	26	811P
7	41	A19C
8	42	66PU
9	43	CCH7
MHz	44	U5PU
4	31	PUPH
5	32	UC70
6	33	HF3A
GHz	34	OPA2
1	21	APH1
2	22	C45H
3	23	1766
CLR DATA	24	H9C8
+/–	11	375U
0	12	H7PC
●	13	UAHH
CLR DISPLAY	EXIT TEST	C75U

Figure 6-4. Keyboard Test Coordinates and Signatures.

TESTS

01 **200 MHz Self Test.** This test sets the VCO to 400 MHz, divides it by two, and counts the 200 MHz output from the divider. It checks the count chain, VCO and VCO phase lock circuitry, and the gate generator.

02 **8's Test.** This will light all LEDs, annunciators, and decimal points. It checks that everything on the display is lit, the intensity of the display, and the alignment of the LEDs and annunciators.

03 **Display Segment Test.** This lights one segment of each digit, and one annunciator at a time, cycling through all segments. The cycle rate can be adjusted with the sample rate pot. It verifies that each segment of the display, segment drivers and display multiplexer operate properly and independently.

04 **Display Digit Test.** This lights one entire digit, and its decimal point, at a time. It cycles through all digits and annunciators. The cycle rate is determined by the sample rate pot. It checks each digit and digit driver independently, and verifies operation of the display multiplexer.

05 **Keyboard Test.** This will display the coordinates of each key as it is pressed. It also generates a unique signature for each key, so that keyboard can be checked without the display. Test 05 may be entered by keyboard or by momentarily tying A108 TP1 to A108 TP5. This makes it possible to enter the keyboard test for troubleshooting even if the keyboard is not operating well enough to enter the test in a normal manner. Test 05 checks the keyboard, keyboard interrupt, and keyboard decode circuitry. The coordinates and signatures for each key are shown in Figure 6-5.

06 **Converter Ramp Test.** Test 06 continuously ramps the Band 3 Converter DAC from 0 to 27 GHz, in 2 MHz (LSB) steps. It also generates a signature for each of the inputs to the DAC. (See Figure 6-6). It can be used to test the YIG DAC, YIG drivers, YIG, and Band 3 RF level circuits.

	START	STOP	CLOCK
CONNECTIONS	A106 TP5	A106 TP5	A105 TP8
BUTTONS	OUT ↑	IN ↓	IN ↓

NODE	SIGNATURE	NODE	SIGNATURE
A108 U4 Pin 2	9U78	A108 U4 Pin 9	7763
A108 U4 Pin 3	9946	A108 U4 Pin 10	HP8A
A108 U4 Pin 4	8F62	A108 U4 Pin 11	P45A
A108 U4 Pin 5	89U9	A108 U4 Pin 12	80A8
A108 U4 Pin 6	833F	A108 U4 Pin 13	77U6
A108 U4 Pin 7	U9CC	A108 U4 Pin 14	7245
A108 U4 Pin 8	FCA6	A108 U4 Pin 15	28U9
+ 5V	49P4		

Figure 6-5. Converter Ramp Test Signatures

07 **VCO Test** This test cycles the VCO frequency from 400 to 500 MHz, in increments of 50 kHz. The cycle rate can be adjusted by the sample rate pot. 07 tests the VCO and the phase lock circuitry.

08 **Power Meter Offset Test** This makes it possible to set the power meter zero DAC to any setting. The setting is entered as a four digit hexadecimal number (figure 6-4). The first two digits are used to program the coarse offset DAC, and the last two digits program the fine offset DAC. Test 08 enables the power meter zero DAC to be tested, and can provide a DC level signal to aid in testing the power meter circuit.

09 **Power Meter Gain Test** This makes it possible to set the power meter sensing circuit to any number. The number is entered as a five digit hexadecimal number (figure 6-4) in the following format.

1st digit	A107 U10 bits 4-7
2nd digit	A107 U10 bits 0-3
3rd digit	A107 U12 bits 4-7 (Power Meter Option only)
4th digit	A107 U12 bits 0-3 (Power Meter Option only)
5th digit bit 0	Sets Amp marked "15 dB Gain" to high gain
5th digit bit 1	Sets Amp marked "30 dB Gain" to high gain

Digit 5 is a 2 bit number, so any number entered for digit 5 will be justified to a number from 0-3. Test 09 checks the RF level and power meter circuits.

10 **Information Read/Alter Routine** Test 10 can read any microprocessor address and, if that address is RAM or I/O, change its contents. The desired address is entered as a 4 digit hexadecimal number (see figure 6-4). When the 4th digit is entered the counter will display the contents of the desired address. The contents are then changed by entering a two digit hexadecimal number.

NOTE

Test 10 can change any temporary storage in the counter, including locations that are essential to the operation of the counter. Changing the wrong location will not damage the counter permanently, but it can cause improper operation. To return the counter to proper operation turn the counter off then back on.

SIGNIFICANT ADDRESSES, I/O PORTS

If an I/O bit is configured as an output, the number read by test 10 will be the same number that is programmed. If an I/O bit is configured as an input, the number read by test 10 will be the input signal level on the I/O line. Therefore, if an I/O port is programmed, and then read, the number displayed may not correspond to the number programmed because some bits of the I/O port may be configured as inputs.

DESCRIPTION	ADDRESS OF PA PORTS	ADDRESS OF PB PORTS
PIA on Ref Loop (A103)	2820	2822
PIA on Phase Lock (A104)	2A00	2402
PIA on Count Chain (A106)	2C00	2602
PIA on Gate Generator (A107)	1900	1902
Frequency Control PIA on Converter Control (A108)	1840	1842
Programmable Counter PIA on Converter Control (A108)	1820	1822
PIA on Band 2 Converter (A109)	1880	1882
PIA on Front Panel Logic (A111)	1808	180A

DESCRIPTION	ADDRESS
GPIB Address Switch	1C04

Figure 6-6. I/O Addresses.

Two important I/O port locations are the yig frequency control (address 1840, 1842) and the VCO frequency control (address 1820, 1822).

To convert from the desired yig frequency to the PIA program number:

1. Round the desired frequency to a multiple of 2 MHz (The yig DAC resolution is 2 MHz).
2. Divide the desired frequency in MHz by 2 (F/2).
3. Convert F/2 from decimal to hexadecimal.
4. The two most significant digits are programmed to address 1842, and the two least significant digits are programmed to address 1840.

To convert from the desired VCO frequency to the PIA program number:

EXAMPLE (420.75 MHz)

1. Round the desired frequency to a multiple of 50 kHz (The resolution of the VCO frequency is 50 kHz).
2. Multiply the desired frequency (in MHz) by 5. . . . . 420.75 X 5 = 2103.75
3. If the result contains no fractional part, go to step 8.
4. Multiply only the fractional part by 16 . . . . .75 X 16 = 12
5. Add the result to the most significant digit from step 2. . . . . MSD of 2103.75 = 2 - 2 + 12 = 14
6. Convert the result to hexadecimal. . . . . $14_{10} = E_{16}$
7. Replace the MSD from step 2 with the result from step 6 and drop the fractional part. . . . . 2103.75 → E103
8. The two most significant digits are programmed to address 1822, and the two least significant digits are programmed to address 1820.

SIGNIFICANT ADDRESSES, RAM

All storage is RAM are in the following formats.

REGISTER FORMAT, FREQUENCY STORAGE		
ADDRESS	SIGN (00 = + , FF = –)	
ADDRESS + 1	100 GHz	10 GHz
ADDRESS + 2	1 GHz	100 MHz
ADDRESS + 3	10 MHz	1 MHz
ADDRESS + 4	100 KHz	10 KHz
ADDRESS + 5	1 KHz	100 Hz
ADDRESS + 6	10 Hz	1 Hz

REGISTER FORMAT, POWER STORAGE		
ADDRESS	SIGN (00 = +, FF = –)	
ADDRESS + 1	NOT	USED
ADDRESS + 2	NOT	USED
ADDRESS + 3	NOT	USED
ADDRESS + 4	NOT	USED
ADDRESS + 5	100 dB	10 dB
ADDRESS + 6	1 dB	. 1 dB

REGISTER	ADDRESS
L.O. frequency	0257
I.F. frequency	02C0
Frequency output to display	0267
Frequency limit low	02DC
Frequency limit high	02D5
Frequency offset	02C7
Source lock frequency	0102
Source lock hardware condition (MISC1)	010D

Figure 6-7. Frequency Storage Registers

REGISTER	ADDRESS
Power output to display	026E
Power offset	02CE

Figure 6-8. Power Storage Registers

REGISTER	ADDRESS
Coarse Tune Gain Constant (2 bytes)	0002
Phase Lock Gain Constant (2 bytes)	0010
Phase Lock Polarity (1 byte)(0=+,FF= –)	010B

Figure 6-9. Other Significant Registers

To Translate Coarse Tune Gain Constant to MHz/V:

1. Convert coarse tune gain constant from hexadecimal to decimal.
2. Multiply gain constant by 1.606.
   $(K0_{16} \rightarrow K_{10} \times 1.606 = K0(MHz/V)$

To Translate Phase Lock Gain Constant to MHz/V:

The phase lock K0 stored in the counter is in DAC steps/kHz. To translate the phase lock K0 to MHz/V, determine if the divide-by 16 is on or off by checking the register MISC1. If the most significant bit is set, divide-by 16 is off. Use one of the following formulas as determined by the state of the divide-by 16.

For Divide-By 16 On:

Convert phase lock gain constant from hexadecimal to decimal. Divide 12782 by the result.
Formula: $12782/(K0_{16} \rightarrow K0_{10}) = K0(MHz/V)$

For Divide-By 16 Off:

Convert phase lock gain constant from hexadecimal to decimal. Divide 798 by the result.
Formula: $798/(K0_{16} \rightarrow K0_{10}) = K0(MHz/V)$

TESTS, continued

11 **Coarse Tune Test** This allows the 14 bit coarse tune DAC to be set to any number. The number is entered as a hexadecimal number from 0 to 3FFF.

21 DAC Option 01 is described in Section 10.

TROUBLESHOOTING TREES

Troubleshooting trees are intended only as a guide, and do not describe every possible failure situation. Turn power off before removing or installing any P.C. boards or connectors. If the following assemblies are repaired or replaced, recalibration of the counter will be necessary.

- A101 Power Supply
- A107 Gate Generator
- A108 Converter Control
- A203 Converter Assembly

CAUTION

Do not attempt to repair or disassemble the A203 hybrid assembly.

TEST EQUIPMENT REQUIRED

MANUFACTURER	MODEL	DESCRIPTION	CRITICAL PARAMETERS
Tektronix	475	Oscilloscope	100 MHz min. Bandwidth
Fluke	8050A	D.V.M.	41/2 digit resolution
H.P.	182C, 8559A	Spectrum Analyzer	125 MHz
H.P.	5004A	Signature Analyzer	
H.P.	651B	Signal Generator	10 Hz - 10 MHz
Wavetek	2002	Sweeper	10 MHz - 2 GHz
EIP	931	Microwave Sweeper	1-20 GHz
H.P.	8690A, 8696A	Microwave Sweeper	20 GHz - 26.5 GHz

Figure 6-10. Troubleshooting Test Equipment (Or Equivalent).

To use the troubleshooting trees:

1. Refer to the main troubleshooting tree.
2. Step through the main troubleshooting tree, performing all necessary checks, until the failure mode is noted.
3. Refer to the appropriate troubleshooting tree for the failure mode.

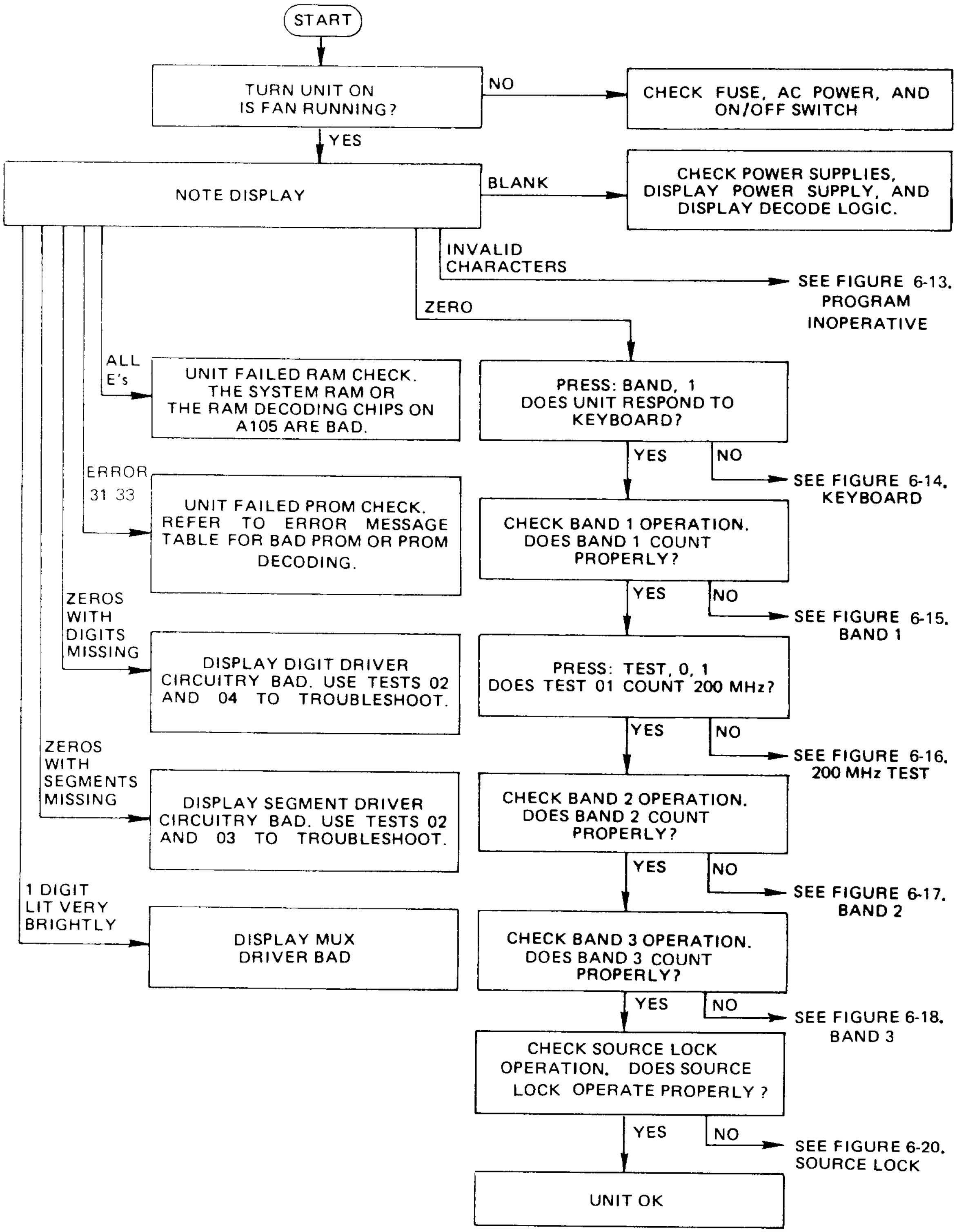
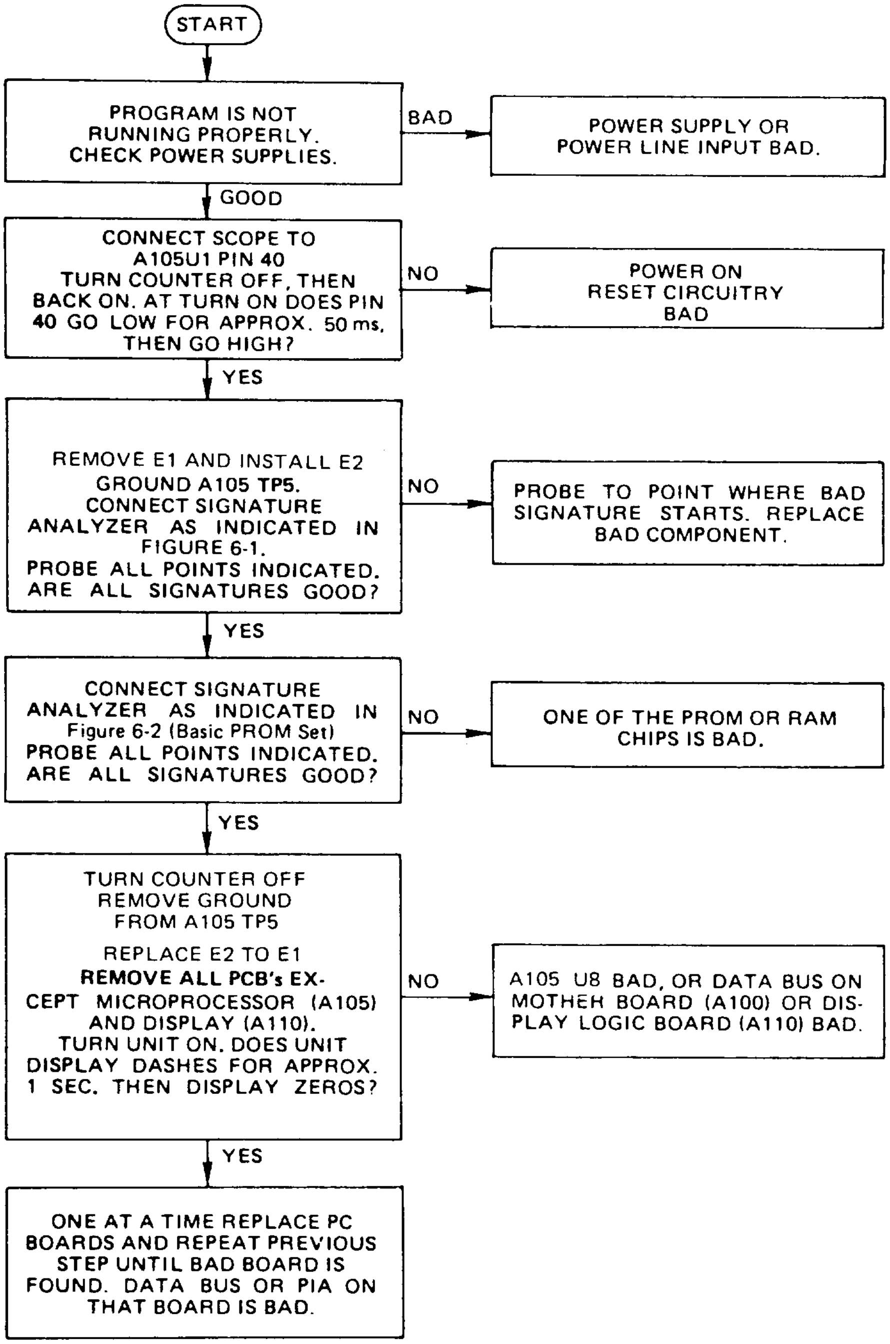


Figure 6–11. Main Troubleshooting Tree



PROGRAM IS NOT RUNNING PROPERLY. CHECK POWER SUPPLIES.

POWER SUPPLY OR POWER LINE INPUT BAD.

CONNECT SCOPE TO A105U1 PIN 40 TURN COUNTER OFF, THEN BACK ON. AT TURN ON DOES PIN 40 GO LOW FOR APPROX. 50 ms, THEN GO HIGH?

POWER ON RESET CIRCUITRY BAD

REMOVE E1 AND INSTALL E2 GROUND A105 TP5. CONNECT SIGNATURE ANALYZER AS INDICATED IN FIGURE 6-1. PROBE ALL POINTS INDICATED. ARE ALL SIGNATURES GOOD?

PROBE TO POINT WHERE BAD SIGNATURE STARTS. REPLACE BAD COMPONENT.

CONNECT SIGNATURE ANALYZER AS INDICATED IN Figure 6-2 (Basic PROM Set) PROBE ALL POINTS INDICATED. ARE ALL SIGNATURES GOOD?

ONE OF THE PROM OR RAM CHIPS IS BAD.

TURN COUNTER OFF REMOVE GROUND FROM A105 TP5

REPLACE E2 TO E1 **REMOVE ALL PCB's EXCEPT MICROPROCESSOR (A105) AND DISPLAY (A110).** TURN UNIT ON. DOES UNIT DISPLAY DASHES FOR APPROX. 1 SEC. THEN DISPLAY ZEROS?

A105 U8 BAD, OR DATA BUS ON MOTHER BOARD (A100) OR DISPLAY LOGIC BOARD (A110) BAD.

ONE AT A TIME REPLACE PC BOARDS AND REPEAT PREVIOUS STEP UNTIL BAD BOARD IS FOUND. DATA BUS OR PIA ON THAT BOARD IS BAD.

Figure 6-12. Program Inoperative

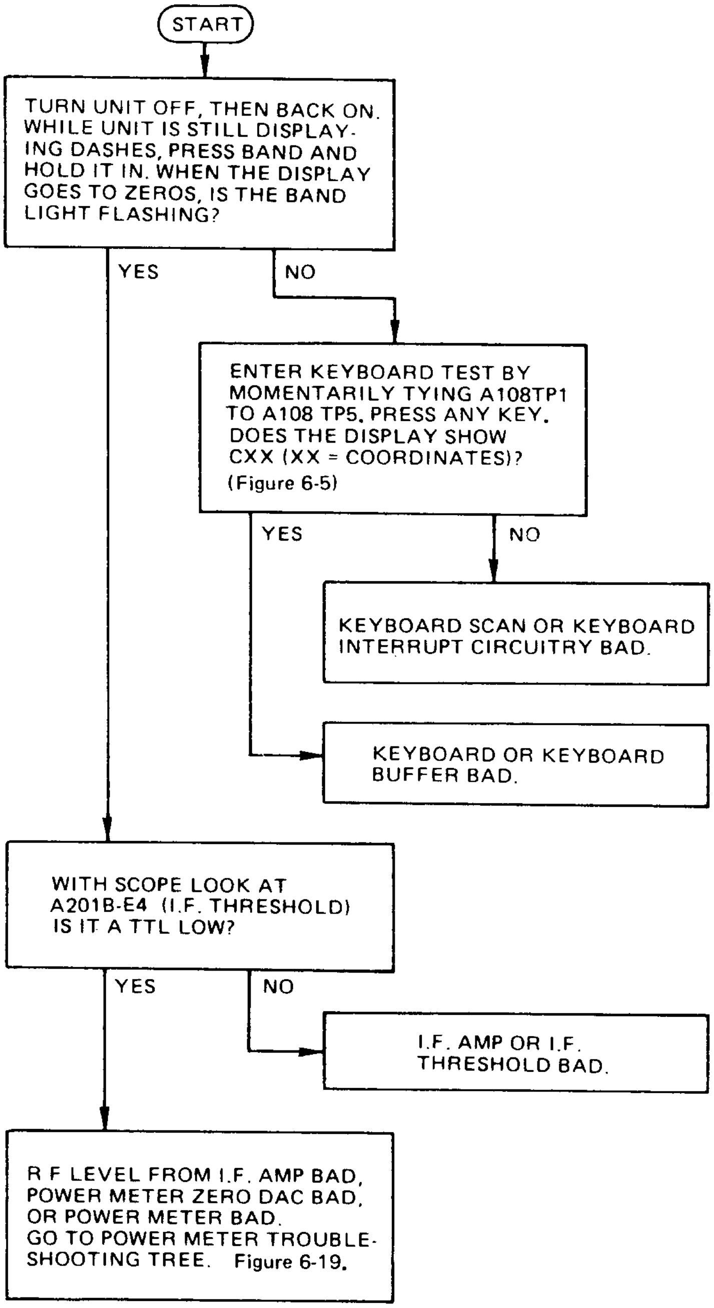


Figure 6-13. Keyboard

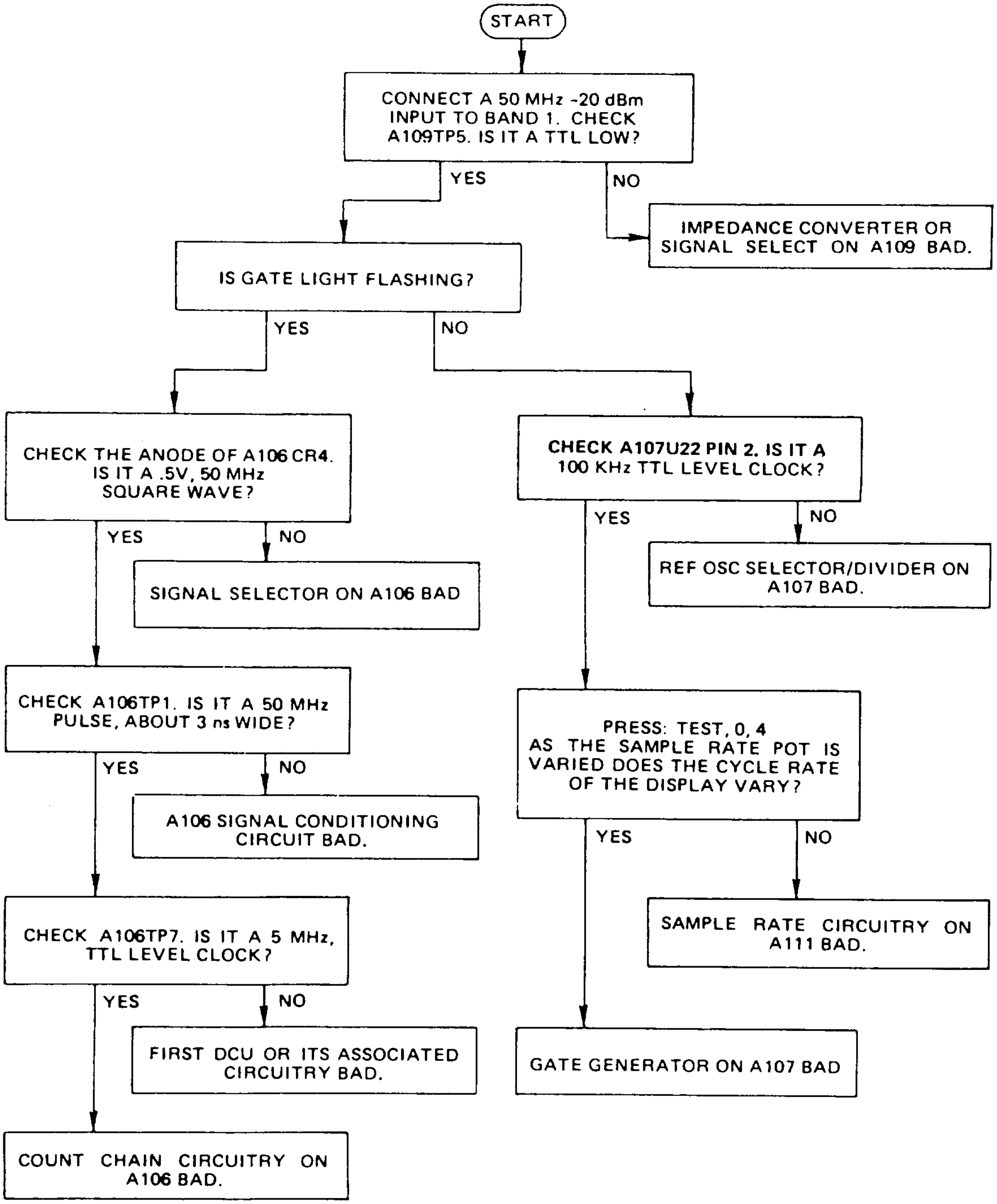


Figure 6-14. Band 1

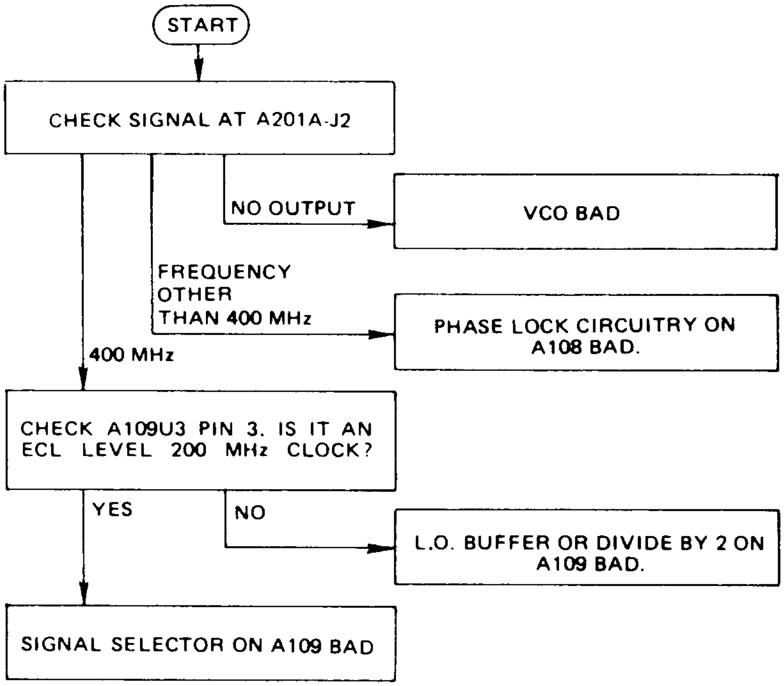


Figure 6-15. 200 MHz Test

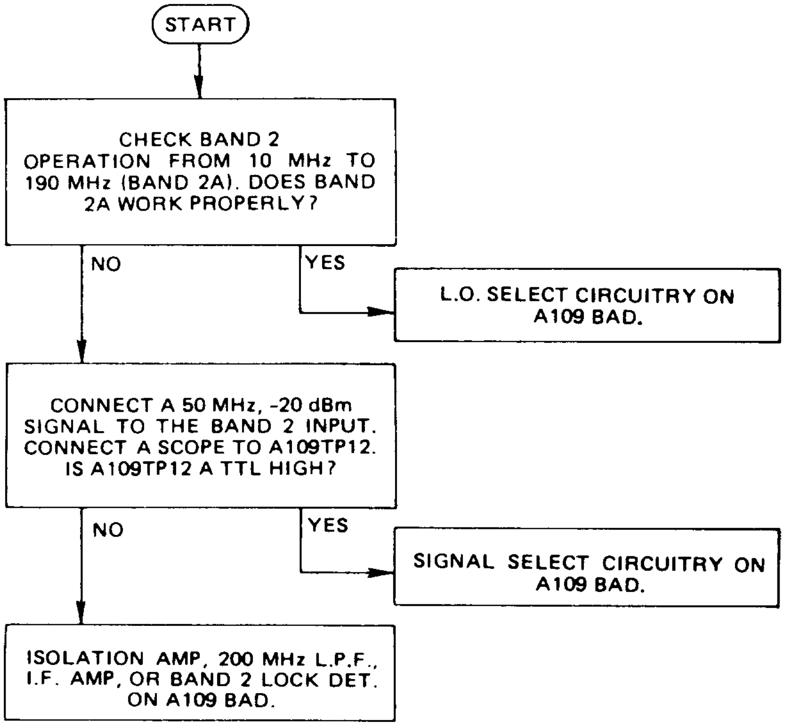


Figure 6-16. Band 2

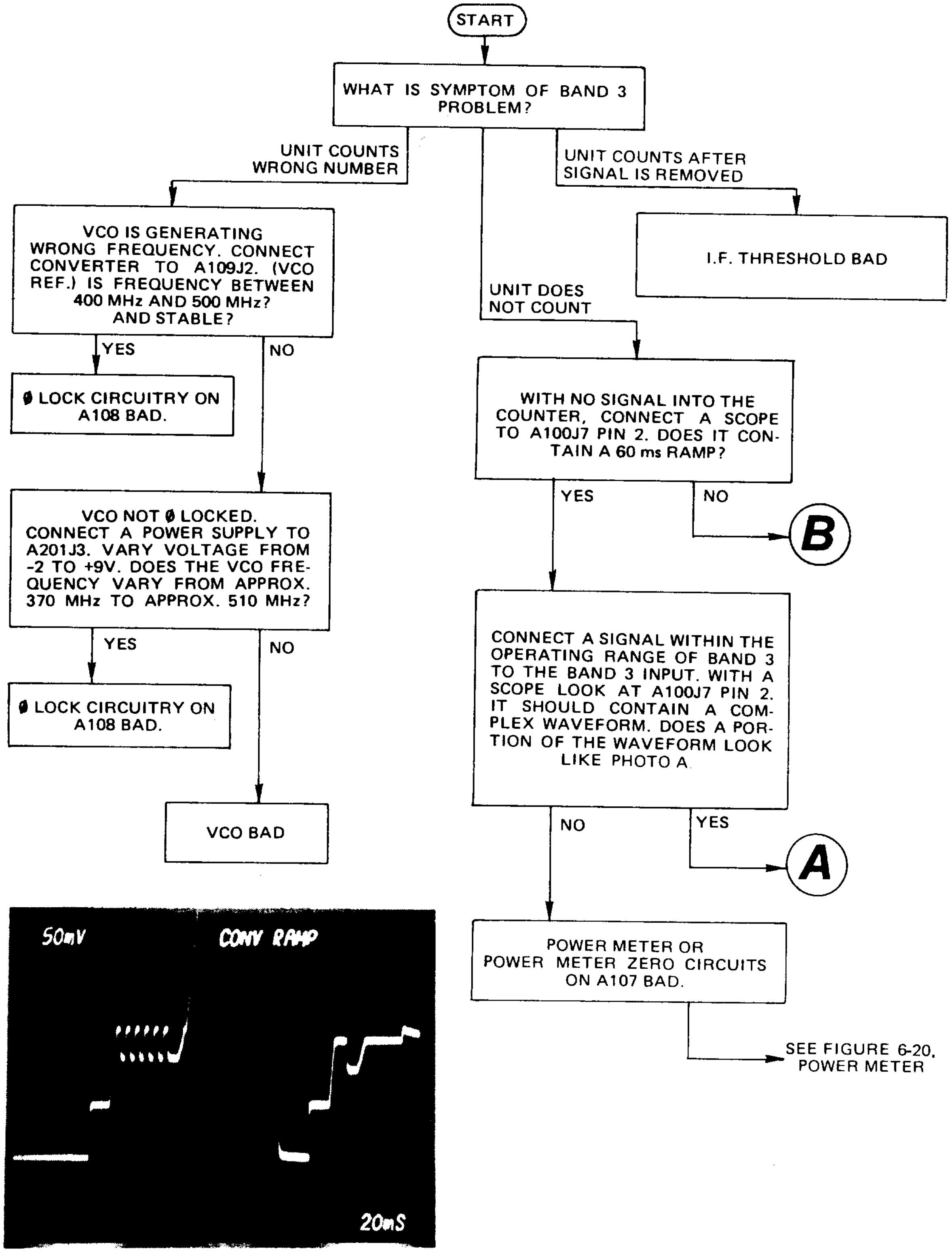


PHOTO A.

Figure 6-17. Band 3

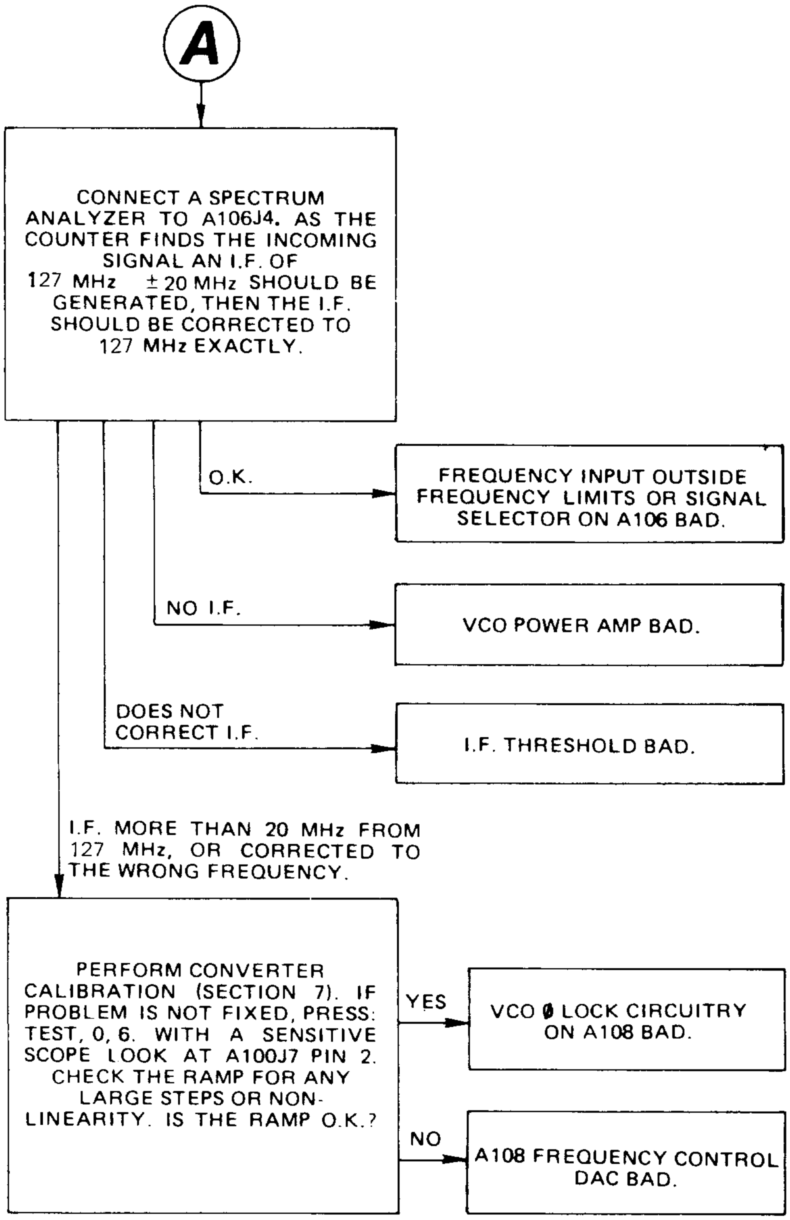


Figure 6-17. Band 3, continued

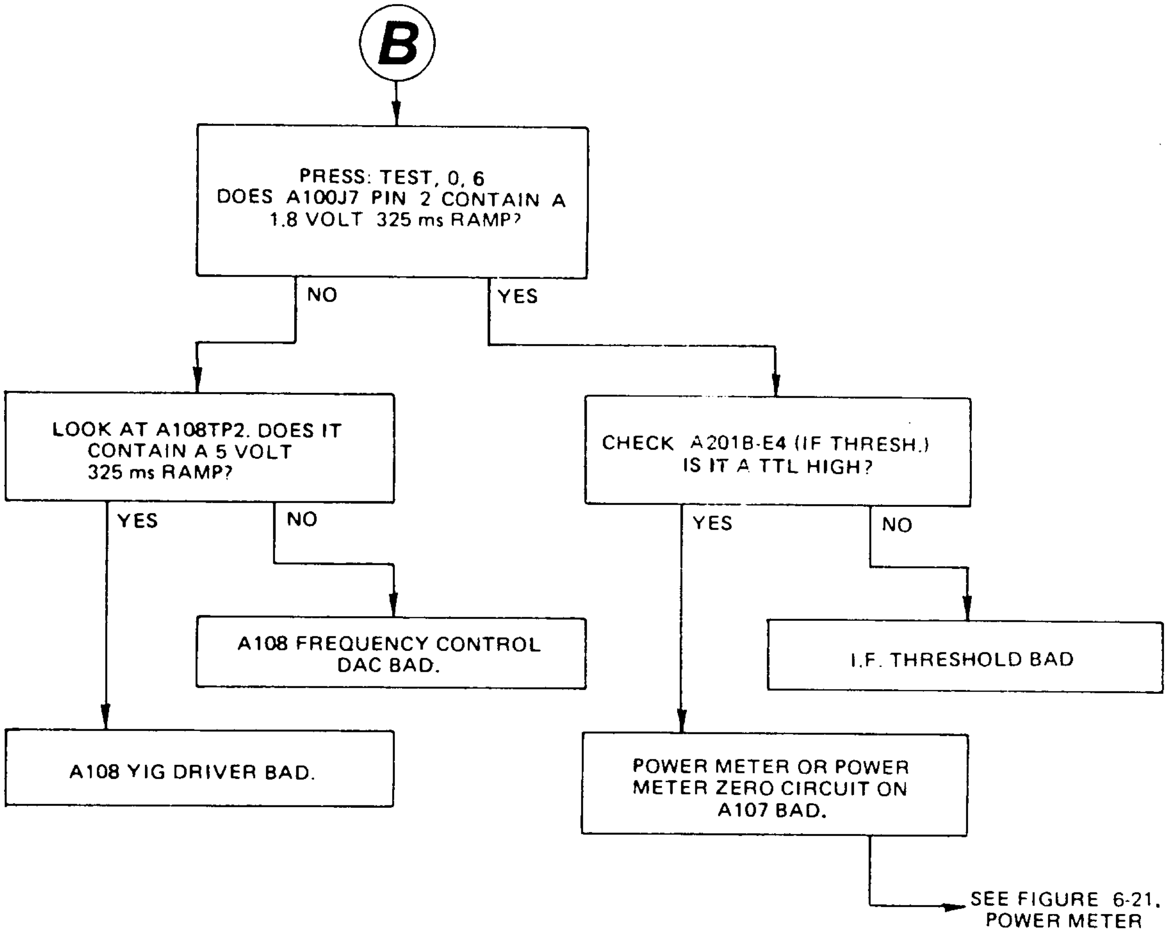


Figure 6-17. Band 3, continued

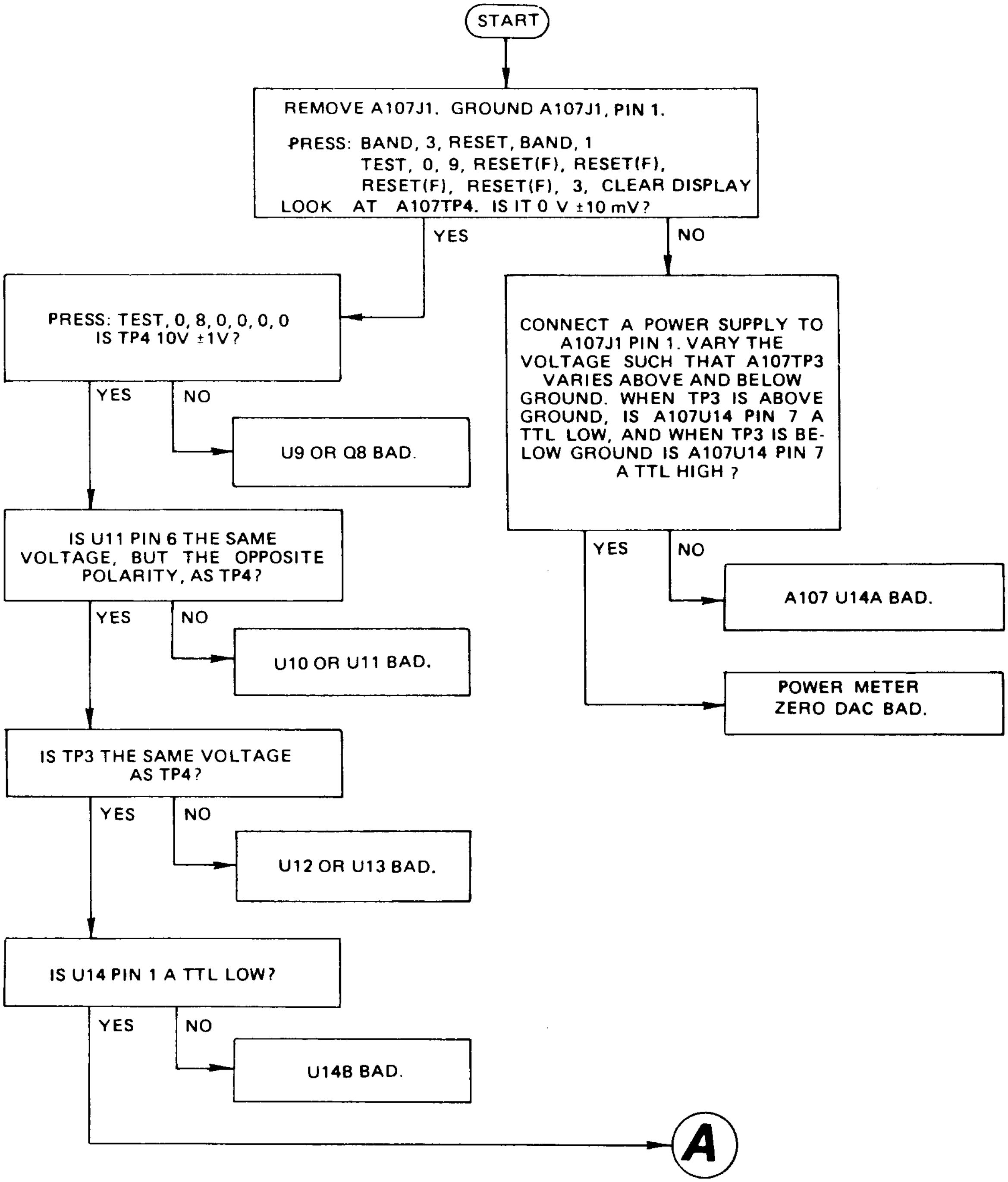


Figure 6-18. Power Meter and Power Meter Zero DAC

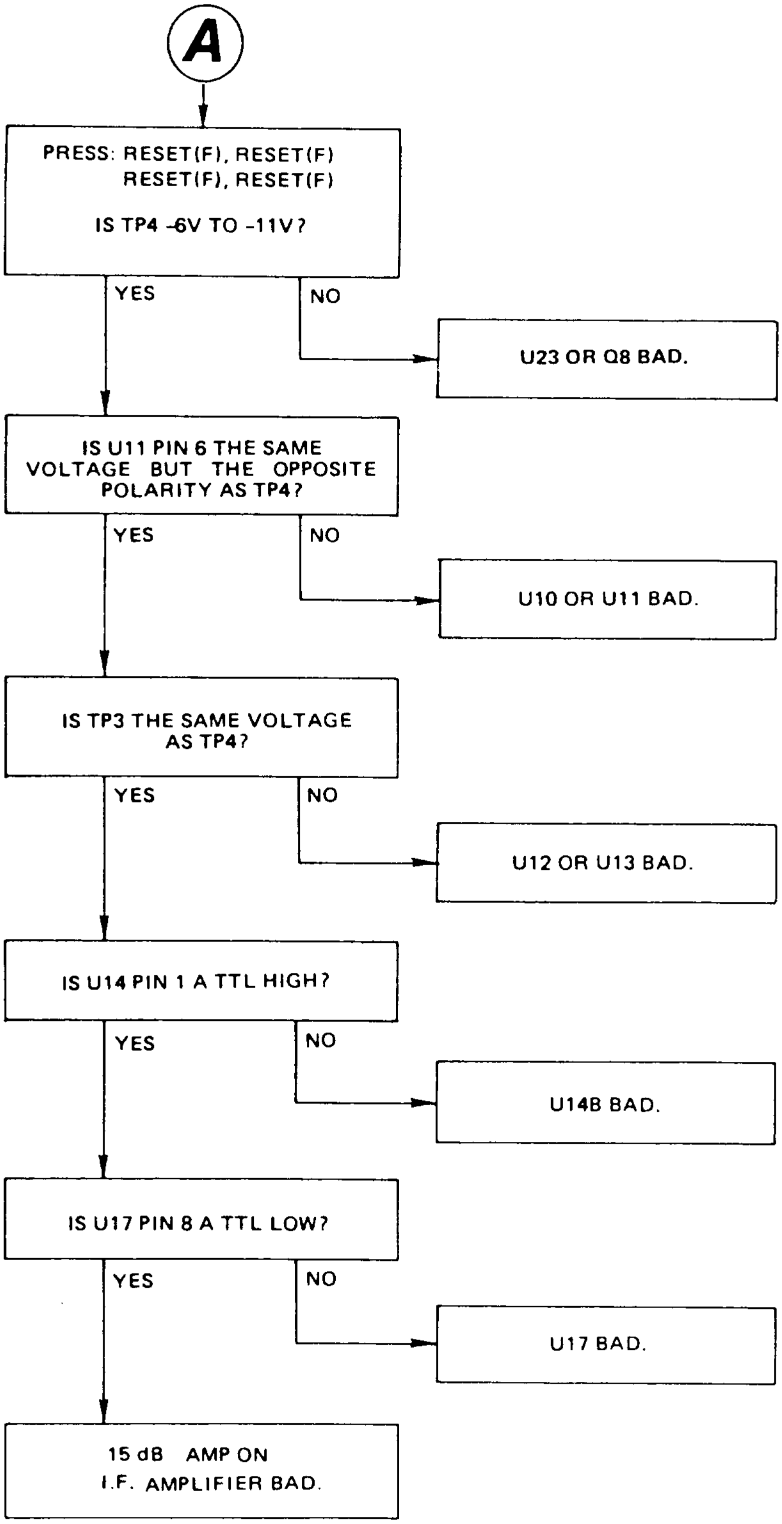


Figure 6-18. Power Meter and Power Meter Zero DAC, continued

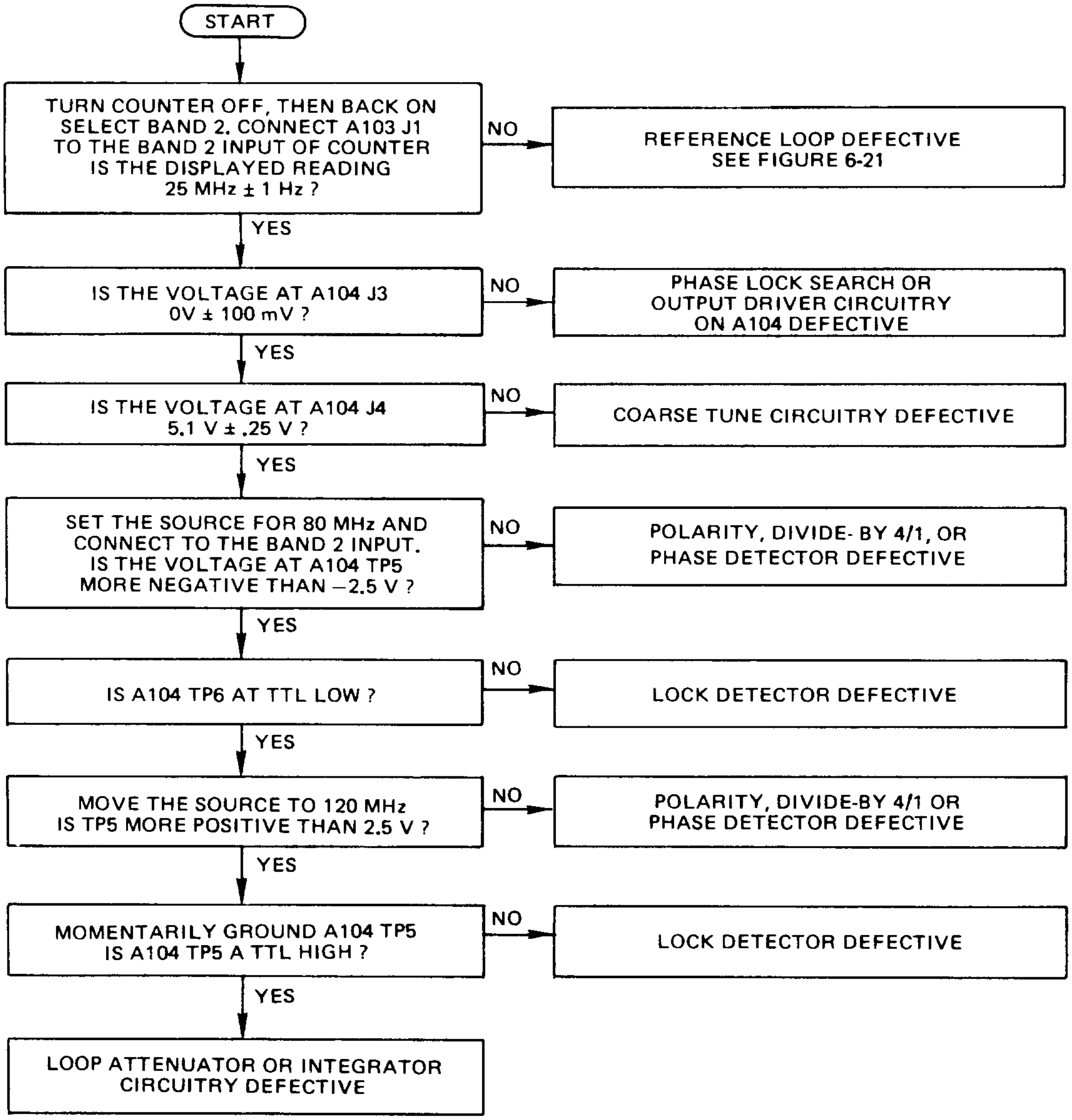


Figure 6-19. Source Lock

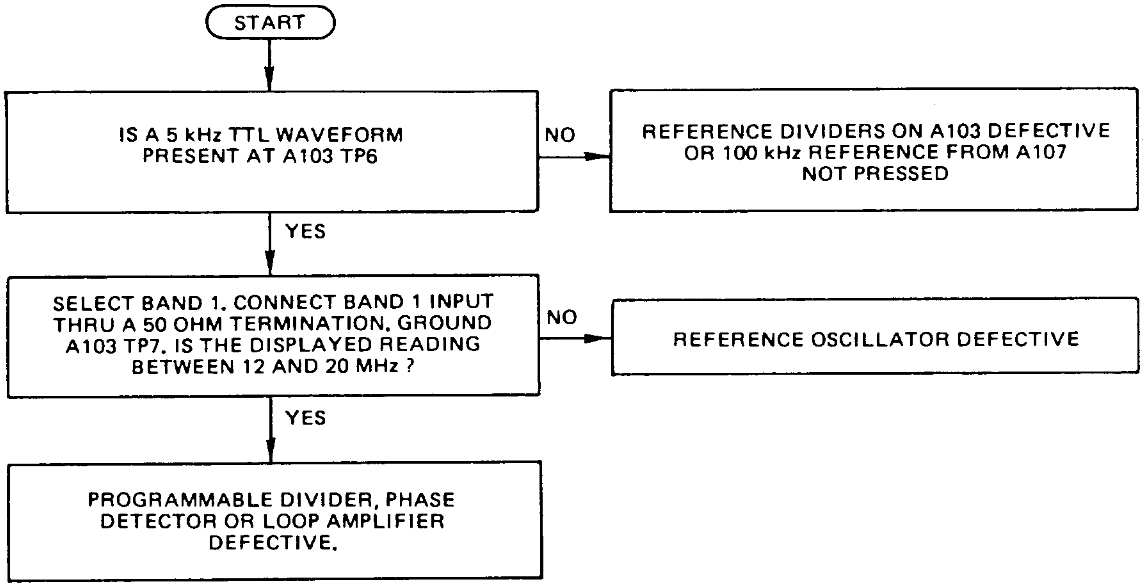


Figure 6-20. Reference Loop

Section 7
Adjustments and Calibrations

GENERAL

To correctly adjust the 575B or 578B counter use the following procedures. Adjustments should only be made if the counter does not operate as specified, or following the replacement of components. If the adjustments do not result in the performance specified then refer to the troubleshooting section of this manual. The test equipment required is:

MANUFACTURER	MODEL	DESCRIPTION	CRITICAL PARAMETERS
Tektronic	475	Oscilloscope	General Purpose
Fluke	8050A	D.V.M.	41/4 digit resolution
H.P.	182C, 8559A	Spectrum Analyzer	125 MHz
Wavetek	2002	Sweeper	10 MHz - 2 GHz
EIP	931	Microwave Source	1 - 20 GHz
H.P.	8690A, 8696A	Microwave Sweeper	20 GHz - 26.5 GHz
EIP	2000017	Service Kit	See Appendix A (A-3)

POWER SUPPLY ADJUSTMENTS

Prior to making any adjustments to the power supply the counter should warm up at least 20 minutes.

Voltages are measured on the back of the Interconnect board (A100), or on the back of the Power Supply board (A101).

1. Connect the Digital Volt Meter (DVM) between ground and +12V.
2. Adjust A101 R5 until the voltage measures +12.000 VCD ± .010 VDC.
3. Connect the DVM between ground and -12 V.
4. Adjust A101 R17 until the voltage measures -12.000 VDC ± .010 VDC.

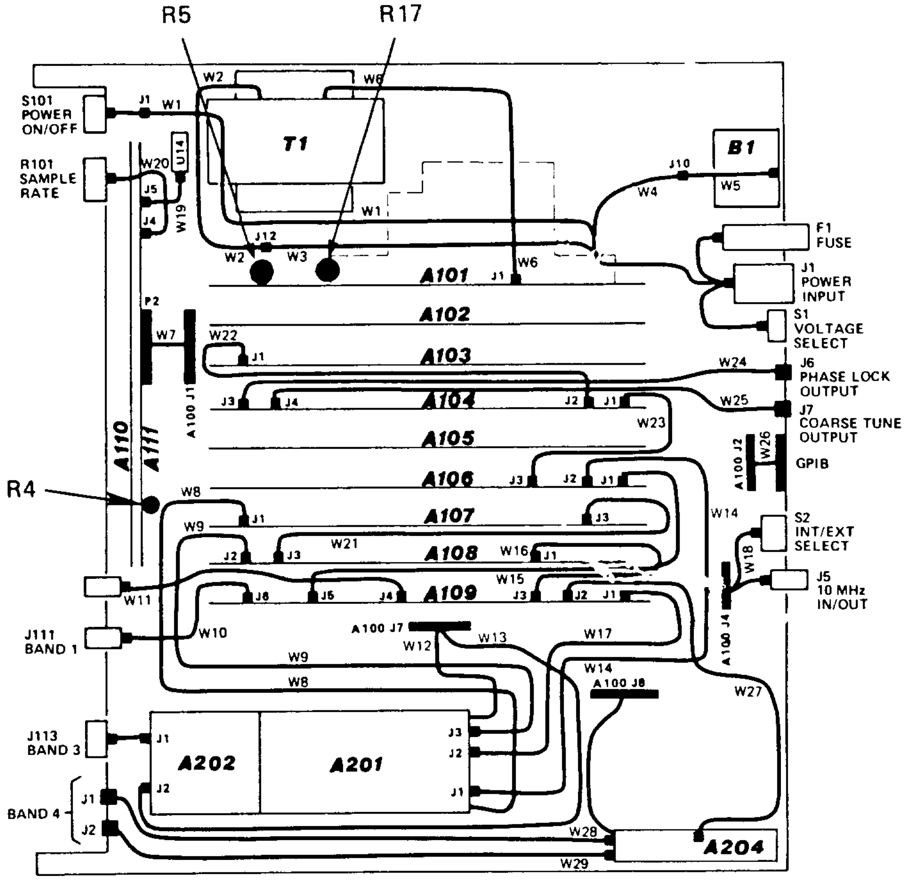


Figure 7-1. Adjustment Locations.

YIG DAC CALIBRATION PROCESS

THEORY

The purpose of this process is to compensate the nonlinearity of the YIG and DAC error. The process allows a software route start in the EEPROM. The instrument generates a YIG DAC correction table, which resides in EEPROM. After the YIG searches for and centers on a signal, the software corrects the DAC reading (not the DAC itself) according to the correction table. This process yields the true YIG frequency. Then the program tunes the VCO according to the true YIG frequency instead of the ERROR DAC reading.

Each entry of the correction table contains two values:

(1) the YIG frequency and
(2) the DAC reading

Each value consists of 2 bytes. The YIG frequency is represented in hex in 2 MHz increments. For example, if the YIG frequency is 1 GHz then:

1 GHz = 1000 MHz = 2 * 500 MHz = 2 * 01F4 (hex)

and "01F4" is what is written to the table.

The table looks like this:

entry 1	YIG freq 1	DAC reading 1*
entry 2	YIG freq 2	DAC reading 2
. . .	. . .	. . .
. . .	. . .	. . .
entry N	YIG freq n	DAC reading n*

where N must be **at least 2 and can be as much as 248.** *The values in entry 1 and N are extrapolated.

YIG DAC CORRECTION TABLE

Given a DAC reading D, the software first searches through the second row of the table. If D is equal to an exact DAC reading in entry n, where 1 <= n <= 248, then the software generates the corresponding YIG frequency reading. If D falls between 2 consecutive DAC readings in entry p and q, where 1 < = p < q < = 248, then the software uses a linear interpolation algorithm to find the corresponding YIG frequency Y as shown in the following equation:

If:

$$\frac{\text{DAC q} - \text{DAC p}}{\text{YIG q} - \text{YIG p}} = \frac{\text{D} - \text{DAC p}}{\text{Y} - \text{YIG p}}$$

then Y is:

$$Y = (D - DAC\ p) * \frac{YIG\ q - YIG\ p}{DAC\ q - DAC\ p} + YIG\ p$$

NOTE

When Y is being calculated, the multiplication is performed before the division to avoid precision error.

If for some reason the instrument cannot find a suitable DAC reading entry, ERROR #40 is generated to indicate error in the correction table.

CORRECTION TABLE SETUP

Setting up the correction table is actually the YIG DAC calibration process. The user enters "Test 90" to activate the process. At first the table contains two entries:

	YIG frequency	DAC number
default 1	0	0 hex
default 2	3FFF hex	3FFF hex

The user applies a synthesized signal Y1 GHz to the counter, then enters Y1 GHz through the counter's front panel or via GPIB. After the user enters the number, a routine converts that number to hexadecimal, stores it to the table as the YIG frequency of entry #2, and shifts the original entry #2 to entry #3. Then the counter sweeps the YIG to look for the signal and center the YIG on it. If the searching and centering are successful, the DAC number D1 is read and stored as DAC # of entry #2 of the table. Now the table looks like this:

default 1	0	0
entry 1	Y1	D1
default 2	3FFF	3FFF

The user can repeat the above sequence up to 246 times with the following restrictions:

(1) the sequence must be repeated at least two times.

(2) the frequency entered must be greater than the previous frequency.

If either of the two requirements above are not fulfilled or the counter cannot center the YIG on the signal, the whole process is aborted and the correction table is not altered.

After N repetitions, the correction table will be as follows:

default 1.	0	0
entry 1.	Y1	D1
entry 2.	Y2	D2
. . .	. . .	. . .
entry N-1.	Y N-1	D N-1
entry N.	YN	DN
default 2.	3FFF	3FFF

where 2 <= N <= 246.

Since default values are used for the first and the last entry, they must be corrected before the user exits the calibration process. The software accomplishes this task by using Y1, Y2, D1, D2 to extrapolate default 1 and Y N-1, YN, D N-1, DN to extrapolate default 2.

The equation is :

$$Y = \frac{D * (Y2 - Y1) + Y1 * D2 - Y2 * D1}{D2 - D1}$$

The final correction table looks like this:

extrapolated entry 0.	Y0	D0
entry 1.	Y1	D1
entry 2.	Y2	D2
. . .	. . .	. . .
entry N-1	Y N-1	D N-1
entry N	YN	DN
extrapolated entry N+1	Y N+1	Y N+1

where 2 <= N <= 246.

FORMAT AND ADDRESS OF THE CORRECTION TABLE

The correction table resides in EEPROM.

Address: 0C00 hex

Format:

yyyy dddd yyyy dddd .... yyyy dddd FFFF FFFF EEEE

where	"yyyy"	means 2 bytes of YIG frequency
	"dddd"	means 2 bytes of DAC reading
	"FFFF FFFF"	represents 4 bytes of end of table mark and
	"EEEE"	means for software usage.

NOTE

Before performing this procedure A108 S-1 must be open. (A108 U4 Pin 17 will be high). After calibration, S1 must be on (A108 U4 P17) low to protect calibration.

CALIBRATION PROCEDURE

Manual Calibration

1. Press "BAND 3" on the front panel.
2. Press "TEST 90" on front panel. the counter will then display "F01".
3. Apply a synthesized 1-GHz signal at 0 dBm to Band 3 of the counter.
4. Enter "1" and press "GHz" on the front panel.
5. Counter should display "F02".
6. Apply a synthesized 1.3-GHz signal at 0 dBm to Band 3 of the counter.
7. Enter "1", ".", "3" and press "GHz" on the front panel.
8. Counter should display "F03".
9. Apply a synthesized 10-GHz signal at 0 dBm to Band 3 of the counter.
10. Enter "1", "0" and press "GHz" on the front panel.
11. Counter should display "F04".
12. Apply a synthesized 20-GHz signal at 0 dBm to Band 3 of the counter.
13. Enter "1", "8" and press "GHz" on the front panel.
14. Counter should display "F05".
15. **Go to step 28 if the model of the counter is 535B/575B/575B.**
16. Apply a synthesized 22-GHz signal at 0 dBm to Band 3 of the counter.
17. Enter "2", "2" and press "GHz" on the front panel.

18. Counter should display "F06".

19. Apply a synthesized 24–GHz signal at 0 dBm to Band 3 of the counter.

20. Enter "2", "4" and press "GHz" on the front panel.

21. Counter should display "F07".

22. Apply a synthesized signal 25.5 GHz at 0 dBm to Band 3 of the counter.

23. Enter "2", "5", ".", "5" and press "GHz" on the front panel.

24. Counter should display "F08".

25. Apply a synthesized signal 26.5 GHz at 0 dBm to Band 3 of the counter.

26. Enter "2", "6", ".", "5" and press "GHz" on the front panel.

27. Counter should display "F09".

28. Press **''CLEAR DATA"** to abort the process, or press **''CLEAR DISPLAY"** to exit the process.

NOTE:

If the counter can not find or center on the signal, it will display an ERROR #42 message.

NOTE:

The above frequencies are required to calibrate the counter. Other frequencies are at user's choice.

Calibration using GPIB controller.

1. Output "B3TA90" to the counter.

2. Command the signal source to generate 1 GHz at 0 dBm.

3. Output "1G" to the counter.

4. Command the signal source to generate 1.3 GHz at 0 dBm.

5. Output "1.3G" to the counter.

6. Command the signal source to generate 10 GHz at 0 dBm.

7. Output "10G" to the counter.

8. Command the signal source to generate 20 GHz at 0 dBm.

9. Output "18G" to the counter.

10. Go to step 19 if the model of the counter is 535B/575B/575B.

11. Command the signal source to generate 22 GHz at 0 dBm.

12. Output "22G" to the counter.

13. Command the signal source to generate 24 GHz at 0 dBm.
14. Output "24G" to the counter.
15. Command the signal source to generate 25.5 GHz at 0 dBm.
16. Output "25.5G" to the counter.
17. Command the signal source to generate 26.5 GHz at 0 dBm.
18. Output "26.5G" to the counter.
19. Output "C" to exit the calibration process or "D" to abort the process.

NOTE:

When the counter has acquired the signal and is ready to accept the next frequency, the GPIB status byte bit 0 will be set to 1. This can be recognized through service request.

TIME BASE CALIBRATION

NOTE

For Option 03, 04, 05, refer to Option Section of Manual.

It is important to note that the precision of the time base calibration directly affects overall counter accuracy. Reasons for recalibration, and the procedures to be used, should be thoroughly understood before attempting any readjustment.

The fractional error in the frequency indicated by the counter is equal to the negative of the fractional frequency error of the Time Base Oscillator with respect to its true value. That is:

$$\frac{\Delta f_s}{f_s} = \frac{\Delta f_t}{f_t}$$

where f_s is the true frequency of the measured signal, and f_t is the true frequency of the Time Base Oscillator. Thus, the inaccuracy associated with a frequency measurement is directly related to the quality of the Time Base Oscillator, and a measure of the precision with which it was originally adjusted.

TEMPERATURE COMPENSATED CRYSTAL OSCILLATOR (TCXO)

The standard time base oscillator used in the counter is a TCXO (A113). The range of the actual measured frequencies of the oscillator will differ by no more than 1 parts in 10^6 if the temperature is slowly varied from 0 to +50 degrees C.

With a stable input frequency, the measurement indicated by the counter will fluctuate in proportion to the TCXO drift. To center this fluctuation on the true value of the measured signal, each TCXO has imprinted on its side the frequency setting required at +25 degrees C.

At approximate room temperature (+25 degrees C), the slope of the frequency vs. temperature curve is normally no worse than $\pm 1 \times 10^{-7}$ parts per degree C. When the counter is used in an ordinary laboratory environment, the TCXO may be set as close to 10,000,000 Hz as desired. In this environment, a peak-to-peak temperature variation of 5^0 C will result in a measured signal error of no more than $\pm 2.5 \times 10^{-7}$ parts. This signal error is due to the temperature characteristics of the Time Base Oscillator.

The natural aging characteristics of the crystal in the Time Base Oscillator can also cause inaccurate signal measurements. Aging refers to the long term, irreversible change in frequency (generally in the positive direction) which all quartz oscillators experience. The magnitude of this frequency fluctuation in the TCXO is as specified. This may improve when in continuous operation.

Error due to aging adds directly to error due to temperature. The number of times the counter requires recalibration depends on the environment in which the counter operates, and upon the level of accuracy required.

For example, if the counter is subjected to the full operation temperature range one month after proper initial adjustments, the inaccuracy could vary from $+1.3 \times 10^{-6}$ parts to -0.7×10^{-6} parts.

TCXO CALIBRATION PROCEDURES

METHOD 1 (with accurate frequency counter)

1. Remove top cover of counter. Connect counter to reliable power source. Note ambient temperature.

2. Measure the frequency of the TCXO (at the rear panel 10 MHz connector) with a second counter of known calibration accuracy.

3. Adjust the TCXO by turning the calibration screw on the TCXO case until the measured frequency equals that shown on the TCXO calibration label.

METHOD 2 (with accurate frequency source)

1. Apply a 10 000 000 Hz signal from a frequency standard (or other oscillator of suitable accuracy and stability) to the Band 1 input of the counter.

2. Press RESOL 0 (1 Hz resolution)

3. Adjust the TCXO until the reading on the counter is offset from 10 000 000 Hz by the negative of the frequency shown on the TCXO. For example, if the TCXO calibration label shows a frequency of 10 000 003 Hz, adjust the TCXO until the counter displays 9 999 997 Hz.

DISPLAY INTENSITY

On the front panel logic assembly (A111), R4 may be adjusted to provide the most comfortable display intensity.

Section 8
Performance Tests

GENERAL

These tests are for the basic counter. Performance tests for options are in Section 10. These tests will enable the user to verify that the counter is operating within specifications.

VARIABLE LINE VOLTAGE

During the performance tests, the counter should be connected to the power source, through a variable voltage device, so that line voltage may be varied ±10% from nominal. This will assure proper operating of the counter under various supply conditions.

REQUIRED TEST EQUIPMENT (or equivalent)

MANUFACTURER	MODEL	DESCRIPTION	CRITICAL PARAMETERS
H.P.	651B	Signal Generator	10 Hz - 10 MHz
Wavetek	2002	Sweeper	10 MHz - 2 GHz
EIP	931	Microwave Source	1 GHz - 20 GHz
H.P.	8690A, 8696A	Microwave Sweeper	20 GHz - 26.5 GHz

BAND 1
(10 Hz - 100 MHz)

1. Set the counter to Band 1.
2. Connect the signal source output, through a 50 ohm shunt feedthrough resistor, to the Band 1 input on the counter.
3. Set the signal level to 25 mv RMS (-19 dBm into 50 ohms).
4. Vary the signal from 10 Hz to 100 MHz (changing signal source as required). The counter should display the correct input frequency.
5. Connect the phase lock output to the phase lock input of the signal source.
6. Set the signal source for an input of 50 MHz.
7. Phase lock the counter at 10 MHz, 50 MHz, and 100 MHz. Verify that the counter phase locks.

BAND 2
(10 MHz - 1 GHz)

1. Set the counter to Band 2.
2. Connect the signal source output to the Band 2 input of the counter.
3. Set the signal level to -20 dBm (22 mv RMS).
4. Vary the signal input from 10 MHz to 1 GHz.
   (The counter should display the correct input frequency.)
5. Set the source frequency to within 50 MHz of the following lock frequencies: 100 MHz, 500 MHz, and 1 GHz. Verify that the counter phase locks.

BAND 3
(578B: 1 GHz - 26.5 GHz)
(575B: 1 GHz - 20 GHz)

1. Set the counter to Band 3.
2. Connect the signal source output to the Band 3 input of the counter.
3. Vary the signal frequency from 1 GHz to 20/26.5 GHz (changing the signal source as required) at the following levels.

1 GHz - 1.2 GHz	-25 dBm (12 mv RMS)
1.2 GHz - 12.4 GHz	-30 dBm (7 mv RMS)
12.4 GHz - 20 GHz	-25 dBm (12 mv RMS)
20 GHz - 26.5 GHz	-20 dBm (22 mv RMS)

The counter should display the correct input frequency.

4. Connect the coarse tune output and the phase lock output to the signal source.
5. Phase lock the counter at 2 GHz, 10 GHz, and 20 GHz. Verify that the counter phase locks.

Section 9
Functional Description and Illustrated Parts Breakdown

This section contains a functional description, a parts list, an illustration and a schematic diagram for each printed circuit board used in this counter.

The parts list is broken down by types of components, listed in alphanumeric sequence. The components that have a different reference designator (REF DES), but have the same EIP part number, are described for the first such component listed. Subsequent descriptions of that component will refer to the first entry. The total number of like components used on the same assembly will be listed with the first entry in the column identified as UNITS PER ASSY.

The last two columns of the parts list will supply the name of the manufacturer and their Federal Supply Code for Manufacturers (FSCM) number. (See Appendix B.)

Pages 9-3 through 9-7 contain the top assembly of the counter and other basic information. After page 9-7 you will note that the page numbers have a three digit first number followed by a dashed number. The three digit number reflects the number of the assembly being described on those pages. The dashed number is the page sequence for that assembly description. For example, pages 105-1 through 105-5 all relate to the A105 printed circuit board assembly.

REFERENCE DESIGNATORS

A	Assembly	Q	Transistor
B	Battery or Fan	R	Resistor
C	Capacitor	S	Switch
CR	Diode	T	Transformer
DS	Indicator (display)	TP	Test Point
F	Fuse	U	Integrated Circuit
J	Jack or Connector	X	Socket or Holder
K	Relay		
L	Inductor		
P	Plug or PCB contacts		

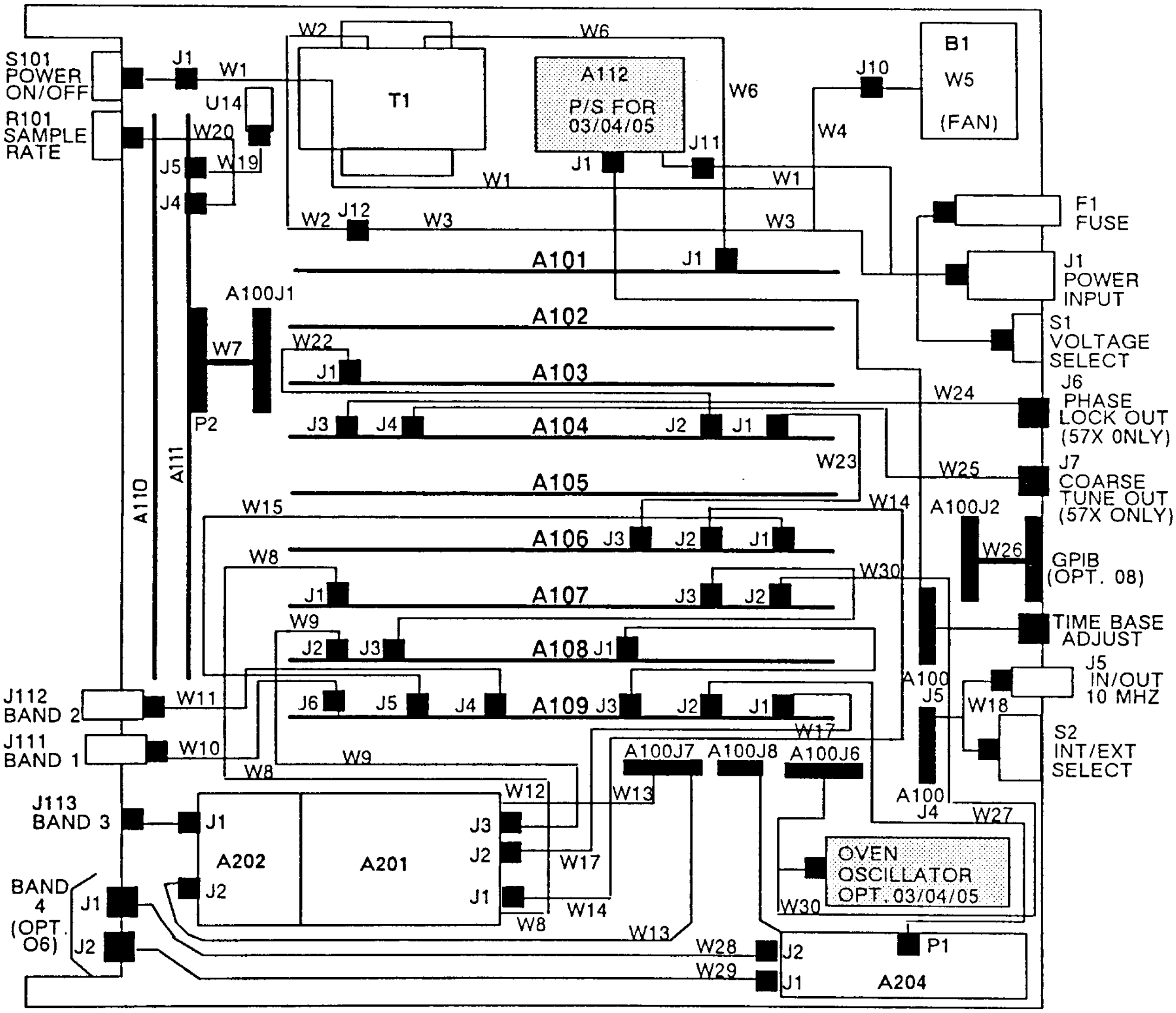


Figure 9-1. Assembly Locations and Cable Connections in Counter

CABLE CONNECTION GUIDE

FROM	CABLE	TO	FROM	CABLE	TO
A1S101J1	W1	A1S1, F1,J1	A108J1	W16	A109J3
A1J12	W2	A1T1	A109J1	W17	A201J2
A1S1	W3	A1J12	A1J5,S2	W18	A100J4
A1J10	W4	A1S1	A1U14	W19	A111J5
A1B1	W5	A1J10	A1R101	W20	A111J4
A101J1	W6	A1T1	A107J3	W21	A108J3
A111P2	W7	A100J1	A103J1	W22	A104J2 (57X ONLY)
A107J1	W8	A201	A104J1	W23	A106J3 (57X ONLY)
A108J2	W9	A201J3	A104J3	W24	A1J6 (57X ONLY)
A1J111	W10	A109J6	A104J4	W25	A1J7 (57X ONLY)
A1J112	W11	A109J4	A100J2	W26	A1,GPIB (OPT. 08)
A201	W12	A100J7	A204P1	W27	A109J2 (BAND 4, OPT 06)
A202J2	W13	A100J7	A204J2	W28	A1J1 (BAND 4, OPT 06)
A106J2	W14	A201J1	A204J1	W29	A1J2 (BAND 4, OPT 06)
A106J1	W15	A109J5	A107J2	W30	A100J6 (OPT. 03/04/05)

575B/578B SOURCE LOCKING MICROWAVE COUNTER

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
	COUNTER, MODEL 575B	2000014-03		EIP	34257
	MODEL 578B	2000015		EIP	34257
1	**FRONT PANEL ASSY**	2010674-01	1	EIP	34257
	Overlay, 575B	5210252	1	EIP	34257
	Overlay, 578B	5210253	Ref	EIP	34257
A1R101	Sample Rate Control Assy	2010134-01	1		
	Switch,Power	2010187-02	1		
	Knob, Knurled	5210223	1	5000160	31013
	Button Set, 12 + 9	5210220	1	5230005-02	
	Alignment Pin	5210190	2		
	Retainer Key	5210191	1		
	Panel	5210378	1		
-2	**REAR PANEL ASSY**	2010219-01	1		
	Panel	5210379	1		
	Conn, BNC	2610024	1	KC7935	91836
	Conn, Filter	2650005	1	3EF1	05245
	Switch, Toggle SPDT	4510001	1	7101H	09353
A1S1	Switch, Voltage Select	2010159-03	1		
	Fuse Carrier	5000171	1	031-1666	
	Fuse Holder	5000170	1	031-1653	
	Fuse, 1A, SB, 250V	5000085	1	MDL-1A	71400
	Fuse, .500A, 250V	5000169	1	FST034-3114	71400
-3	FAN ASSY	2010136-01	1		
	Fan, 115 Volt AC	5000151	1	760/126LF/182/1115	
	Conn, Plug, 3 Pin	2620110	1	03-06-2032	
	Contact, Male	2620038	2	02-06-2103	
	Spacer	5210016	2		
-4	**FRAME KIT**	2010151-01	1		
	Panel, Side, Enclosure	5210210	2		
	Trim, Front Post	5220004	2		
	Trim, Handle	5220025	2		
	Frame	5210248	2		
	Corner Post, Front	5250001	2		
	Corner Post, Rear	5250002	2		
	Handle, Enclosures	5250011	2		
	Label, Keyboard Operation Guide (LH)	5560113-00	1		
-5	Lable, Keyboard Operation (LH) Guide (RH) (RH)	5560113-01	1		
-5	**TRANSFORMER, ASSY, A1T1**	2010359-01	1		
	Transformer, Power	4900005	1		
	Conn, Plug, 9 pin	2620112	1	03-06-2092	0000A
	Conn, Housing, 6 pin	2620129	Ref	640427-6	AMP
	Contact, Male	2620038	7	02-06-2103	0000A
	Contact, Female	2620036		02-06-1103	0000A
-6	**FRONT CARD GUIDE ASSY**	5210199	1	5210199	
-7	**REAR CARD GUIDE ASSY**	5210200	1		
-8	**TOP COVER ASSY**	2010212-01	1		
-9	**BOTTOM COVER**	5210209	1		
-10	**TILT BAIL**	5000055	1		
-11	Foot, Plastic Enclosure	5220003	4		
-12	Line Cord Set - Domestic	5440002	1		
	Line Cord Set - Export	5440017	1		

575B/578B SOURCE LOCKING MICROWAVE COUNTER (continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
	PCB ASSEMBLIES			**See Page No.:**	
A100	Counter Interconnect	2020180-01	1	100-1	
A101	Power Supply	2020131-01	1	101-1	
A102	GPIB	2020133-02	1	102-1	
A103	Reference Loop/DAC	2020201-03	1	103-1	
A104	Phase Lock	2020202-02	1	104-1	
A105	Microprocessor	2020215-02	1	105-1	
A106	Count Chain	2020136-03	1	106-1	
A107	Gate Generator	2020197-09	1	107-1	
A108	Converter Control	2020200-04	1	108-1	
A109	Band 2 Converter	2020139-05	1	109-1	
A110	Display & Keyboard	2020140-02	1	110-1	
A111	Front Panel Logic	2020191-02	1	111-1	
A203	Microwave Converter, Band 3	2010241	1	Shown for reference only	
	Voltage Control Usc.				
	Amplifier				
	:rowave				
	Microwave Converter, Ban				
	CABLES				
W1	A1S101J1 to A1S1, F1, J1	2010159-01			
W2	A1J12 to A1T1	2010155-01			
W3	A1S1 to A1J12	2010159-01			
W4	A1J10 to A1S1	2010159			
W5	A1B1 to A1J10	2010136			
W6	A101J1 to A1T1	2010155			
W7	A111P2 to A100J1	2040169			
W8	A107J1 to A201P3	2040171			
W9	A108J2 to A201J3	2040174			
W10	A1J111 to A109J6	2040165			
W11	A1J112 to A109J4	2040166			
W12	A201 to A100J7	2040170			
W13	A202J2 to A100J7	2040170			
W14	A106J2 to A201J1	2040172			
W15	A106J1 to A109J5	2040210			
W16	A108J1 to A109J3	2040208			
W17	A109J1 to A201J2	2040175			
W18	A1J5, S2 to A100J4	2040167			
W19	A1U14 to A111J5	2040168			
W20	A1R101 to A111J4	2040168			
W21	A107J3 to A108J3	2040227			
W22	A103J1 to A104J2	2040240			
W23	A104J1 to A106J3	2040239			
W24	A104J3 to A1J6	2040241			
W25	A104J4 to A1J7	2040242			
W26	A100J2 to A1, GPIB	2040177			
W27	A204P1 to A109J2	2040213			
W28	A204J2 to A1J1	2040231		REVISION LEVEL OF	
W29	A204J1 to A1J2	2040232		PROMS MUST BE SPECIFIED	
	PROMS (FOR REFERENCE ONLY)			WHEN ORDERING PROM SET	
A105	BASIC PROM SET	2060003-XX			
-U11	PROM 1, Basic Program	6500026-01	1		
-U12	PROM 2, Basic Program	6500026-02	1		
-U13	PROM 3, Basic Program	6500026-03	1		

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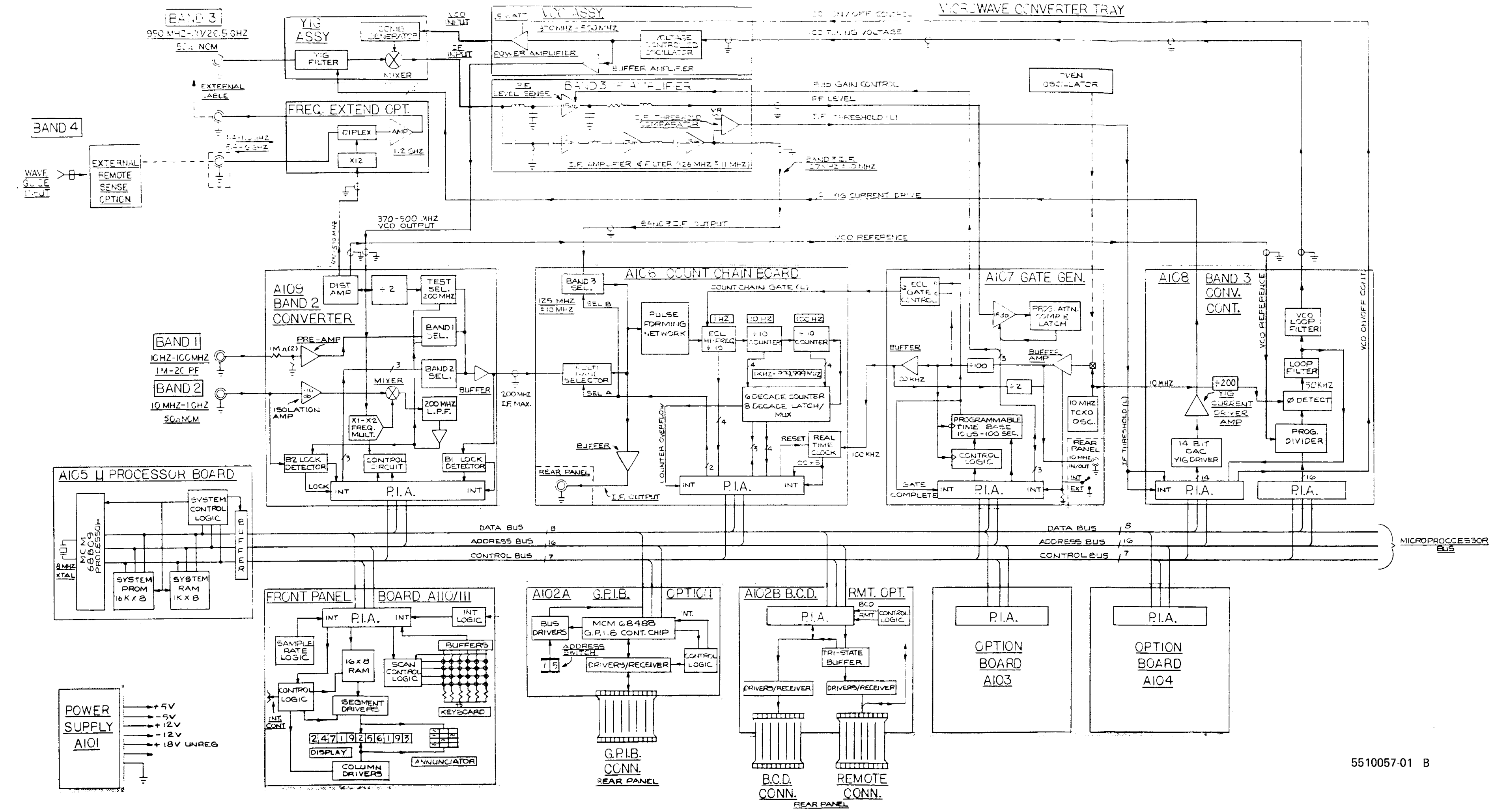

Figure 9-2. 575B/578B Block Diagram

A100
COUNTER INTERCONNECT
(202180)

*FUNCTIONAL
DESCRIPTION
NOT REQUIRED*

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A100 COUNTER INTERCONNECT ASSY

2020180-G

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A100	Counter Interconnect Assy	2020180	1	EIP	34257
J1	Header, Str, 26 pin	2620078	1	3429 - 2302	76381
J2	Header, Str, 50 pin	2620081	2	3433 - 2302	76381
J3	J2				
J4	Friction Lock, 4 pin	2620061	1	09 - 65 - 1049	0000A
J5	Friction Lock, 6 pin	2620090	1	09 - 65 - 1069	0000A
J6	Header, Str, 7 pin	2620186	1	09-64-1071	0000A
J7	Header, Str, 10 pin	2620187	1	09-64-1101	0000A
J8	Friction Lock, 4 pin	2620068	1	640456-4	02660
XA101	Conn, 11 position	2620183	1	5193-442-1	02660
XA102	Conn, 50 position	2620185	1	5193-442-3	02660
XA103 thru XA109	Conn, 30 position	2620184	7	5193-442-2	02660

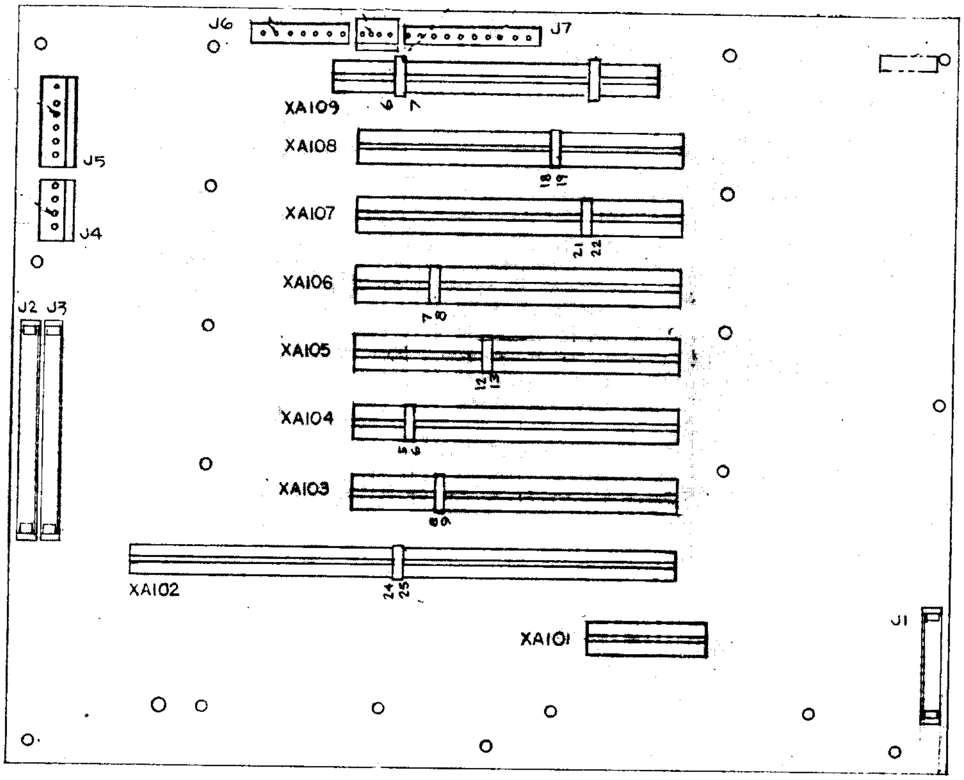
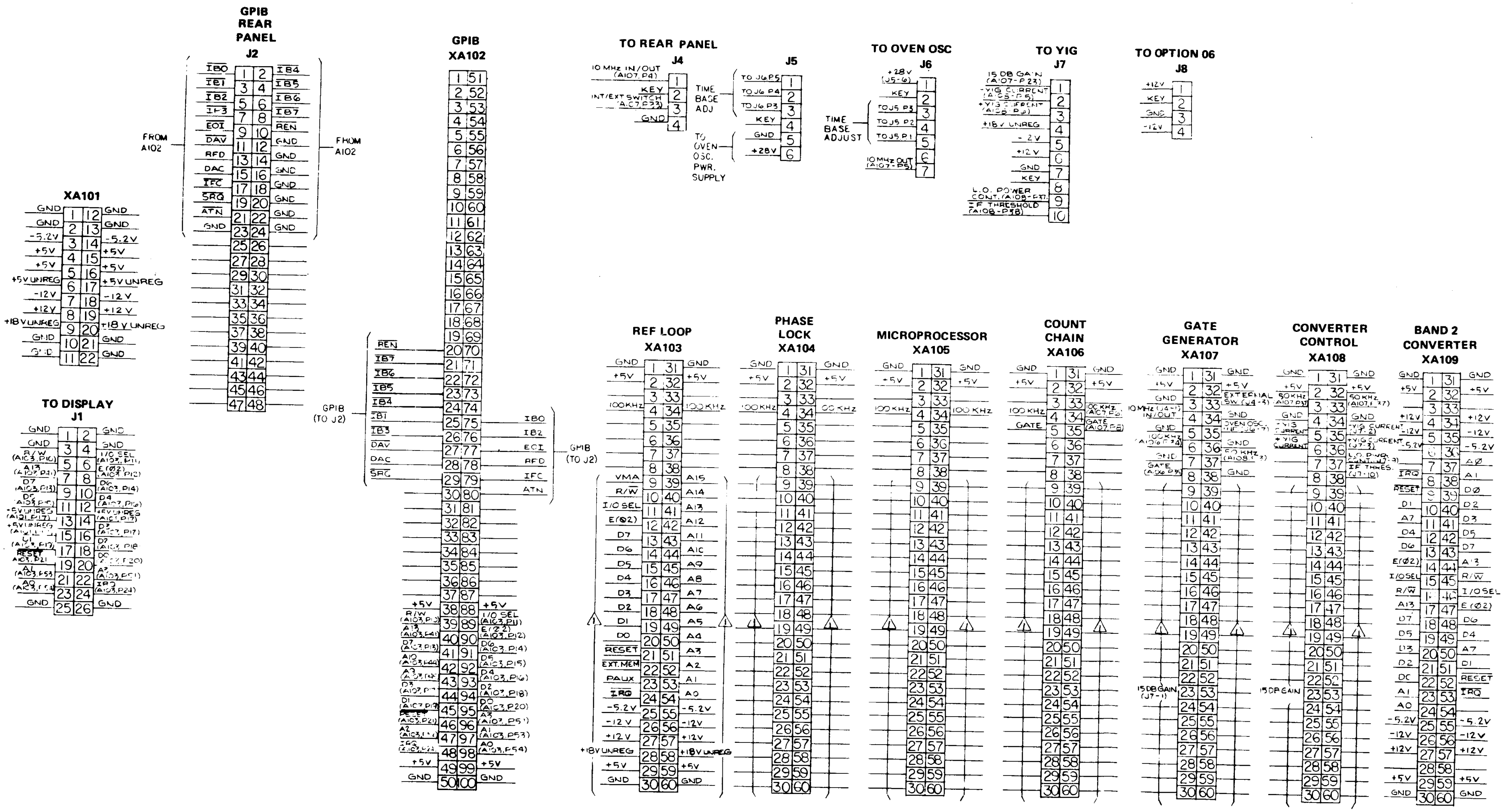


Figure 100-1. Counter Interconnect Component Locator



5500180-00 A

⚠ XA103 THRU XA106 HAVE COMMON CONNECTIONS ON LINES SHOWN IN BRACKETS.

Figure 100-2. Counter Interconnect Schematic

A101
POWER SUPPLY
(2020131)

The power supply furnishes all basic operating voltages required by the counter. The supply consists of two basic sub-assemblies:

- PC Board (A101), containing the rectifiers, filter capacitors, and regulator circuitry.
- Chassis mounted components consisting of the power transformer (T1); primary wiring; F1 fuse (100/120V); the 220/240V power programming switch; and the on/off power switch (S101) mounted on the front panel.

The basic voltages required by the counter are unregulated +18V, regulated +5V, -5.2V, +12V and -12V.

The input AC voltage is full wave rectified and filtered to produce DC voltages of ±9V and ±18V.

The unregulated +18V is used directly as one supply voltage. The +18V is regulated to a +12V by the action of LM305, a series pass transistor (MJE3055), and foldback current limiting circuitry. The -18V is regulated to a -12V by LM304, a series pass transistor, and foldback current limiting circuitry.

The +9V is regulated to +5V by a three terminal regulator containing thermal and current shutdown circuitry. The -9V is also regulated to -5.2V by a three terminal regulator that contains thermal and current shutdown circuitry.

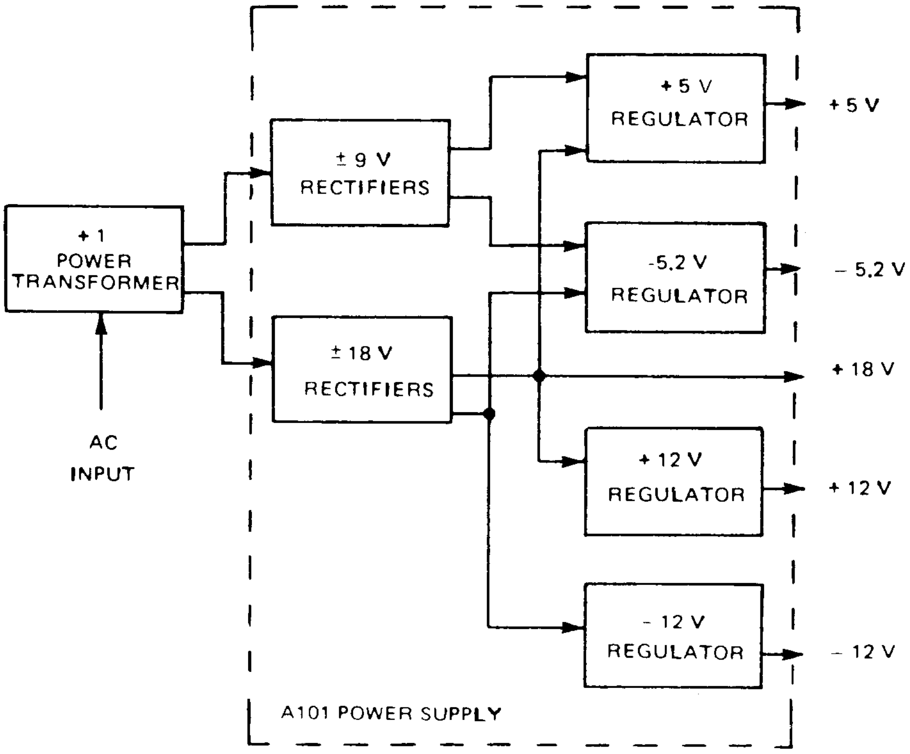


Figure 101-1. Power Supply Function Diagram

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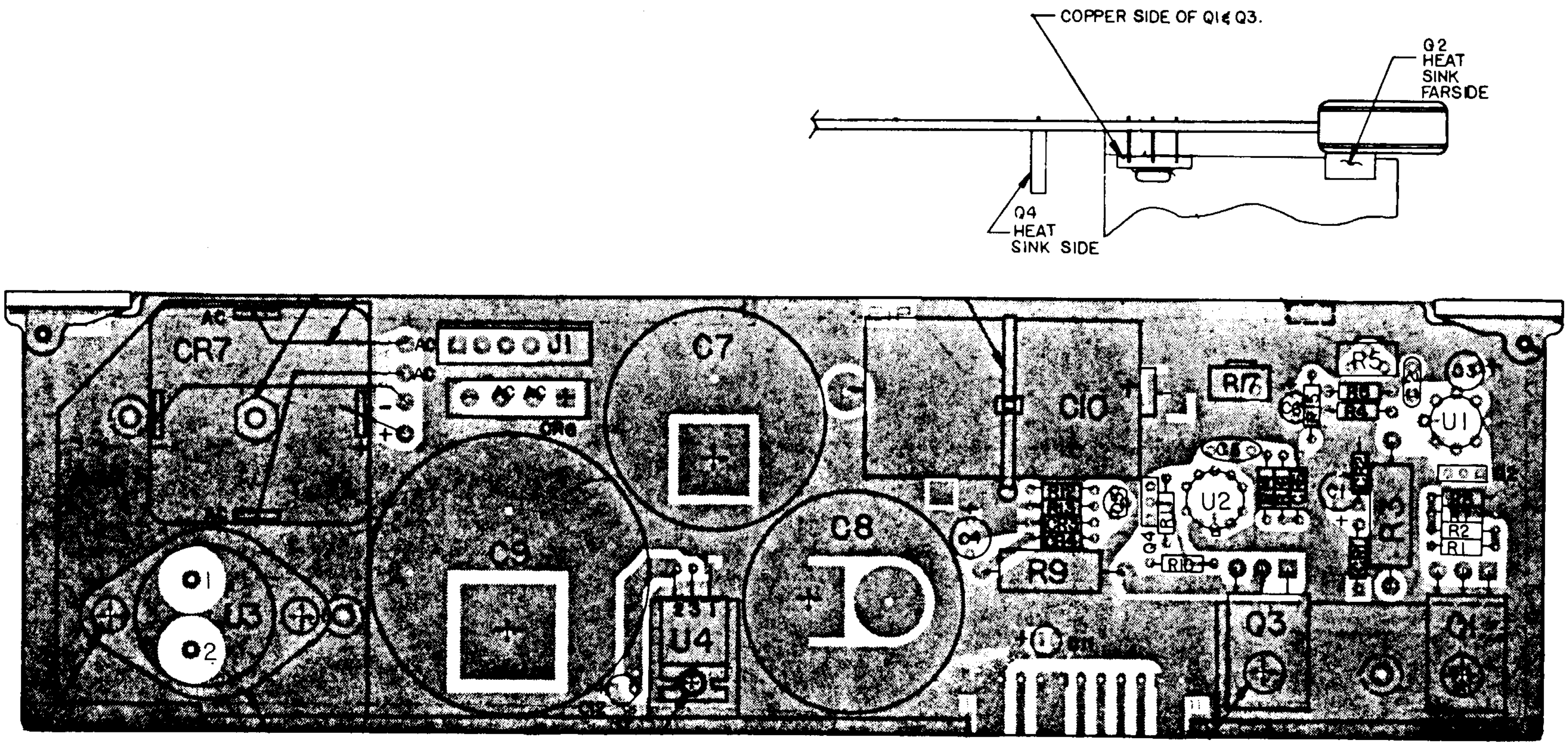
A101 POWER SUPPLY ASSY

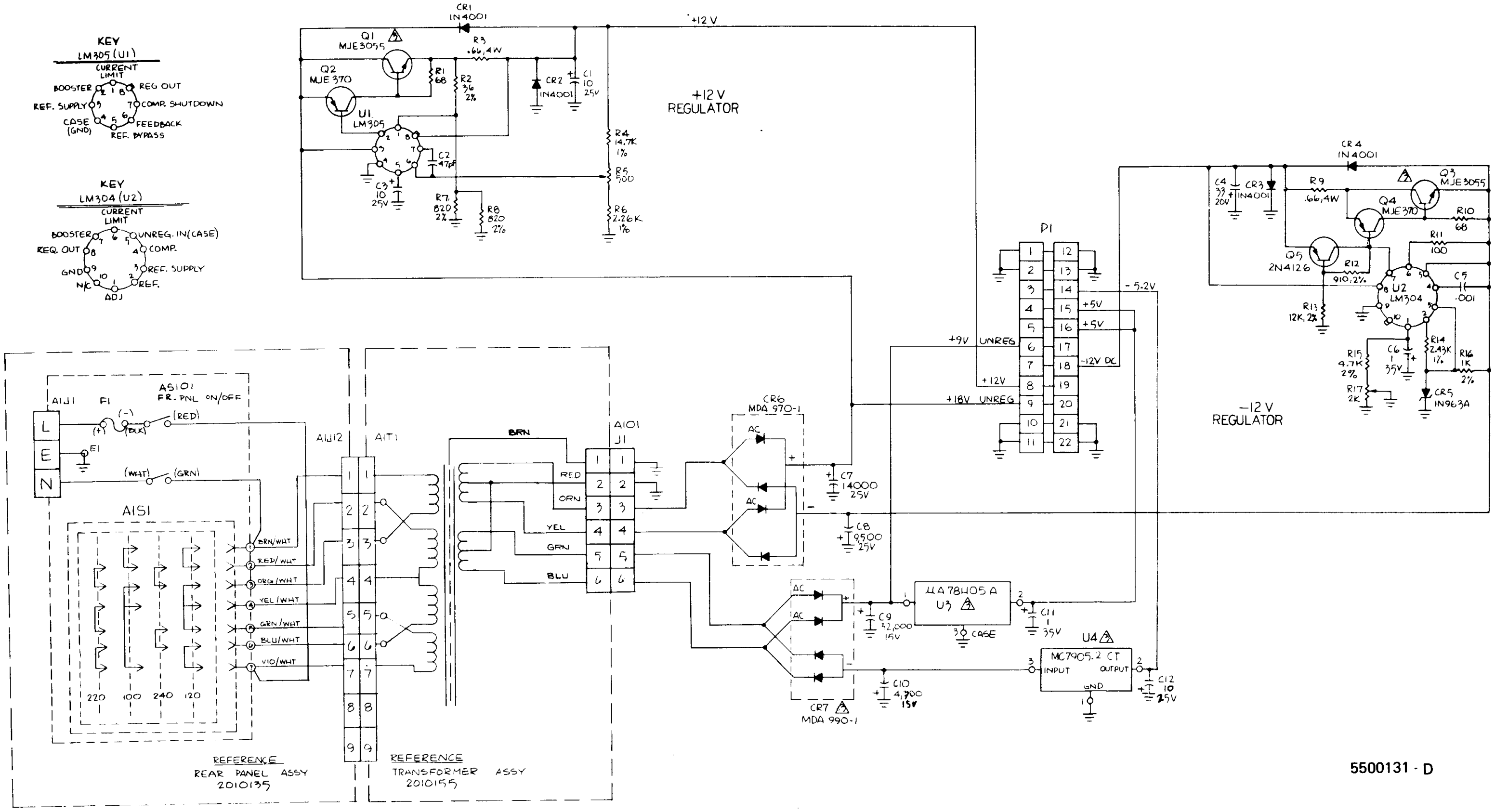
2020131-01 · L

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A101	Power Supply Assy	2020131	1	EIP	34257
C1	Tant. 10μF. 20%. 25V	2300029	3	TAG 20 - 10/25(M)	14433
C2	Mica, 47 pF, 5%, 500V	2260004	1	DM10 - 470J	72136
C3	C1				
C4	Tant, 33μF, 20%, 20V	2300023	1	TAG 20 - 33/20 - 20	14433
C5	Cer, .001μF, 20%, 1KV	2150001	1	SGA - D10	56289
C6	Tant, 1.0μF, 20% 35V	2300008	2	TAG 20 -1.0/35 - 50	14433
C7	Elec, 14,000μF, 25V	2200017	1	3110HB143U025	80031
C8	Elec, 9,500μF, 15V	2200016	1	3110HA952U025	80031
C9	Elec, 32,000μF, 15V	2200019	1	3110RB323U015	80031
C10	Elec, 4,900μF, 15V	220020-00	1	3050JJ4920U15JM	80031
C11	C6				
C12	C1				
CR1 thru CR4	Rectifier	2704001	4	IN4001	07263
CR5	Zener, 12V	2720963	1	IN963A	04713
CR6	Rectifier Brdg	2710029	1	MDA970 - 1	04713
CR7	Rectifier, Brdg	2710028	1	MDA990 - 1	04713
J1	Conn, 6 pin (FRCTN Lock)	2620157	1	640445-6	0000A
Q1	NPN Power	4710001	2	MJE3055	04713
Q2	PNP Power	4710002	2	MJE370	04713
Q3	Q1				
Q4	Q2				
Q5	PNP, General Purpose	4704126	1	2N4126	04713
R1	Comp, 68 ohms, 5%, 1/4 W	4010680	2	RC07GF680J	81349
R2	Met Ox, 36 ohms, 2%, 1/4 W	4130360	1	C4/2%/36	24546
R3	Wire Wound, .66 ohms, 3%, 1/4W	4110012	2	RS - 2	91637
R4	Prec, 14.7K ohms, 1%, 1/8 W	4061472	1	RN55D1472F	81349
R5	Var. Cer., 500 ohm	4250014	1	72XR500	73138
R6	Prec, 2.26K ohms, 1%, 1/8 W	4062261	1	RN55D2261F	81349
R7	Met Ox, 820 ohms, 2%, 1/4 W	4130821	2	C4/2%/820	24546
R8	R7				
R9	R3				
R10	R1				
R11	Comp, 100 ohms, 5%, 1/4 W	4010101	1	RC07GF101J	81349
R12	Met Ox, 910 ohms, 2%, 1/4 W	4130911	1	C4/2%/910	24546
R13	Met Ox, 12K ohms, 2%, 1/4 W	4130123	1	C4/2%/12K	24546
R14	Prec, 2.43K ohms, 1%, 1/8 W	4062431	1	RN55D2431F	81349
R15	Prec, 4.7K ohms, 2%, 1/4 W	4130472	1	C4/2%/4.7	24546
R16	Met Ox, 1K ohms, 2%, 1/4 W	4130102	1	C4/2%/1K	24546
R17	Var, Cer, 2K ohms	4250016	1	72XR2K	73138
U1	Voltage Regulator	3040305	1	LM305	0000X
U2	Voltage Regulator	3040304	1	LM304	0000X
U3	+5VDC Regulator	3057805-01	1	UA78H05A	07263
U4	-5.2 V Regulator	3057905	1	MC7905.2 CT	04713
	Heatsink	5210196	1	EIP	34257



2020131 - L

Figure 101-2. Power Supply Component Locator



△3 CR7,Q1,Q3, ,U3;U4 ARE MOUNTED ON HEATSINKS.

Figure 101-3. Power Supply Schematic

A102
GENERAL PURPOSE INTERFACE BUS
(2020133)

The GPIB assembly makes the 575B/578B counters fully compatible with the IEEE 488-1978 standards. With this assembly, and the PROM (A105 U19), the counter responds to remote control instructions, and can output measurement results.

The most important component on this assembly is the MC 68488 GPIA. It performs all the GPIB bus command decoding, and takes care of the HANDSHAKE processes. The A105 Microprocessor assembly receives and sends device dependent messages to the Interface Bus via GPIA.

The GPIB address of the counter can be set with the two thumb-wheel switches mounted on the board. These address switches are read by the microprocessor only during the initial power-up. When the address switches are read, the data buffer (U8) is enabled by the GPIA, putting the address switch information on the data bus.

U1 through U4 are bus transceivers. They conform to the electrical specifications of the IEEE 488-1978 standard. The open collector mode of operation is chosen for all the drivers.

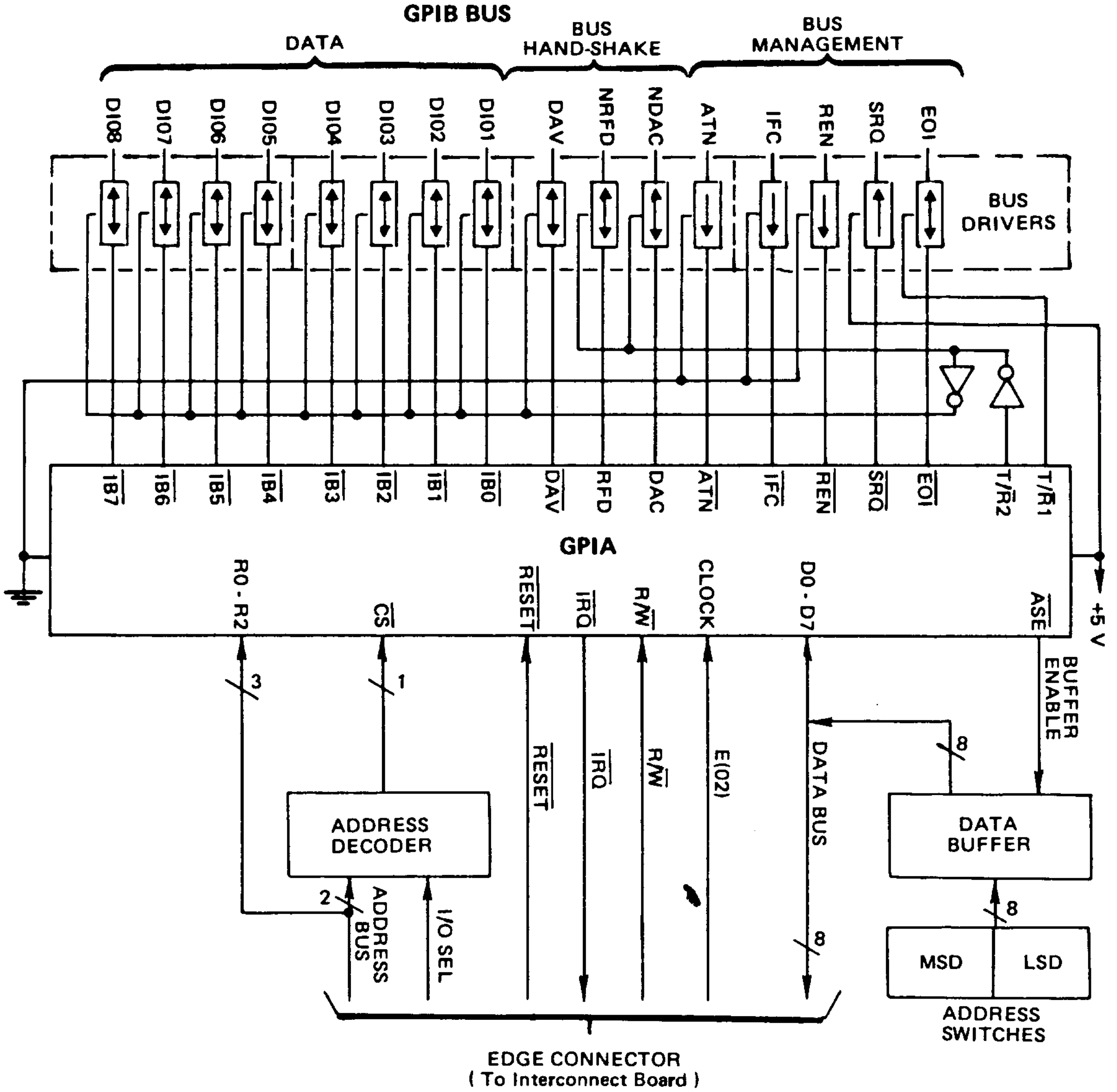


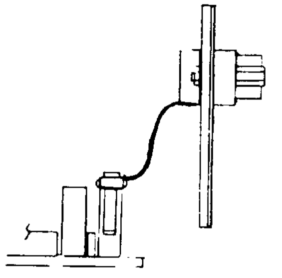
Figure 102-1. GPIB Interface Block Diagram

**ADDRESS CHARACTERS		ADDRESS CODES					
Listen	Talk	binary					decimal
		5	4	3	2	1	*
SP	@	0	0	0	0	0	00
!	A	0	0	0	0	1	01
''	B	0	0	0	1	0	02
#	C	0	0	0	1	1	03
$	D	0	0	1	0	0	04
%	E	0	0	1	0	1	05
&	F	0	0	1	1	0	06
'	G	0	0	1	1	1	07
(	H	0	1	0	0	0	08
)	I	0	1	0	0	1	09
*	J	0	1	0	1	0	10
+	K	0	1	0	1	1	11
,	L	0	1	1	0	0	12
—	M	0	1	1	0	1	13
.	N	0	1	1	1	0	14
/	O	0	1	1	1	1	15
0	P	1	0	0	0	0	16
1	Q	1	0	0	0	1	17
2	R	1	0	0	1	0	18
3	S	1	0	0	1	1	19
4	T	1	0	1	0	0	20
5	U	1	0	1	0	1	21
6	V	1	0	1	1	0	22
7	W	1	0	1	1	1	23
8	X	1	1	0	0	0	24
9	Y	1	1	0	0	1	25
:	Z	1	1	0	1	0	26
;	[	1	1	0	1	1	27
<	/	1	1	1	0	0	28
=	]	1	1	1	0	1	29
>	^	1	1	1	1	0	30

* Decimal Talk/Listen Address is provided as a cross reference for those controllers which use decimal address.

** Address Characters in ASCII Code.

Figure 102-2. Allowable Address Codes



DETAIL A-A

CONTACT	SIGNAL LINE	CONTACT	SIGNAL LINE
1	DIO 1	13	DIO 5
2	DIO 2	14	DIO 6
3	DIO 3	15	DIO 7
4	DIO 4	16	DIO 8
5	EOI	17	REN
6	DAV	18	GND. (6)
7	NRFD	19	GND. (7)
8	NDAC	20	GND (8)
9	IFC	21	GND. (9)
10	SRQ	22	GND. (10)
11	ATN	23	GND. (11)
12	SHIELD	24	GND. LOGIC

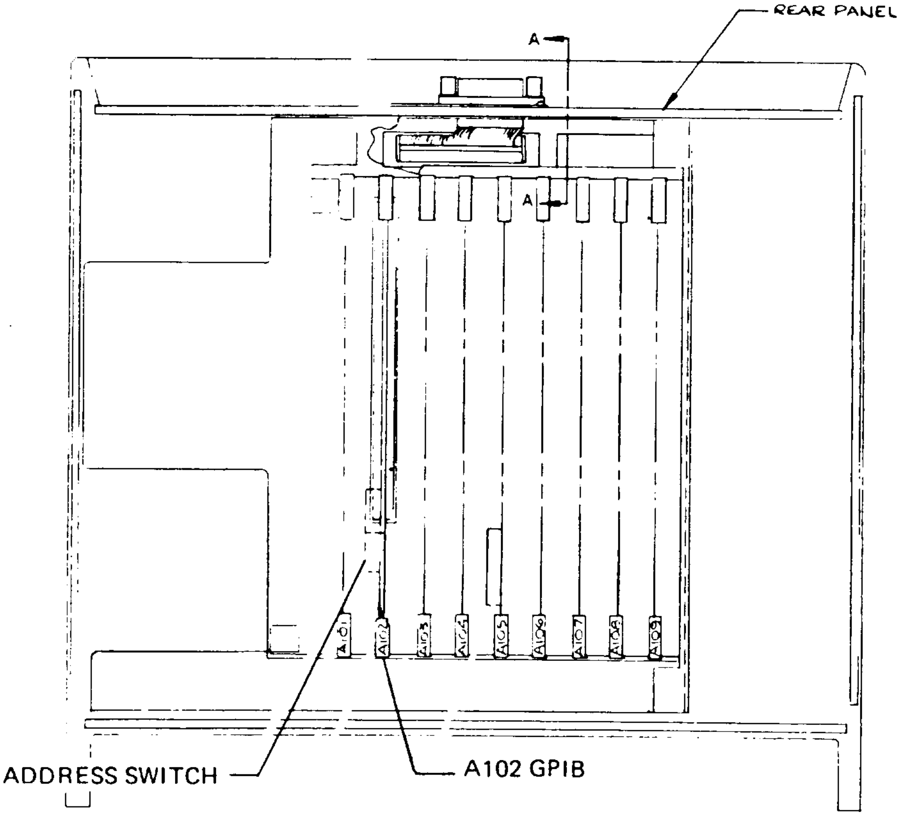


Figure 102-3. Location of GPIB in Counter

A102 GENERAL PURPOSE INTERFACE BUS

2020133-02 A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A102	GPIB PCB ASSY 102B)	2020133	1	EIP	34257
C1	Cer, .01μF, 20%, 100V	2150003	3	TG - S10	56289
C2	C1				
C3	C1				
C4	Tant, 33μF, 10%, 10V	2300015	2	TAG20 - 33/10 - 50	14433
C5	C4				
R1 thru R8	Comp, 5.6K, 5%, 1/4W	4010562	8	RC07GF562J	81349
SW1A and SW1B	Thumbwheel Switch	4540004	2	1X2270 - 0000	
TP1 thru TP6	P.C. pin .040 diameter	2620032	6	460-2970-02-03	71279
U1 thru U4	Quad 3-state Bus Transciever	3053448	4	MC3448	04713
U5	Hex Inverter	3087404	1	74LS04	27014
U6	General Purpose Interface Adaptor	3050027	1	MC68B488P	04713
U7	Tri Input NAND Gate	3087410	1	74LS10	27014
U8	Oct Bus Transciever	3084245	1	74LS245	27014
W26	Cable, Flat Ribbon (Rear Panel to A100 J2)	2040177	1	EIP	34257

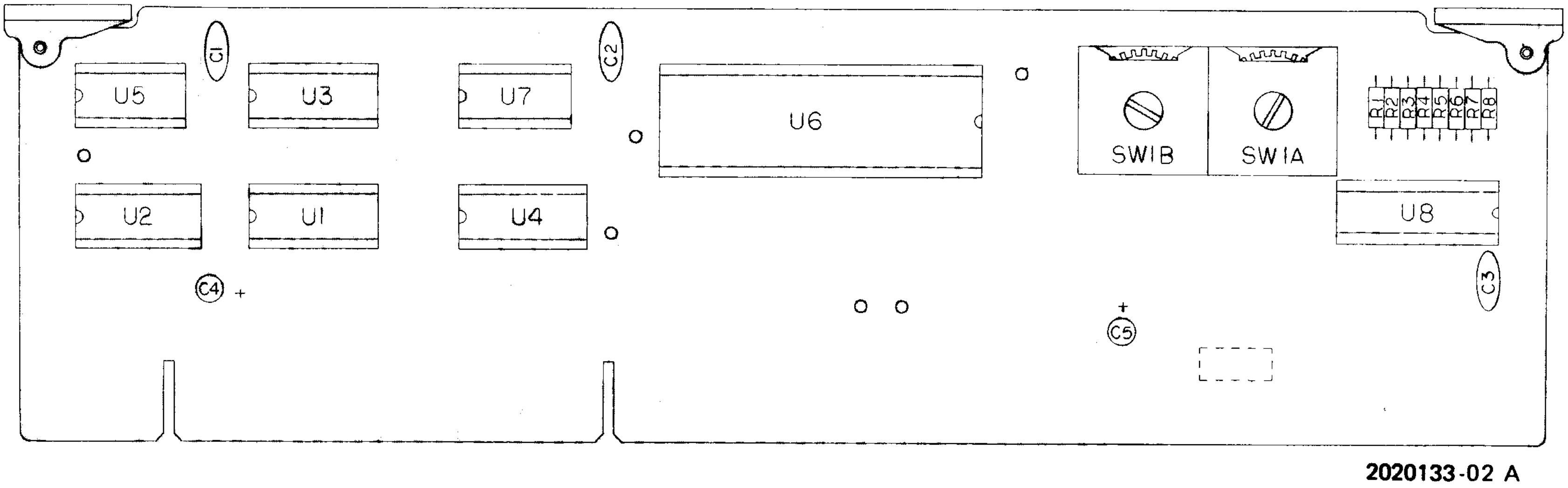
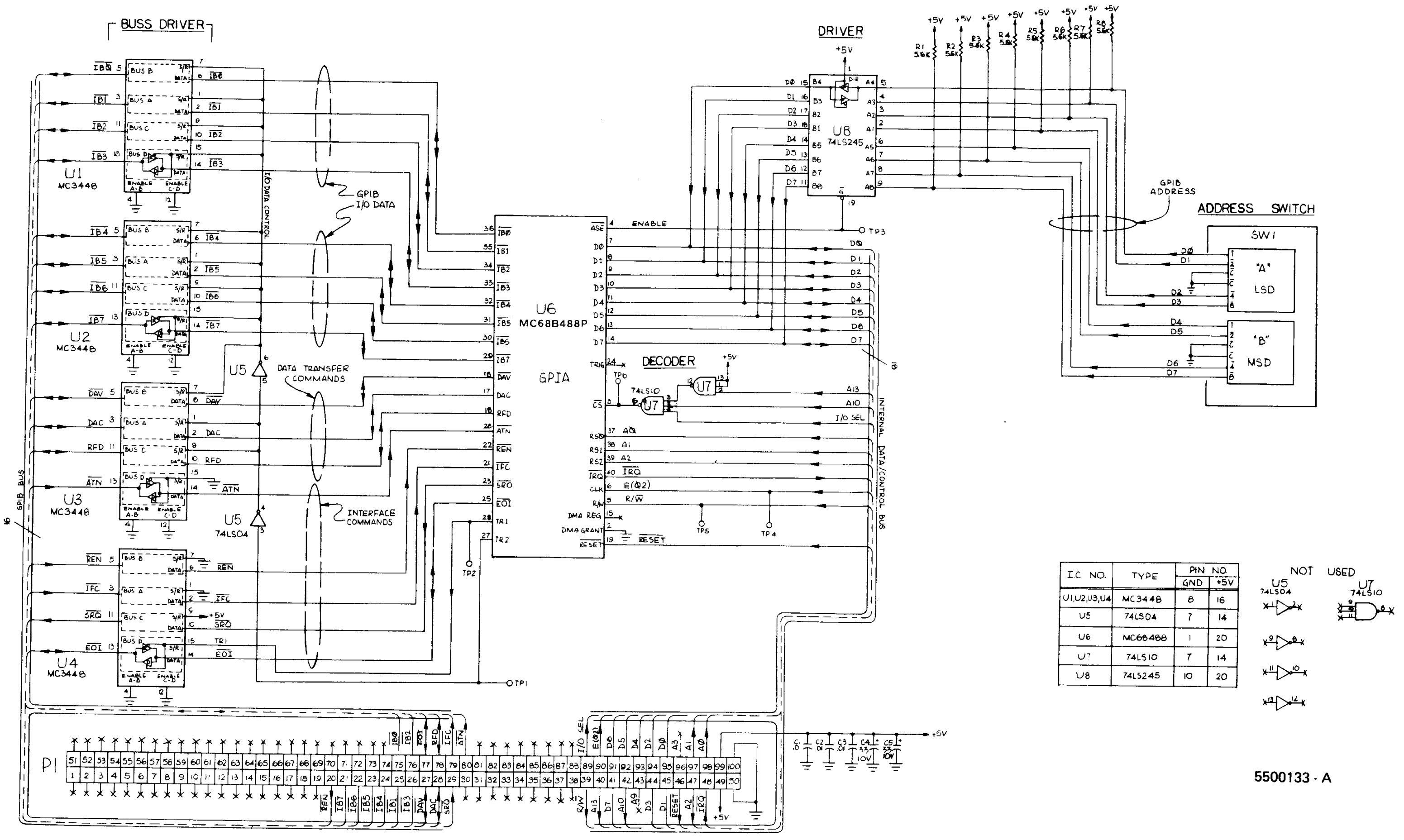


Figure 102-4. GPIB Component Locator



I.C. NO.	TYPE	PIN NO.	
		GND	+5V
U1,U2,U3,U4	MC3448	8	16
U5	74LS04	7	14
U6	MC68488	1	20
U7	74LS10	7	14
U8	74LS245	10	20

Figure 102-5. GPIB Schematic

A103
REFERENCE LOOP and DIGITAL TO ANALOG CONVERTER
(2020201)

The A103 assembly provides two major functions.

- Reference Loop (Phase Lock Loop frequency synthesizer)
- Digital to Analog Converter (DAC)
  (use with Option 01)

REFERENCE LOOP

The reference loop is a phase lock loop frequency synthesizer which tunes from 10.000 MHz to 49.995 MHz in 2.5 kHz steps. The synthesizer actually operates 1 octave above this range and is divided by 2 in U16B. The reason for dividing the output frequency of the synthesizer is to permit a 5 kHz sample rate at the phase detector instead of 2.5 kHz sample rate. This higher sample rate permits a higher loop bandwidth, which is desired for tuning speed and low phase noise on the output. A single LC VCO is used to cover this range by dividing its output frequency by 2 in U16A when the synthesizer output frequency is greater than 25 MHz.

An output of the VCO (via buffer U18 and divider U16A) is applied to the programmable frequency divider (U6 thru U11 and U13). The frequency divider is programmed by the microprocessor via P.I.A. U12, and latches U4 and U5. The output of the frequency divider is compared to the 5 kHz reference (derived from a 100 kHz clock signal from the gate generator board) in the phase detector U14.

A phase difference between the VCO and the 5 kHz reference will result in an output from the phase detector. The phase detector has two output ports; a pump up port and a pump down port. Pump down is U14 pin 2. Pump down is normally high, and goes low to reduce the VCO frequency. Pump up is U15 pin 6. Pump up is normally low, and goes high to increase the VCO frequency.

The outputs of the phase detector go to the charge pump which converts them to a single tri-state output. The charge pump output is open with no pump command, sources current with pump up, and sinks current with pump down. The output of the charge pump is connected to the input of the loop amplifier U19. The loop amplifier provides the proper gain and filtering to achieve the desired loop response. The output of the loop amplifier is the VCO tuning voltage.

The programmable frequency divider uses a two modulus (divide number) prescaler and two programmable counters. (Refer to figure 103-1.)

The prescaler is used to divide the VCO frequency down to a lower frequency which can be handled by low power Shottky TTL programmable counters. The two modulus prescaler permits prescaling without loss of resolution. At the start of the divider cycle the prescaler is set to divide by the larger modulus (11), and both programmable counters have been loaded with their respective program numbers from the P.I.A. The programmable counters each decrement 1 count for each output pulse from the prescaler.

When programmable counter B (U7) reaches the count of zero, the 10/11 control flip-flop (part of U11) changes state and causes the prescaler to divide by the lower modulus (10).

When programmable counter A reaches the count of 2 the input of the PL period flip-flop (part of U11) goes high so that, on the count of 1, the flip-flop changes state. This will cause both programmable counters to be reloaded with their respective program numbers, and the 10/11 control flip-flop to reset (prescaler in 11 state). The very next count causes the PL period flip-flop to reset, starting the programmable frequency divider cycle over again. The equation for the divide ratio of the programmable frequency divider N_d is:

$$N_d = 10N_{\text{counter A}} + N_{\text{counter B}}$$

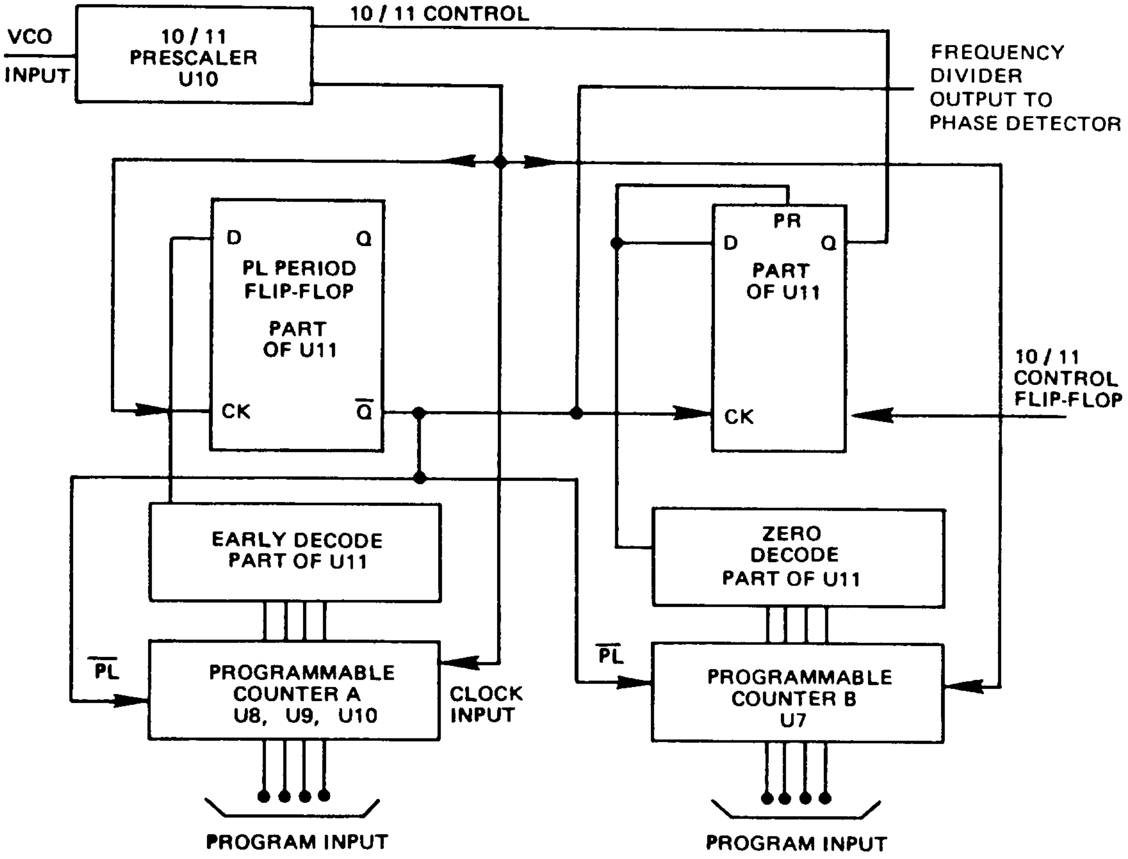


Figure 103-1. Programmable Frequency Divider Block Diagram

DIGITAL TO ANALOG CONVERTER (DAC) (Option 01)

The DAC is referenced to a 1 volt reference voltage that is generated by U1. A gain adjustment (R5) is provided to calibrate the reference to 1 volt. U3 consists of a 12 bit multiplying DAC, three individual four bit registers, and address decoding. The digital data is written to the DAC, four bits at a time, and stored in the appropriate registers. The data is then transferred simultaneously to the DAC and, in conjunction with U2, converts the digital data to an analog voltage that corresponds to the three digits selected on the front panel.

See Section 10 if DAC option 01 is installed.

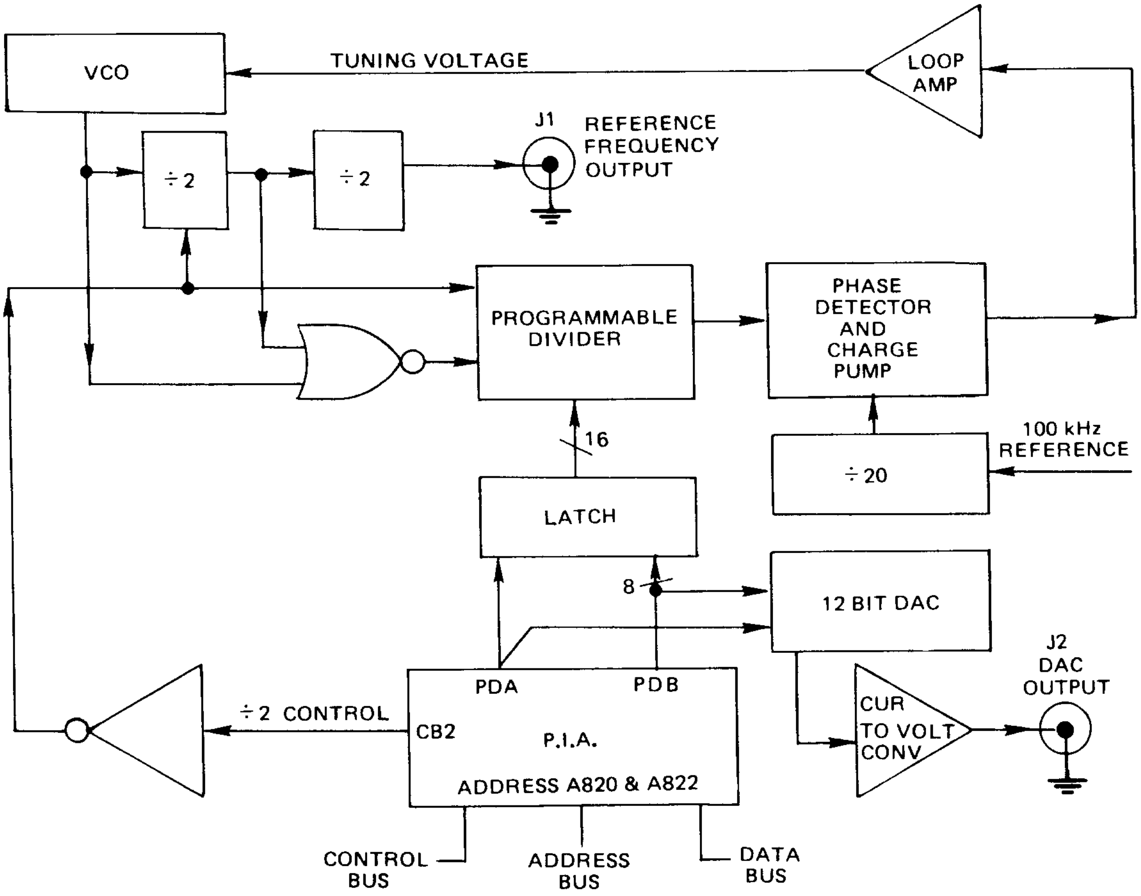


Figure 103-2. Overall Block Diagram

A103 REFERENCE LOOP

2020201-03 A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A103	REFERENCE LOOP ASSY	2020201-01	1	EIP	
C1 thru C3	Not Used				
C4	Tant, 33μF, 10%, 10V	2300015	4	TAPA 33M10	14433
C5 thru C12	Disc, .01μF, 20%, 100V	2150003	13	TG-S10	56289
C13	Tant, 10μF, 20%, 25V	2300029	4	DF106M25S	72136
C14	C13				
C15	C5				
C16	C5				
C17	C4				
C18	C4				
C19	C5				
C20	C5				
C21	Tant, 1.0μF, 10%, 35V	2300008	1	TAPA 1.0M35	14433
C22	Cer, .047 ohm, 10%, 50V	2150090	2	5020EM50RD473K	EMCAP
C23	Met Film, .47μH, 10%, 63V	2350010	1	MKT-1819-447/06	
C24	C22				
C25	C4				
C26	Disc, .001μF, 20%, 100V	2150001	2	5GA-D10	56289
C27	Tant, 100μF, 20%, 10V	2300039-00	1	TAPA 100MIO	14433
C28	C13				
C29	C5				
C30	C13				
C31	C26				
C32	Cap, Mica 47pF, 500V	2260004-00	1		
CR1	Not Used				
CR2	Dual Low Leak	2710013-00	1	ID100	
CR3	Fast Switch	2704148	3	1N4148	
CR4	Varactor	2710025	1	MV1404	72259
CR5	CR3				
CR6	CR3				
CR7	Zener, 5.1V	2705231	1	IN5231	04713
L1	Not Used				
L2	Inductor, .18μH	3510013	1	DD-0.18	72259
R1 thru R5	Not Used				
R6	Comp, 10K, 5%, 1/4W	4010103	1	RC07GF103J	81349
R7	Comp, 510, 5%, 1/4W	4010511	8	RC07GF511J	81349
R8	Comp, 4.7, 5%, 1/4W	4010479-00	2	RCO7GF479J	81349
R9	Comp, 1K, 5%, 1/4W	4010102	2	RC07GF102F	81349
R10	Comp, 4.3K, 5%, 1/4W	4010432	1	RC07GF432J	81349
R11	R7				
R12	Comp, 220K, 5%, 1/4W	4010224	1	RC07GF224J	81349
R13 thru R16	R7				
R17	Comp, 1.5M, 5%, 1/4W	4010155	1	RC07GF155J	81349
R18	R8				
R19	Comp, 1.2K, 5%, 1/4W	4010122	1	RC07GF122J	81349
R20	Comp, 750, 5%, 1/4W	4010751	1	RC07GF751J	81349
R21	R7				
R22	R7				
R23	Comp, 150, 5%, 1/4W	4020151-00	1	RC07GF151J	81349
R24	Comp, 100, 5%, 1/4W	4010101	2	RC07GF101J	81349
R25	Met Ox, 2.4K, 2%, 1/4W	4130242	1	C4/2%/2.4K	24546

A103 REFERENCE LOOP

2020201-03 A

REF DES	DESCRIPTION	EIP NO.	PER ASSY	TYP MFG NO.	TYP FSCM NO.
R26	R24				
R27	R9				
R28	Met Ox, 2K, 2%, 1/4W	4130202	1	C4/2%/2K	24546
R29	R6				
U1 thru U3	Not Used				
U4	Eight bit Latch	3034373	2	74C373	01295
U5	U4				
U6	UP/DOWN Counter	3084192	4	DM74LS192	27014
U7 thru U9	U6				
U10	2-Modulous Prescaler	3112013 -02	1	MC12013	04713
U11	Counter Control Logic	3112014	1	MC12014	04713
U12	P.I.A.	3086821	1	MC68B21P	04713
U13	Dual Flip Flop	3087474	1	DM74LS74	27014
U14	Phase Freq/Det	3014044	1	MC4044L	04713
U15	Quad, NAND, 2 INP	3087400	1	DM74LS00	27014
U16	Dual D Flip Flop	3110131	1	MC10131	04713
U17	Dual Decade Counter	3084490	1	SN74LS490	01295
U18	Quad, NOR, 2 INP	3110102	1	MC10102P	04713
U19	Op Amp, J-FET	3040071	1	TL071	01295
U20	Oscillator	3011648	1	MC1648	04713
TP1 thru TP8	.040D Pin, Gold	2620032	8	460-2970-02-03	71279

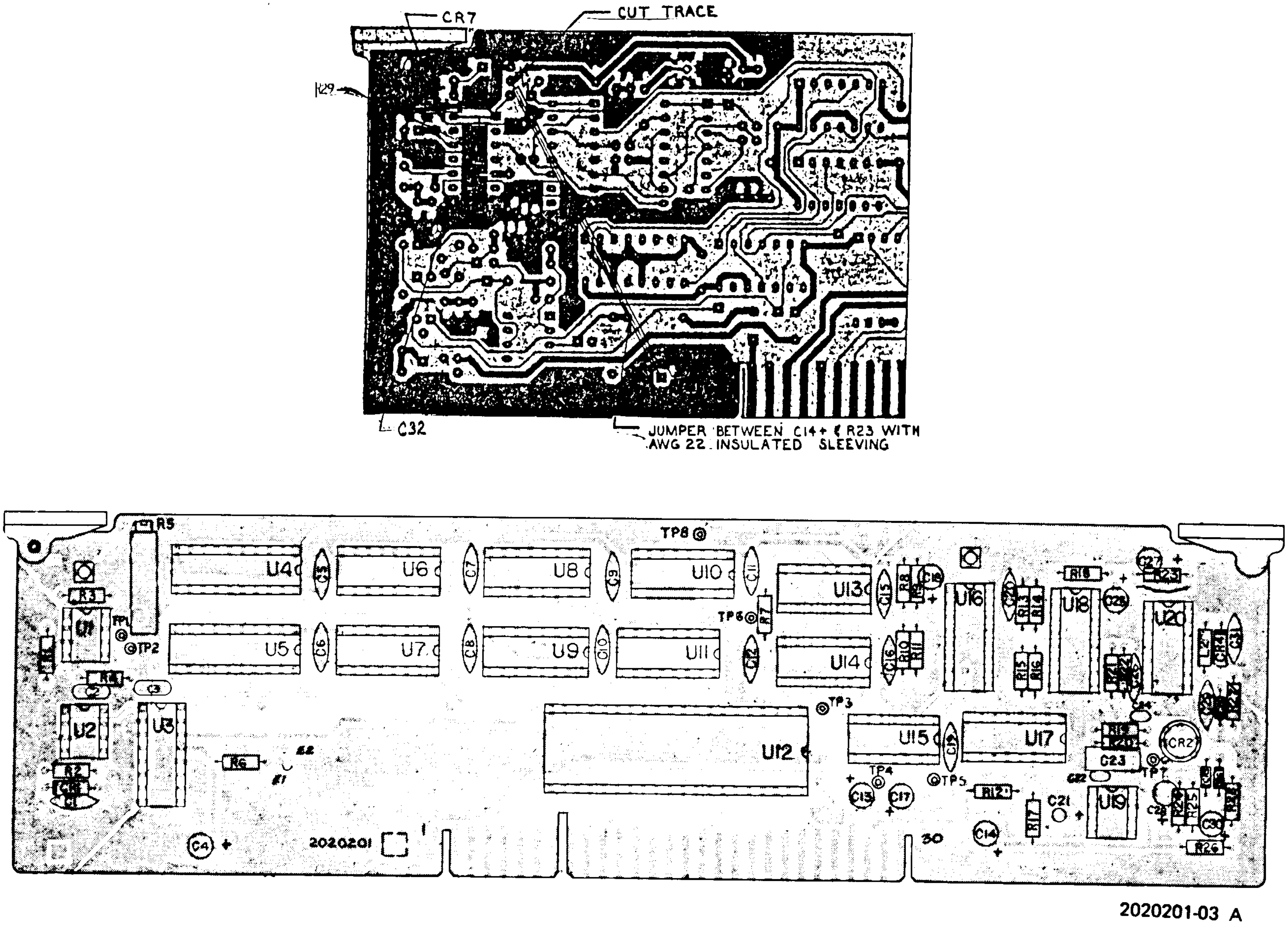
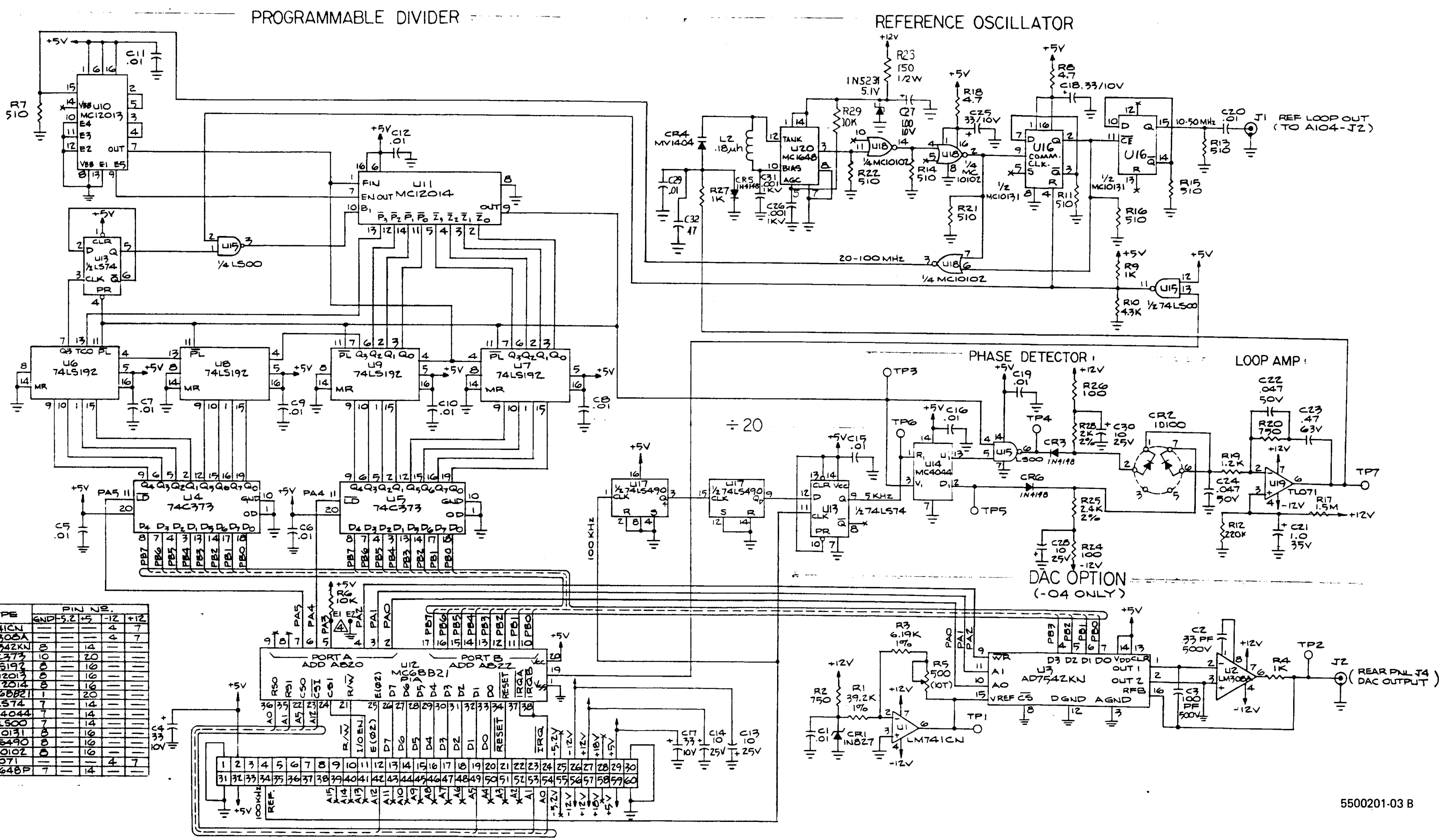


Figure 103-3. DAC / Reference Loop Component Locator

NOTE: C1 THRU C3, CR1, J2, R1 THRU R5,
AND U1 THRU U3 ARE NOT USED ON -01.



LAST REF USED	NOT USED
C32	
CR7	
J2	
L2	L1
R29	
TP8	
U20	

I.C. No.	TYPE	PIN No.				
		GND	-5.2	+5	-12	+12
U1	LM741CN	—	—	—	4	7
U2	LM308A	—	—	—	4	7
U3	AD7542KN	8	—	14	—	—
U4, U5	74C373	10	—	20	—	—
U6,7,8,9	74LS192	8	—	16	—	—
U10	MC12013	8	—	16	—	—
U11	MC12014	8	—	16	—	—
U12	MC68B21	1	—	20	—	—
U13	74LS74	7	—	14	—	—
U14	MC4044	7	—	14	—	—
U15	74LS00	7	—	14	—	—
U16	MC10131	8	—	16	—	—
U17	74LS490	8	—	16	—	—
U18	MC10102	8	—	16	—	—
U19	TL071	—	—	—	4	7
U20	MC1648P	7	—	14	—	—

NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL RESISTORS ARE ¼ W, 5%, AND ARE EXPRESSED IN OHMS.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
   ALL .01 UF CAPACITORS ARE 100V.
3. NOT USED.
4. JUMPER BETWEEN E1 & E2 ON -02 (DAC OPTION)

Figure 103-4. DAC / Reference Loop Schematic

A104
PHASE LOCK
(2020202)

The phase lock assembly contains the circuitry required to phase lock the down converted external voltage controlled oscillator (VCO) frequency from the IF to a clock derived reference frequency. The assembly also contains a lock detector to determine if the loop is within normal operating limits, and a coarse tune output provision for dual input VCO's.

The phase lock circuitry consists of the following major blocks:

- IF Buffer/Divider
- Polarity Selection
- Phase Detector
- Loop Attenuator
- Output Driver
- Shallow Search
- Coarse Tune
- Lock Detector
- Bandwidth Selection

IF BUFFER/DIVIDE BY 4

The IF input is buffered or divided by four and gated into the polarity selection circuitry. The direct buffer includes an IF range of 10 MHz to 50 MHz. The divide by four function is selected when the IF range is 50 MHz to 200 MHz.

POLARITY SELECTION

The polarity of the VCO is measured by the microprocessor and the polarity circuitry is directed by the microprocessor to input the reference frequency, or the IF frequency, to the reference port of the Phase Detector as appropriate. This digitally changes the polarity of the Phase Detector output.

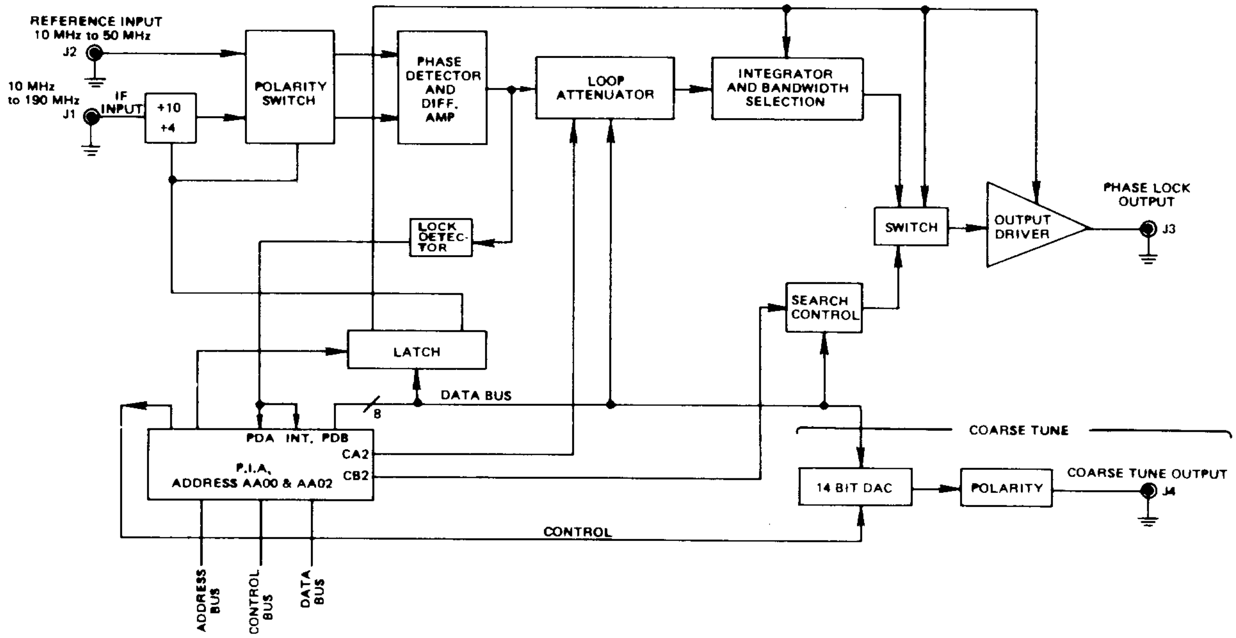


Figure 104-1. Phase Lock Assembly

PHASE DETECTOR

The phase detector circuitry compares the reference input to the IF conditioned VCO input, and outputs a voltage proportional to the phase difference between the two inputs. A digital comparator produces a differential output to a low pass filter which is amplified to a maximum output magnitude of +8V for ±π radians variation in phase difference. An IF conditioned frequency above or below the reference frequency will yield a steady state error signal of plus or minus 8V.

LOOP ATTENUATOR

The phase detector error signal is attenuated under microprocessor control by a gain DAC. At the lowest VCO gain constant the DAC will be set to the highest gain. Additionally, when the IF Divide by Four is selected, the gain of the DAC is increased by four to compensate the loop. This process produces a constant loop gain for different gain VCO's.

OUTPUT DRIVER

The output driver buffers the bandwidth selection error signal to provide either ±10V or ±75 MA depending upon the input port selected on the VCO. For high gain VCO's the stage can be changed to a gain of one sixteenth by the microprocessor providing either ±.6V or ± .5 MA.

SHALLOW SEARCH

The microprocessor disconnects the normal error signal from the Loop Attenuator and drives the Bandwidth selection circuitry with a reference voltage from a gain controlled DAC. This process is used to measure the VCO gain, which allows you to adjust the Loop Attenuator setting and polarity.

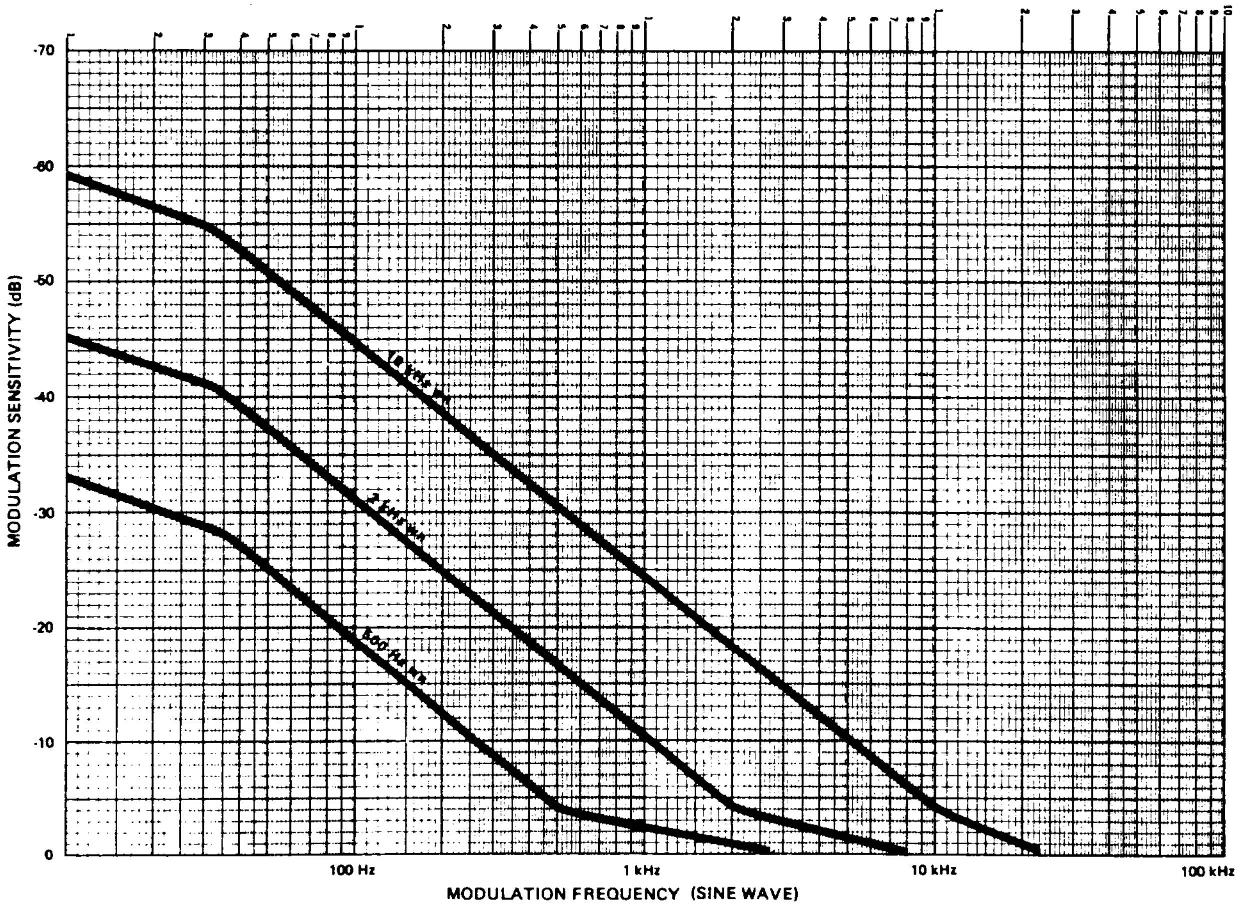


Figure 104-2. Loop Gain vs. Modulation Frequency

COARSE TUNE

The microprocessor controls a gain DAC to move the coarse tune output voltage between 0 and +10V for a two input VCO.

LOCK DETECTOR

A window detector determines if the phase detector is operating within normal range. The lock detector input time constant is short when out of lock to make initial acquisition of lock rapid and independent of selected bandwidth. The time constant after the phase detector is within range is made long to reduce nuisance tripping.

BANDWIDTH SELECTION

The gain corrected error signal is applied to an integrator that has three selectable bandwidths. The error signal can be disconnected and the output of the shallow search DAC substituted to control the output under microprocessor control. A second switch on the input to the bandwidth selection circuitry is closed during out of lock conditions to provide rapid acquisition of phase lock.

PHASE LOCK FREQUENCY CENTERING

The purpose of the 57X Phase Lock Loop is to reduce the frequency variation present on a VCO. Within the bandwidth and dynamic range of the PLL there will be an effective modulation sensitivity as shown in Figure 104-2. Figure 104-3 gives the maximum Peak to Peak deviation versus modulation frequency of an unlocked VCO that the loop will linearly handle. Above the solid line in each bandwidth, the indicated count will average some number above or below the desired frequency. Below the limit line, the count will average the desired number. The PLL in this high noise or high modulation condition acts to center the frequency.

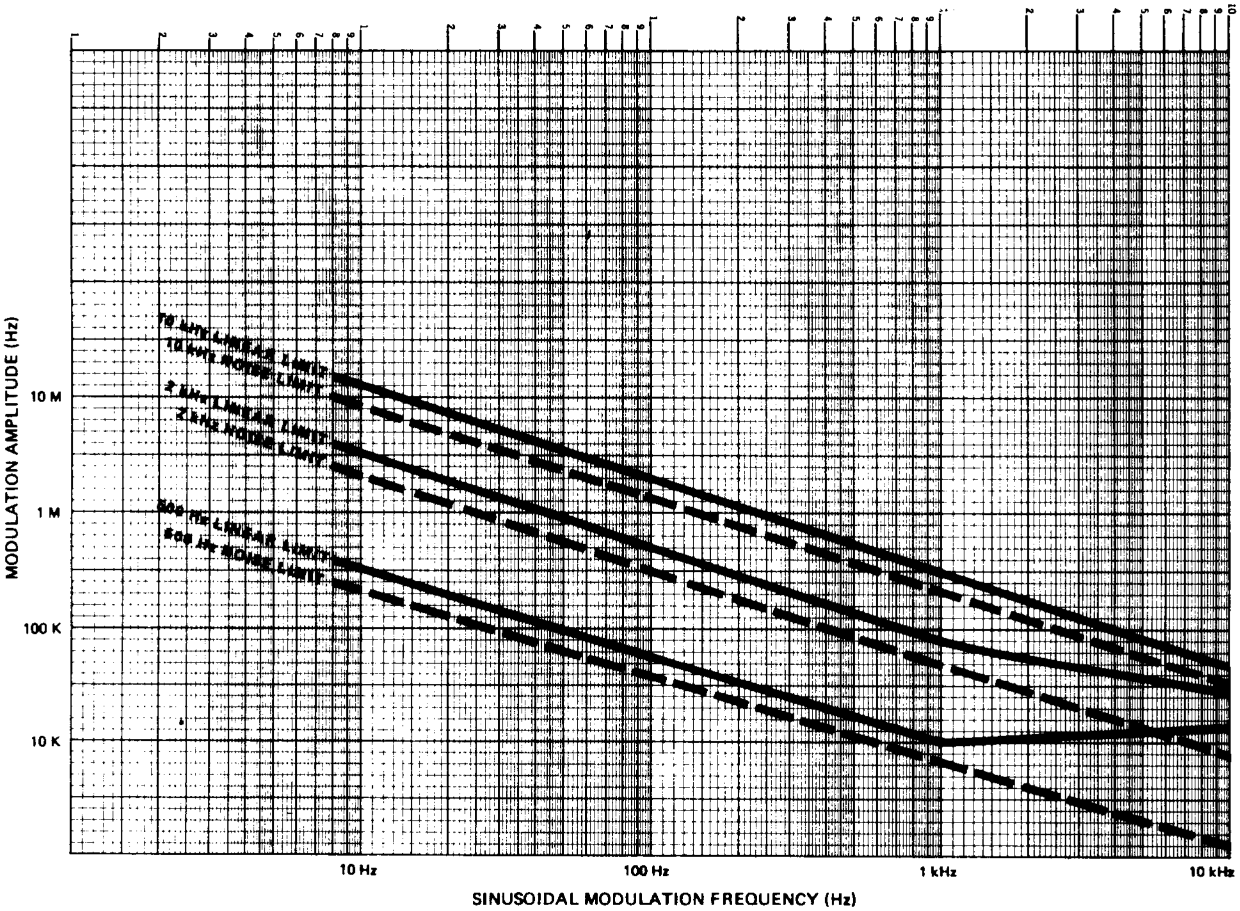


Figure 104-3. Maximum Modulation Amplitude vs. Modulation Frequency to Maintain Phase Lock

A104 PHASE LOCK

2020202-02 A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A104	PHASE LOCK ASSY	2020202-01	1	EIP	34257
C1	Disc, .01μF, 20%, 100V	2150003	29	TG-S10	56289
C2	C1				
C3	Mica, 100pF, 5%, 500V	2250002	3	DM 15101J	72136
C4 thru C13	C1				
C14	Mica, 47pF, 5%, 500V	2250017	2	DM 15470J	72136
C15	C14				
C16 thru C19	C1				
C20	Cer, 0.1μF, 20%, 16V	2150012	1	RT16-0.1MFD/16V	72136
C21	C1				
C22	Cer, 1.0μF, 20%, 50V	2150023	2	RE50-1-05MC	Murata
C23 thru C25	C1				
C26	Mica, 12pF, 5%, 500V	2250004	1	DM15CD120J	72136
C27 thru C29	C1				
C30	C22				
C31 thru C33	C1				
C34	Cer, .001μF, 20%, 1KV	2150001	1	5GA-D10	56289
C35	Mica, 20pF, 5%, 500V	2250008	1	DM15200J	72136
C36	Tant, 33μF, 10%, 20V	2300023	2	TAPA 33M20	14433
C37	C3				
C38	Not Used				
C39	C1				
C40	C3				
C41	C1				
C42	C1				
C43	Tant, 100μF, 20%, 10V	2300039	2	TAPA 100M10	14433
C44	C36				
C45	Tant, 10μF, 20%, 25V	2300029	2	DF106M25S	72136
C46	C45				
C47	C43				
C48	Cer, X7R, 0.1μF,10%,50V	2150028-00	1	RC50-104KB	51406
CR1	Fast Switch	2704148	4	IN4148	
CR2	CR1				
CR3	Hot Carrier	2710004-00	3	5082-2835	HP
CR4	CR3				
CR5	CR3				
CR6	CR1				
CR7	Power Rectifier	2704001	2	IN4001	
CR8	CR7				
CR9	CR1				
R1	Comp, 2.2K, 5%, 1/4W	4010222	1	RC07GF222J	81349
R2	Comp, 3K, 5%, 1/4W	4010302	2	RC07GF302J	81349
R3	Comp, 51 ohm, 5%, 1/4W	4010510	4	RC07GF510J	81349
R4	Comp, 1K, 5%, 1/4W	4010102	7	RC07GF102J	81349
R5	Comp, 270 ohm, 5%, 1/4W	4010271	3	RC07GF271J	81349
R6	R4				
R7	R5				
R8	R5				
R9	Comp, 510 ohm, 5%, 1/4W	4010511	3	RC07GF511J	81349
R10	R3				
R11	R9				
R12	R9				

A104 PHASE LOCK

2020202-02 A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R13	Comp, 150 ohm, 5%, 1/4W	4010151	5	RC07GF151J	81349
R14	Met Film, 511 ohm, 1%, 1/10W	4055110	4	RN55C5110F	81349
R15	R14				
R16	Not Used				
R17	Met Film, 10K, 1%, 1/10W	4051002	2	RN55C1002F	81349
R18	R14				
R19	R14				
R20	Not Used				
R21	Comp, 270K, 5%, 1/4W	4010274	1	RC07GF274J	81349
R22	R17				
R23	Comp, 10K, 5%, 1/4W	4010103	6	RC07GF103J	81349
R24	R23				
R25	Not Used				
R26	Comp, 3.3K, 5%, 1/4W	4010332	3	RC07GF332J	81349
R27	Not Used				
R28	R23				
R29	Comp, 5.1K, 5%, 1/4W	4010512	1	RC07GF512J	81349
R30	Not Used				
R31	R23				
R32	R23				
R33	Comp, 820, 5%, 1/4W	4010821	2	RC07GF821J	81349
R34	Comp, 300, 5%, 1/4W	4010301	1	RC07GF301J	81349
R35	Met Film, 5.11K, 1%, 1/10W	4055111	2	RN55C5111F	81349
R36	R35				
R37	R26				
R38	R4				
R39	Comp, 560K, 5%, 1/4W	4010564	1	RC07GF564J	81349
R40	Comp, 30K, 5%, 1/4 W	4010303	1	RC07GF303J	81349
R41	R23				
R42	Comp, 82 ohm, 5%, 1/4 W	4010820	1	RC07GF820J	81349
R43	R26				
R44	Comp, 620, 5%, 1/4W	4010621	1	RC07GF621J	81349
R45	Comp, 47, 5%, 1/4 W	4010470	1	RC07GF470J	81349
R46	Met Ox, 1.6K, 2%, 1/4W	4130162	1	CR/2%/1.6K	24546
R47	R3				
R48	R4				
R49	R4				
R50	Comp, 22K, 5%, 1/4W	4010223	1	RC07GF223J	81349
R51	R13				
R52	R13				
R53	R2				
R54	Met Ox, 20K, 2%, 1/4W	4130203	1	C4/2%/20K	24546
R55	R3				
R56	Met Ox, 24K, 2%, 1/4W	4130243	1	C4/2%/24K	24546
R57	R13				
R58	R13				
R59	Comp, 91, 5%, 1/4W	4010910	2	RC07GF910J	81349
R60	R59				
R61	Comp, 390, 5%, 1/4W	4010391	1	RC07GF391J	81349
R62	R4				
R63	R4				
R64	Comp, 1M, 5%, 1/4W	4010105	2	RC07GF105J	81349
R65	Comp, 100K, 5%, 1/4W	4010104	1	RC07GF104J	81349
R66	Comp, 47K, 5%, 1/4W	4010473	1	RC07GF473J	81349
R67	R33				
R68	Met Ox, 12K, 2%, 1/4 W	4130123	1	C4/2%/12K	24546
R69	Met Ox, 12.1K, 1%, 1/10 W	4051212	1	RN55C1212F	81349
R70	Comp, 10, 5%, 1/4 W	4010100	1	RC07GF100J	81349
R71	R64				

A104 PHASE LOCK

2020202-02 A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
RN1	Network, 9 x 510 ohm, (9R)	4170008	1	785-1-R510	08740
U1	High Speed Divide-by-4	3018600	1	SP8600B	0000C
U2	Quad MECL 10K, Translator MECL	3110124	1	MC10124L	04731
U3	Quad Line Receiver	3110115	1	MC10115	04731
U4	ECL 10K, 1 2-Inp Nors	3110102	2	MC10102P	04731
U5	U4				
U6	Phase Frequency Detector	3012040	1	MC1204OL	04731
U7	8 Bit Latch	3034373	1	74C373	27014
U8	Analog Switch	3030201	3	H13-0201-5	Harris
U9	Op. Amplifier	3040016	2	OP16GJ	PMI
U10	Lin. Op. Amplifier	3041458	1	MC1458C	04713
U11	DAC, 8 Bit, 1/2 LSB CMOS	3057524	2	AD7524JN	AD
U12	U11				
U13	P.I.A.	3086821	1	MC68B21P	04713
U14	Quad Op Amp	3044136	1	μA4136	07263
U15	U9				
U16	U8				
U17	Op Amp, Low Noise	3040714	1	μA714HC	07263
U18	U8				
U19	Low Noise Op Amp	3045534	1	NE5534N	72136
U20	12 Bit Latching DAC	3057542	1	AD7542JN	AD
U21	Flip Flop	3034013	1	MC 14013	04731
U22	Op Amp Buffer	3040308	2	LM308AN	0000X
U23	U22				
Q1	PNPN, General Purpose	4704124	1	2N4124	04713
Q2	NPN, Amplifier	4710033	1	MPSA-06	04713
Q3	PNP, Amplifier	4710036	1	MPSA56	04713
TP1 thru TP10	.040D Pin, Gold	2620032	10	460-2970-02-03	71279

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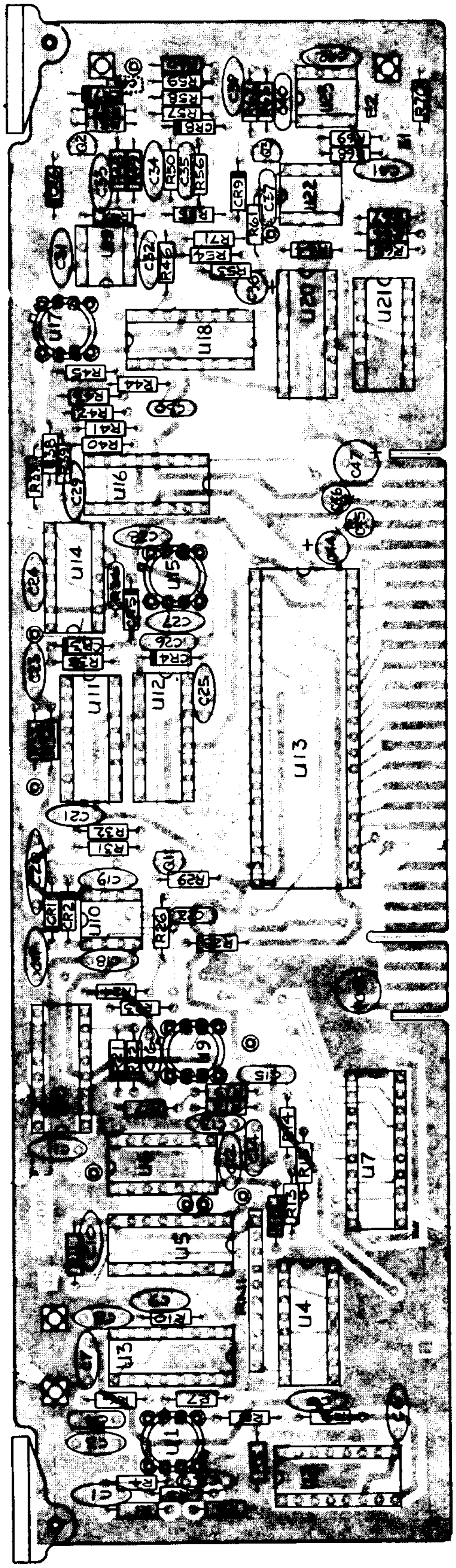
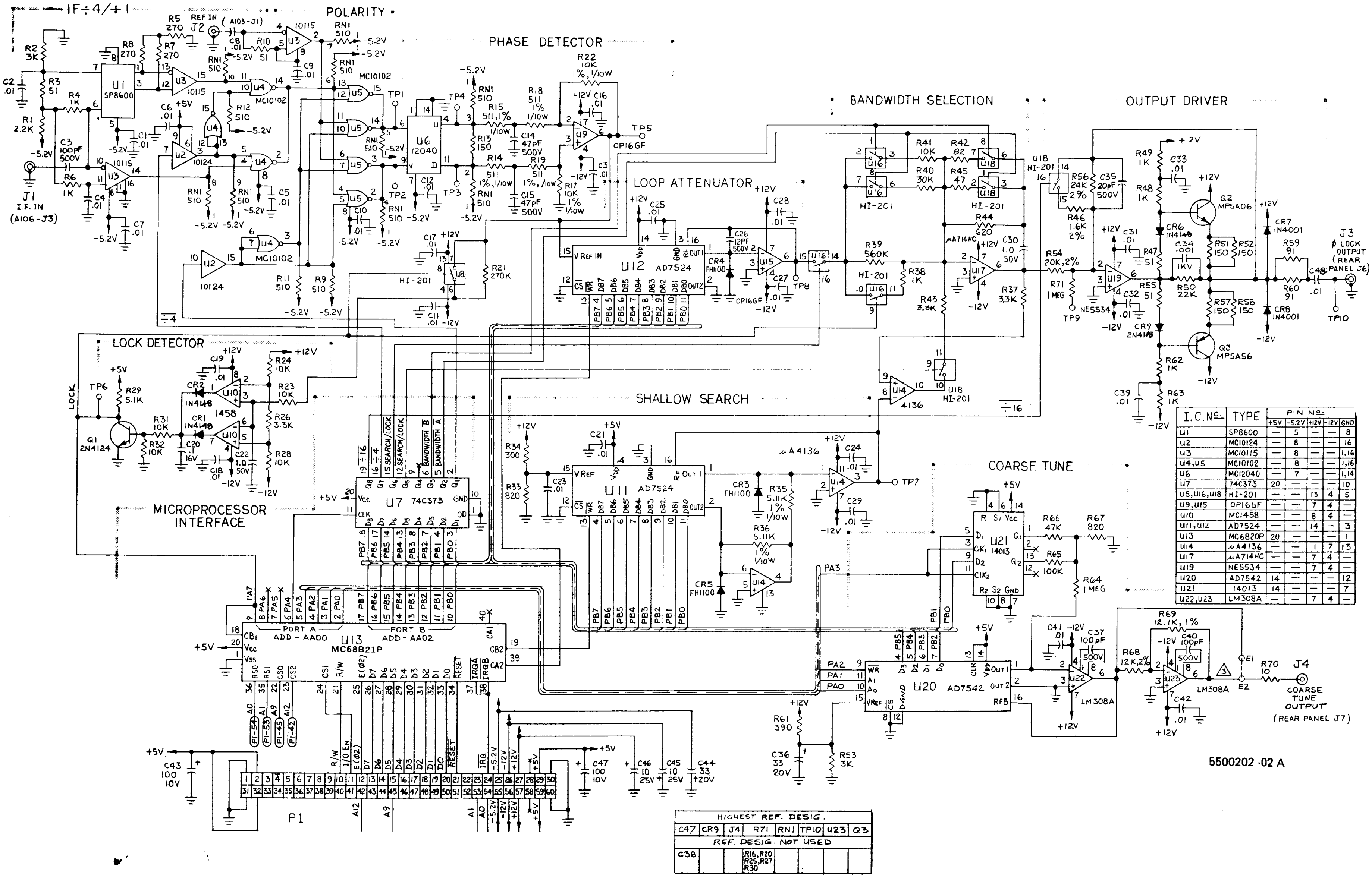


2020202-02 A

Figure 104-4. Phase Lock Component Locator



I.C. No.	TYPE	PIN No.				
		+5V	-5.2V	+12V	-12V	GND
U1	SP8600	—	5	—	—	8
U2	MC10124	—	8	—	—	16
U3	MC10115	—	8	—	—	1,16
U4,U5	MC10102	—	8	—	—	1,16
U6	MC12040	—	7	—	—	1,14
U7	74C373	20	—	—	—	10
U8,U16,U18	HI-201	—	—	13	4	5
U9,U15	OP16GF	—	—	7	4	—
U10	MC1458	—	—	8	4	—
U11,U12	AD7524	—	—	14	—	3
U13	MC6820P	20	—	—	—	1
U14	μA4136	—	—	11	7	13
U17	μA714HC	—	—	7	4	—
U19	NE5534	—	—	7	4	—
U20	AD7542	14	—	—	—	12
U21	14013	14	—	—	—	7
U22,U23	LM308A	—	—	7	4	—

HIGHEST REF. DESIG.							
C47	CR9	J4	R71	RN1	TP10	U23	Q3
REF. DESIG. NOT USED							
C38			R16, R20 R25, R27 R30				

5500202-02 A

Figure 104-5. Phase Lock Schematic

A105

MICROPROCESSOR

(20201215)

The Microprocessor board contains the microprocessor, the control logic, and the firmware for controlling the operation of the counter. The board can be divided into five functional blocks.

1. Microprocessor
2. Power-up Reset Circuit
3. Address Decoder
4. RAM and Program Memory
5. Control Logic Buffers

MICROPROCESSOR

The counter uses a Motorola 68B09 microprocessor. The clock generation circuitry for the digital system is contained within the 68B09. The only external components required for clock generation are two 24-pF capacitor and an AT-cut 8-MHz crystal.

The NMI, FIRO, and DMA functions of the 68B09 are not used. Their corresponding control lines are always disabled. The processor state indicators (BS, BA) are also not used by the counter. The HALT and the MRDY controls are connected to the Interconnect board through the edge connector.

POWER-UP RESET CIRCUIT

The Power-up Reset circuit provides a 100-ms reset signal to the entire digital system after the counter is turned on. The reset signal remains true as long as the +5-volt power supply stays below +4 volts.

When the counter is turned on, the voltage across C5 is 0 volts. The output of the comparator U1 is at logic low. The capacitor C5 slowly charges up through R2. The output of the comparator remains low as long as the voltage across C5 is lower than the voltage on pin 3 of the comparator. When the voltage across C5 becomes higher than that on pin 3, the output of the comparator becomes true, removing the reset signal. R3 is provided for hysteresis purposes. When power is removed, C5 will discharge quickly through CR1.

ADDRESS DECODER

The address decoding is performed by a 4-to-16 line decoder. The 64K-byte address space is divided into sixteen 4K-byte blocks, one of which is always enabled.

The enable signals for the memory blocks become true no later than 51 ns after Q. They stay true until a maximum of 40 ns after E has become false. The 4-to-16-line decoder has open collector outputs. This enables the addressed memory block to be enlarged by wire-ORing two or more outputs together.

The memory map for the counter is as follows:

Volatile RAM Memory	0000 - 07FF
Non-Volatile RAM Memory	0800 - 0FFF
I/O	1000 - 2FFF
Signature Analysis	3000 - 3FFF
Program Memory	4000 - FFEF
Reserved (6809)	FFF0 - FFF1
	FFF2 - FFF3
	FFF4 - FFF5
	FFF6 - FFF7
IRQ	FFF8 - FFF9
	FFFA - FFFB
	FFFC - FFFD
RESET	FFFE - FFFF

RAM AND PROGRAM MEMORY

RAM

A 2K-byte-wide volatile RAM is provided for the normal operation of the counter. To prevent data from being erroneously written into the RAM, the chip enable signal is active only when the E clock and the RAM memory block enable signal from the address decoder are both active and when the A11 address line is at logic 1.

PROM

A block of 48K bytes of memory are assigned for system program. The Microprocessor board contains three 28-pin sockets for PROMs. Each of the sockets is wired to accept a 16K-byte PROM.

CONTROL LOGIC AND BUFFERS

The digital system of the counter contains three buses: the data bus, the address bus, and the control bus.

DATA BUS

The data bus originates from the microprocessor. For signature analysis, the data bus can be disconnected from the rest of the system at the microprocessor by removing jumper header E1. The data bus on the microprocessor board is buffered from the rest of the digital system. The data bus buffer is enabled only when the address space assigned to I/O is addressed. The direction of the data bus buffer is determined by the state of the R/W control line.

CONTROL BUS

The control bus contains eight control lines. Five of the control lines originate from the Microprocessor board. The other three control lines originate from the rest of the digital system.

R/W, E, and Q originate from the microprocessor. Reset is supplied by the power-up reset circuit. The I/O SEL control line is true when A15 and A14 are at logic 0 and either A13 or A12 or both are at logic 1 levels. The IRQ control line is the wired-OR of the interrupt request lines. MRDY is the wired-OR of the memory ready control lines. The MRDY and HALT control lines are provided for future expansion.

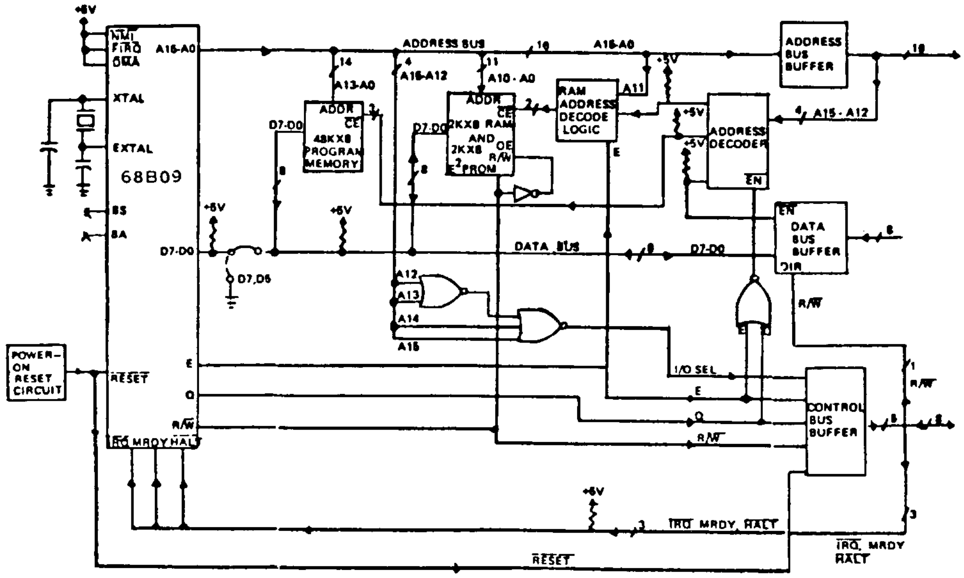


Figure 105-1. Functional Block Diagram, PMicroprocessor

A105 MICROPROCESSOR

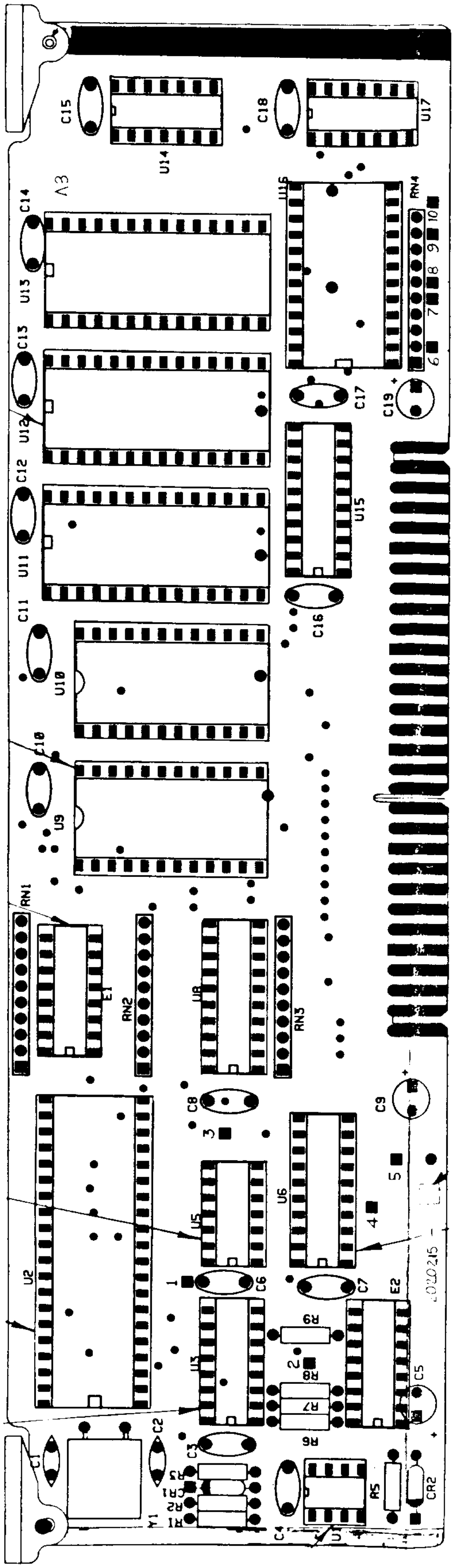
2020215-02 A

REF DES	DESCRIPTION	EIP NO.	PER ASSY	TYP MFG NO.	TYP FSCM NO.
C1	Mica, 24pF, 5%, 500V	2260018-00	2	CD10ED240J03	14655
C2	C1				
C3	Disc, 0.01µF, 20%, 100V	2150003-00	14	TG - S10	56289
C4	C3				
C5	Tant, 3.9µF, 10%, 15V	2300027-00	1	196D395X9015HA1	56289
C6	C3				
C7	C3				
C8	C3				
C9	Tant, 33µF, 10V	2300015-00	2	TAPA33M10	14433
C10	C3				
C11	C3				
C12	C3				
C13	C3				
C14	C3				
C15	C3				
C16	C3				
C17	C3				
C18	C3				
C19	C9				
CR1	H/C	2710016-00	1	5082-2835	28480
CR2	ZNR, 3.9V	2705228-01	1	IN5228	04713
R1	Met Ox, IM, 5%, 1/4W	4010105-00	1	RC07GF105J	81349
R2	Met Ox, 22K, 5%, 1/4W	4010223-00	1	RC07GF223J	81349
R3	Met Ox, 300K, 5%, 1/4W	4010304-00	1	RC07GF304J	81349
R4	Not used				
R5	Met Ox, 240, 5%, 1/4W	4010241-00	1	RC07GF241J	81349
R6	Met Ox, 4.7K, 5%, 1/4W	4010472-00	4	RC07GF472J	81349
R7	R6				
R8	R6				
R9	R6				
RN1	Res Ntwrk, 9 x 10k, 2%, 2W	4170003-00	3	782-1-R10K	80740
RN2	RN1				
RN3	RN1				
RN4	Res Ntwrk, 9x4.7k, 2%, 1.25W	4170014-00	1	4310R-101-472	32997
TP1 Thru TP10	Pin, T.P. Swage	2620032-00	10	460-2970-02-03	71279
U1	Int: Volt Comparator	3050311-00	1	MLM311P1	27014
U2	Microprocessor	3050025-00	1	MC68B09	04713
U3	Dvr Hex Bus/Buffer	3084365-00	1	SN74LS365N	01295
U4	Not used				
U5	3 Inp NOR Gate	3087427-00	1	DM74LS27	27014
U6	Dvr Line/Oct Buff Invg	3084244-00	2	SN74LS244N	01295
U7	Not used				
U8	Xcvr Octal Bus	3084245-00	1	SN74LS245N	01295

A105 MICROPROCESSOR

2020215-02 A

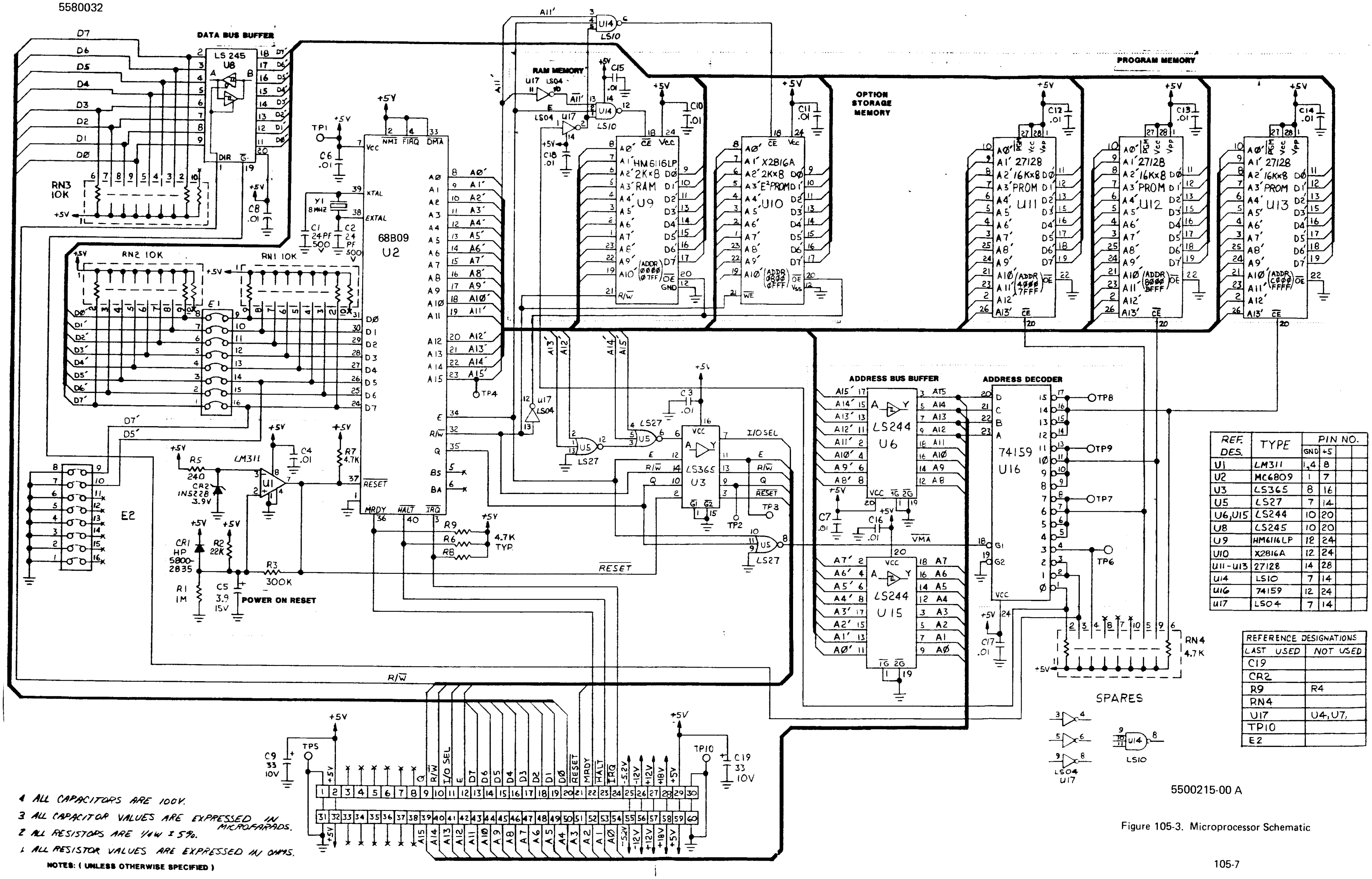
REF DES	DESCRIPTION	EIP NO.	PER ASSY	TYP MFG NO.	TYP FSCM NO.
U9	2K x 8 CMOS RAM	3056116-00	1	HM6116LP-4	62786
U10	2K x 8E PROM	6420000-00	1	X2816A	60395
U11	PROM Set: 16K x 8	2060006-00	1		27128
U12	U11				
U13	U11				
U14	3 INP NAND Gate	3087410-00	1	DM74LS10	27014
U15	U6				
U16	4-16 Decoder	3074159-00	1	SN74159N	01295
U17	Hex Inverter	3087404-00	1	DM74LS04	27014
E1	Prog, Header, 16 Pin DIP	5000205-00	1	16-675-191T	51167
Y1	Xtal, 8.00 MHz	2030100-00	1	MP-1	ATRON



2020215-01 A

Figure 85-2. Component Locator, Microprocessor

5580032



4 ALL CAPACITORS ARE 100V.

3 ALL CAPACITOR VALUES ARE EXPRESSED IN MICROFARADS.

2 ALL RESISTORS ARE 1/4w ± 5%.

1 ALL RESISTOR VALUES ARE EXPRESSED IN OHMS.

NOTES: (UNLESS OTHERWISE SPECIFIED)

REF. DES.	TYPE	PIN NO.			
		GND	+5		
U1	LM311	1,4	8		
U2	MC6809	1	7		
U3	LS365	8	16		
U5	LS27	7	14		
U6,U15	LS244	10	20		
U8	LS245	10	20		
U9	HM6116LP	12	24		
U10	X2816A	12	24		
U11-U13	27128	14	28		
U14	LS10	7	14		
U16	74159	12	24		
U17	LS04	7	14		

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C19	
CR2	
R9	R4
RN4	
U17	U4, U7,
TP10	
E2	

5500215-00 A

Figure 105-3. Microprocessor Schematic

A106
COUNT CHAIN
(2020136)

The Count Chain assembly receives IF signals from the Band 3 IF Amplifier (A201B) and the Band 2 converter A109). It also receives a gate signal and a 100 kHz reference signal from the Gate Generator (A107). The Count Chain assembly selects the appropriate IF signal, gates it, and counts it to produce a BCD output that represents the input frequency. It also produces IF output signals at J3 and J4.

The A106 board receives two IF input signals on J1 and J2. The appropriate input is selected by enabling one of two differential amplifiers (U1A or U1B). Enabling of the appropriate amplifier is achieved by turning on a transistor switch (Q11 or Q12). The appropriate transistor is turned on by the output of an open collector inverter (U7C or U7A) driven by a TTL signal from the PIA (U10).

The output of the input selector differentially drives a squaring circuit. The squaring circuit consists of a differentially driven current mirror (Q1) driving a tunnel diode (CR4). The voltage across the tunnel diode changes abruptly between two states (approximately 0.2V and 0.5V). The signal across the diode drives the pulse forming circuit. This circuit begins with a high speed differential amplifier (Q2 and Q3). The output of this amplifier drives Q4 which is a current switch. The square wave current, from Q4's collector, drives an inductor (L1). The voltage across the inductor is a series of pulses; a positive pulse when Q4 turns on and a negative pulse when Q4 turns off. Diode CR5 tends to remove the negative pulses and increases the damping to improve the amplitude of the positive pulses. The positive pulses from the generator drive a pulse inverter (Q6). The pulse inverter is a high-speed zero bias amplifier that is biased at cut off by diode CR6.

The output of the pulse inverter (Q6) drives the input to the first decade counter (U2). The bias for the U2 input is established by a tracking bias supply (U3, Q7). The voltage at TP2 is equal to the voltage on U2 pin 1, plus a fixed DC offset selected by R47. The BCD outputs from U2 are slew-rate limited, and can only be seen on an oscilloscope after the counting ends and comes to rest. The carry output U2 pin 9 is an ECL level signal, and is always visible.

The ECL output of U2 drives an ECL to TTL converter (Q8, Q9 and Q10). This converter is a differential amplifier with a cascade output buffer (Q8). The response of Q8 is improved by inductive peaking provided by L2. The output of Q8 drives a decade counter (U4) which in turn drives a third decade counter (U5). The BCD outputs of U4 and U5 are connected to a 6 decade counter (U6) which derives its clock information directly from the BCD outputs of U5. When counting is finished, 8 decades of BCD data are read by the microprocessor (through the PIA U10) from U6 by a time multiplex process. The multiplexer (set to the first digit by the end of the previous reset clock) loads the multiplex latches with the $\overline{\text{Latch Load}}$ clock, and steps to the remaining 7 digits with 7 pulses on the $\overline{\text{Scan Clock}}$ line. The first decade of BCD data from U2 is read directly from the PIA.

A single reset line is used to reset all count stages to zero before the next count cycle begins.

A real-time clock (U8, U9) is also on the count chain assembly. This circuit takes the 100kHz reference signal that is coming from the Counter Interconnect Assembly (A100) and divides it by 10,000 to give a 10Hz (100ms) clock. The output from this clock is fed to the PIA to allow the microprocessor to gather time information at a 10Hz rate for timing functions within the program.

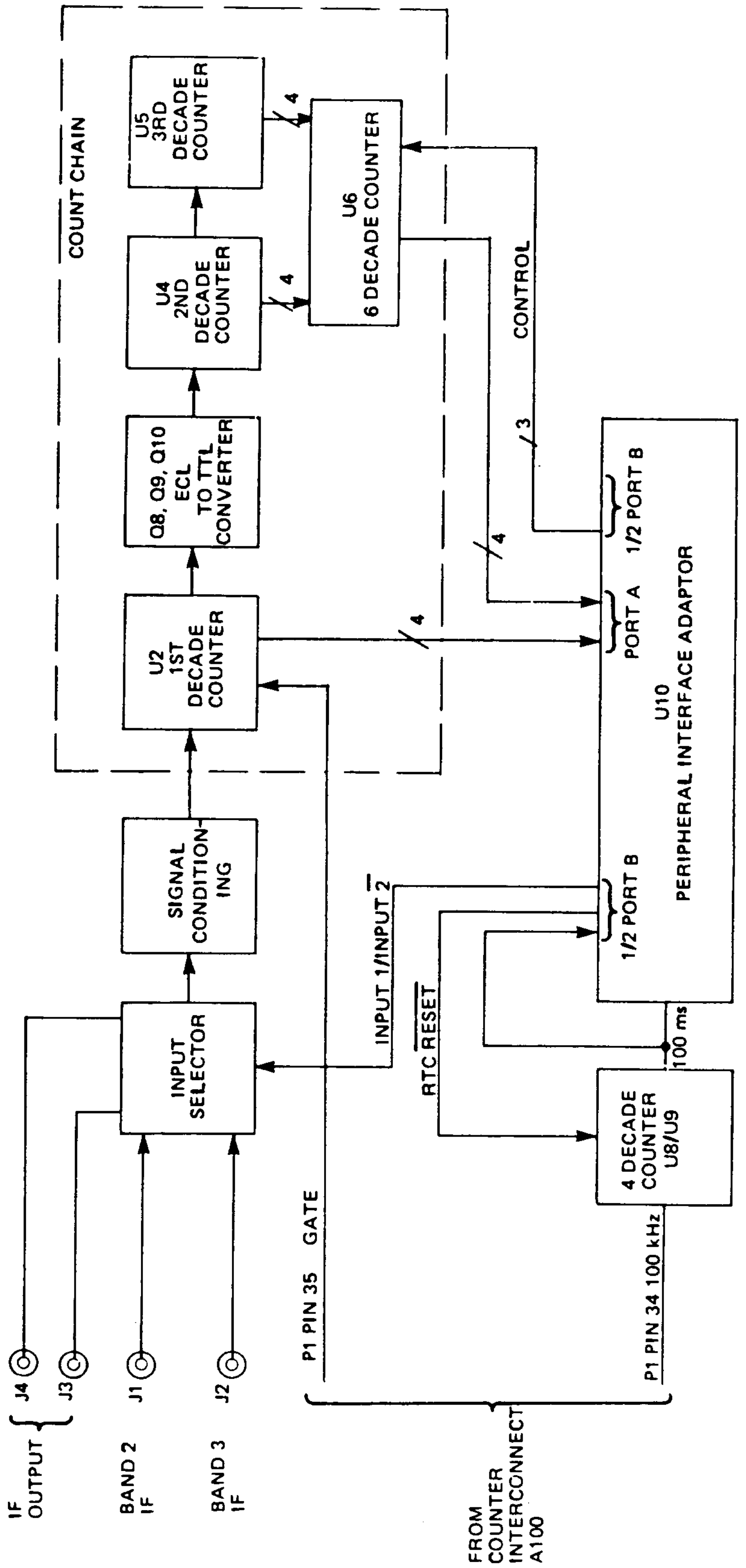


Figure 106-1. Count Chain Functional Diagram

A106 COUNT CHAIN ASSY

2020136-03C

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A106	Count Chain Assy	2020136	1	EIP	34257
C1	Tant, 33μF, 20%, 10V	2300015	5	TAG 20 - 33/10 - 50	14433
C2	Cer., .01μF, 20%, 100V	2150003	17	TG - S10	56289
C3	C2				
C4	C1				
C5	Mica, 10pF, 5%, 500V	2260012	1	DM15CD100J03	72136
C6	Tant, 10μF, 20%, 25V	2300029	4	DF106M25S	72136
C7	C2				
C8	C2				
C9	Cer., .001μF, 20%, 1KV	2150001	3	5GA - D10	56289
C10	C2				
C11	Not Used				
C12	C9				
C13	C2				
C14	C6				
C15	C6				
C16	C2				
C17	C9				
C18	Not Used				
C19	Not Used				
C20	C1				
C21	C2				
C22	C1				
C23	Not Used				
C24 thru C28	C2				
C29	C1				
C30 thru C33	C2				
C34	C6				
CR1	General Purpose	2704148	3	IN4148	07263
CR2	Zener, 6.2V	2705234	1	IN5234	04713
CR3	CR1				
CR4	Tunnel, Switching	2710033	1	G00010C	20754
CR5	Hot Carrier	2710004-00	1	5082 - 2835	28480
CR6	CR1				
CR7	Not Used				
L1	Part of Board				
L2	Inductor, 1μH	3510003	1	DD 1.0	72259
Q1	PNP, RF	4704959	1	2N4959	04713
Q2	NPN, MICROWAVE	4710032	3	NEO2137	33279
Q3	Q2				
Q4	PNP, RF	4710010	1	MPS - H81	04713
Q5	PNP, RF, Graded 2N5179	4710013	1	4705179	34257
Q6	NPN, RF	4710026	1	NE73432B	0000S
Q7	Q2				
Q8	NPN, RF	4705179	3	2N5179	04713
Q9	Q8				
Q10	Q8				
Q11	PNP, General Purpose	4704126	2	2N4126	04713
Q12	Q11				

A106 COUNT CHAIN ASSY, continued

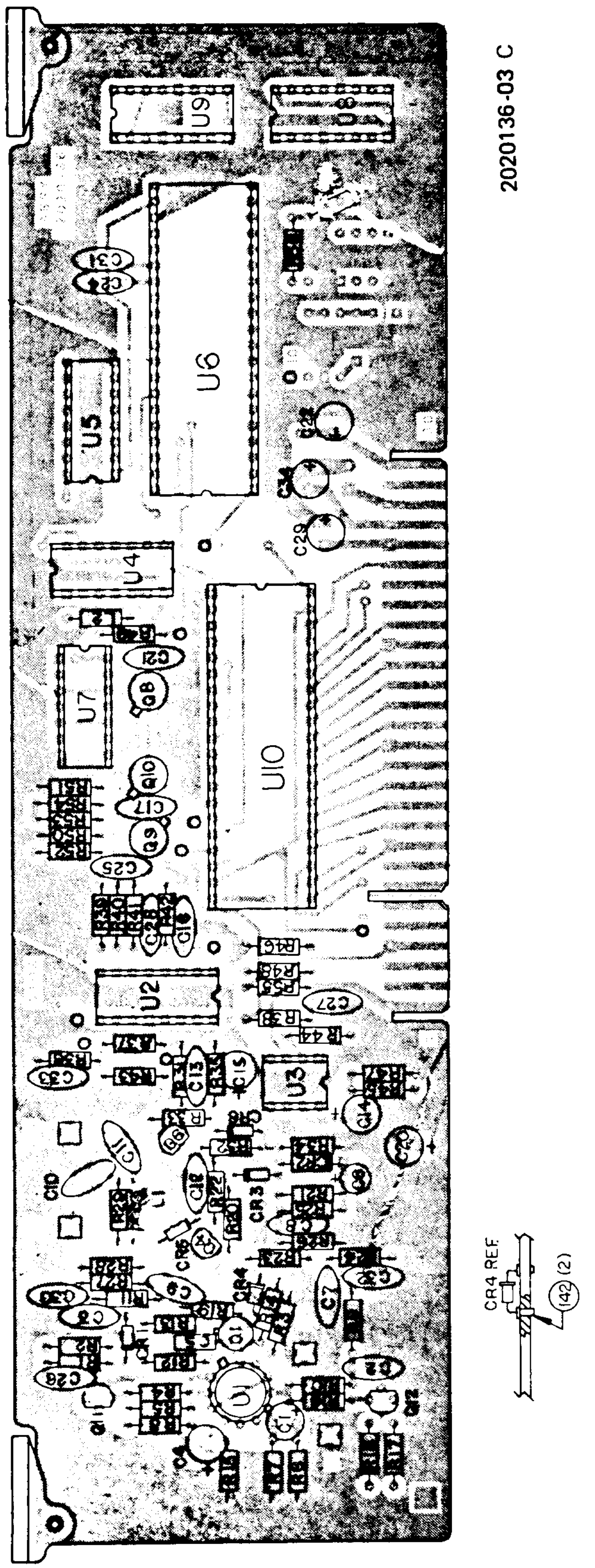
2020136-03 C

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R1	Comp., 1.5K, 5%, 1/4 W	4010152	2	RC07GF152J	81349
R2	Comp., 6.2K, 5%, 1/4 W	4010622	2	RC07GF622J	81349
R3	Comp., 51 ohm, 2%, 1/4 W	4130510	2	C4/2%/51	24546
R4	Comp., 5.1K, 5%, 1/4 W	4010512	2	RC07GF512J	81349
R5	Comp., 2.7K, 5%, 1/4 W	4010272	2	RC07GF272J	81349
R6	Comp., 51 ohm, 5%, 1/4 W	4010510	1	RC07GF510J	81349
R7	Met Ox, 2K, 2%, 1/4 W	4130202	3	C4/2%/2K	24546
R8	Comp., 510 ohm, 5%, 1/4 W	4010511	1	RC07GF511J	81349
R9	Comp., 5.6 ohm, 5%, 1/4 W	4010569	5	RC07GF5R6J	81349
R10	R5				
R11	R9				
R12	Met Ox, 68 ohm, 2%, 1/4 W	4130680	1	C4/2%/68	24546
R13	Met Ox, 43 ohm, 2%, 1/4 W	4130430	1	C4/2%/43	24546
R14	Met Ox, 3.9K, 2%, 1/4 W	4130392	1	C4/2%/3.9K	24546
R15	R7				
R16	R4				
R17	R1				
R18	R2				
R19	Comp., 100 ohm, 5%, 1/4 W	4010101	1	RC07GF101J	81349
R20	Met Ox, 56 ohm, 2%, 1/4 W	4130560	2	C4/2%/56	24546
R21	R9				
R22	R20				
R23	Comp., 200 ohm, 2%, 1/4 W	4130201	1	RL07S201G	24546
R24	R9				
R25	Met Ox, S.A.T. (2K, 2% Nom)	4130999	1	C4/2%/XX	24546
R26	Met Ox, 39 ohm, 2%, 1/4 W	4130390	2	C4/2%/39	24546
R27	R23				
R28	Met Ox, 270 ohm, 2%, 1/4 W	4130271	1	C4/2%/270	24546
R29	R3				
R30	Not Used				
R31	Comp, 10 ohm, 5%, 1/4 W	4010100	1	RC07GF100J	81349
R32	Met Ox, 47 ohm, 2%, 1/4 W	4130470	1	C4/2%/47	24546
R33	Met Ox, 20 ohm, 2%, 1/4 W	4130200	1	C4/2%/20	24546
R34	Met Ox, 510 ohm, 2%, 1/4 W	4130511	1	C4/2%/510	24546
R35	R9				
R36	Met Ox, 1K, 2%, 1/4 W	4130102	3	C4/2%/1K	24546
R37	R26				
R38	Comp., 390 ohm, 5%, 1/4 W	4010391	1	RC07GF391J	81349
R39 thru R42	Comp, 10 K, 5%, 1/4 W	4010103	4	RC07GF103J	81349
R43	Met Ox, 20 K, 2%, 1/4 W	4130203	4	C4/2%/20K	24546
R44	R43				
R45	R36				
R46	R43				
R47	Met Ox, 18 ohm, 2%, 1/4 W (NOM) SAT	4130999	1	C4/2%/18	24546
R48	R43				
R49	Met Ox, 240 ohm, 2%, 1/4 W	4130241	1	C4/2%/240	24546
R50	R23				
R51	R23				
R52	R36				
R53	Met Ox, 430 ohm, 2%, 1/4W	4130431	1	C4/2%/430	24546

A106 COUNT CHAIN ASSY, continued

2020136-03C

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R54	R7				
R55	Comp., 1.8K, 5%, 1/4 W	4010182	1	RC07GF182J	81349
R56	Comp., 4.7K 5%, 1/4 W	4010472	1	RC07GF472J	81349
TP1 thru TP10	Conn., Pin, .040D	2620032	10	460-2970-0203	71279
U1	Dual/Diff Ampl	3043049	1	CA3049T	07263
U2	UHF, BCD, Decade Counter	3010637	1	SP8637B	0000C
U3	Op Amplifier	3040741	1	LM741CN	0000X
U4	PST Decade Counter	3084196	1	SN74LS196N	01295
U5	4 Bit Decade Counter	3084160	1	SN74LS160N	01295
U6	6 Dec. Ctr/8 Dec. Latch	3057031	1	LS74031	01295
U7	Hex Inverter	3087404	1	DM74LS04N	0000X
U8	Decade Counter	3084490	2	74LS490N	01295
U9	U8				
U10	Periph. Interface Adapter	3086821	1	MC68B21P	04713



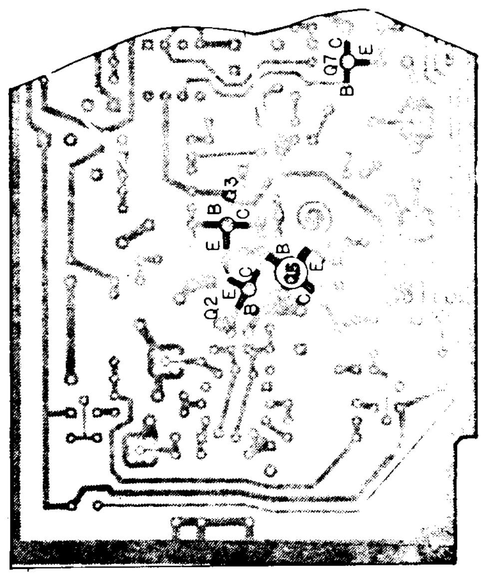
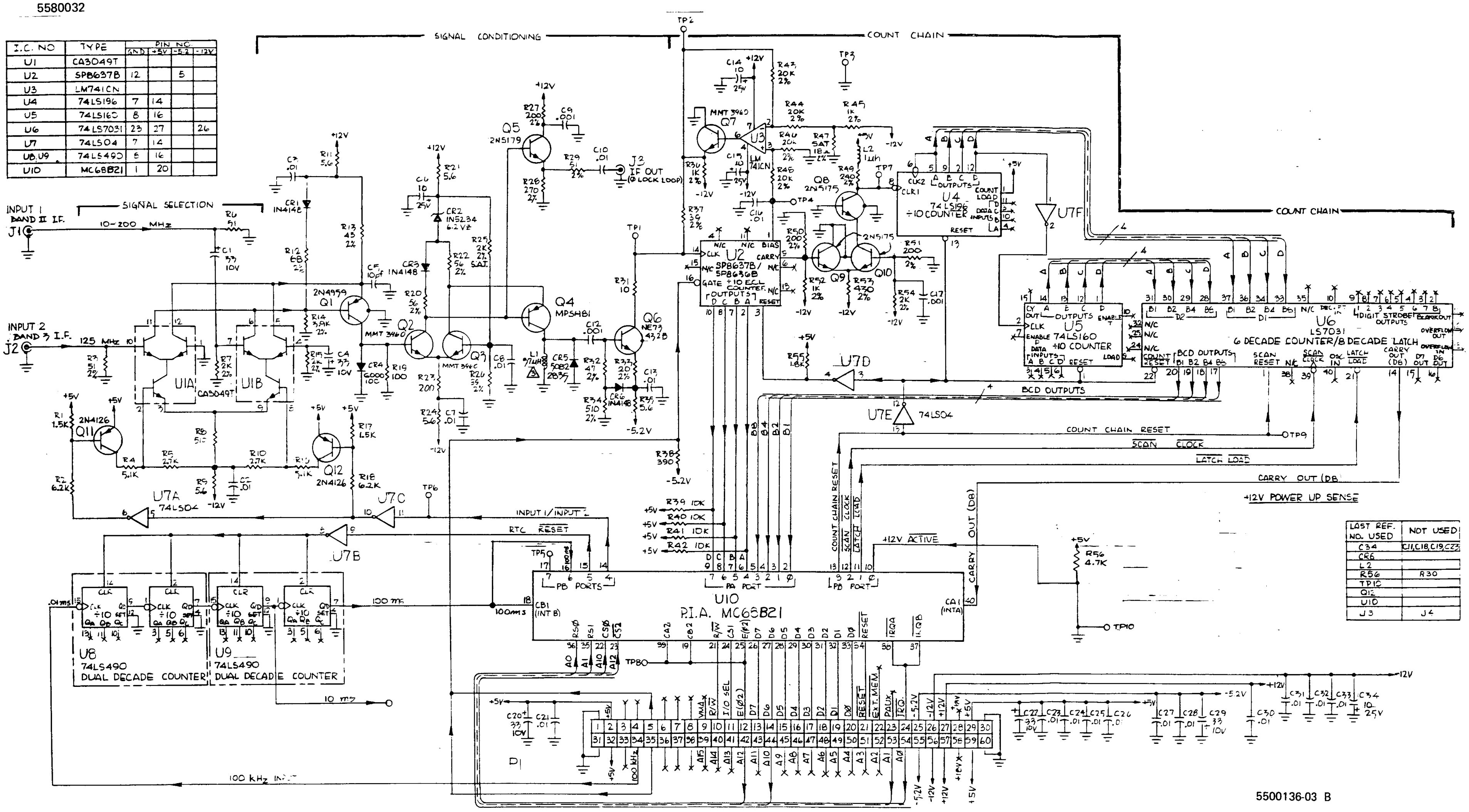


Figure 106-2. Count Chain Component Locator

5580032

I.C. NO	TYPE	PIN NO.			
		GND	+5V	-5.2	-12V
U1	CA3049T				
U2	SPB637B	12		5	
U3	LM741CN				
U4	74LS196	7	14		
U5	74LS160	8	16		
U6	74LS7031	23	27		26
U7	74LS04	7	14		
U8,U9	74LS490	5	16		
U10	MC68B21	1	20		



LAST REF. NO. USED	NOT USED
C34	C11,C18,C19,C23
CR6	
L2	
R56	R30
TP10	
Q12	
U10	
J3	J4

5500136-03 B

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE ¼W, 5%. RESISTANCE IS EXPRESSED IN OHMS.
2 ALL CAPACITOR VALUES ARE EXPRESSED IN MICROFARADS.
3 INDUCTOR PART OF P.C. BOARD.

Figure 106-3. Count Chain Schematic

A107
GATE GENERATOR
(2020197)

This assembly performs the following functions.

- Reference Oscillator Control
- Gate Generation
- Band 3 Amplitude Determination
- Power Meter Control (Option 02 only)

REFERENCE OSCILLATOR CONTROL

This circuit selects, as the time base for the counter, either the internal reference oscillator or an external 10 MHz signal applied to the rear panel. This circuit provides a 100 kHz TTL level clock signal for the gate generator, a 10 MHz TTL level clock signal for the microwave converter and, in the internal oscillator mode, a 10 MHz signal (1 volt p-p into 50 ohms) to the rear panel.

The 10 MHz internal reference signal is applied to a switchable "analog to TTL" converter (Q1, Q2, Q3). When the Ref Int/Ext line is high the TTL converter is enabled. One output goes to drive Q4, giving a square wave (1V p-p into 50 ohms) on the 10 MHz Ref line. A second output goes to NAND gate U1 (also switchable for signal isolation).The output of U1 goes to J3 to be used by the microwave converter. The output of U1 also goes to the clock input of U2. U2 is a dual decade divider that divides by 100. The output of U2 is a 100 kHz TTL clock signal to the gate generator.

When the Reference Int/Ext line is set to external (low) the TTL converter (Q1, Q2, Q3) and driver (Q4) are disabled, TTL converter (Q5, Q6, Q7) is enabled, and U1 is set to select the external input. An external reference signal applied to the 10 MHz reference line is then converted to the input of U2.

GATE GENERATOR

The Gate Generator must provide an accurate, stable, signal gate to the Count Chain. The gate must be switchable, in decade increments, between 100 micro sec and 1 sec. The gate generator consists of a programmable divide-by-N time base (U5), a dual flip-flop (U6A, U6B), and an ECL flip flop (U8). The divide ratio of U5, which determines the gate time, is set by U5 pins 12, 13, and 14 as follows.

Pin 12	Pin 13	Pin 14	Divide Ratio	Gate Time
0	0	1	10^1	100 μsec
0	1	0	10^2	1 Msec
0	1	1	10^3	10 Msec
1	0	0	10^4	100 Msec
1	0	1	10^5	1 sec

The outputs of U5 and U6 enable ECL flip-flop U8, but U8 is clocked directly from the 100kHz clock to insure gate accuracy.

When the gate is not active, U5 is permitted to free-run by holding U6B clear (T0). The gate is initialized by setting U6B. This clears U6A and clears U5 (T1). The next clock pulse sets U8 (T2). The gate is then enabled by momentarily clearing U6B (T3). The next clock sets U6A which enables U5 and U8 (T4). At T5 the gate is opened and U5 begins counting clocks (T5). Halfway through the gate, U5 pin 1 goes high (T6). After U5 has accumulated the proper number of clocks,its output, pin 1, goes low. This sets U6B, which clears U6A, and sets U8 pin 7 high (T7). The next clock closes the gate (T8). The program next clears U6B (T9), which enables the gate to free-run again (T0). See figure 107-1.

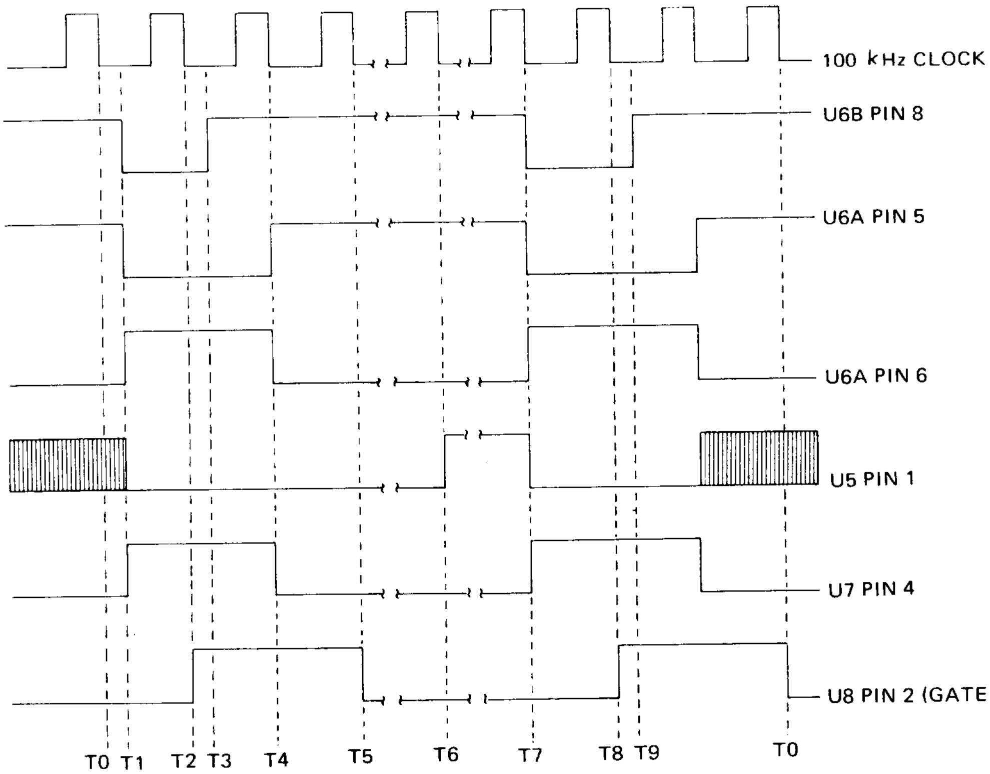


Figure 107-1. Gate Generator Timing Diagram

BAND 3 AMPLITUDE DETERMINATION

This circuit consists of three main parts.

- THE POWER METER ZERO DAC is used to automatically zero offsets in the Power Meter. It consists of two 8 bit latching DACs (U3, U4), and a comparator (U14A). All the latching DACs are driven in parallel by shift register U16, with the appropriate DAC being written to by the four write lines (U15, pins 2, 4, 6, 8). The coarse DAC (U3) has a range of ± 200 micro amps, and the fine DAC (U4) has a range of +1.5 micro amps. The Power Meter Zero DAC (U3) is adjusted so that on step 1 U14A is not set, but on the next step U14A is set. This adjusts the input to U14 to 0volts, nulling any offsets in the power meter circuit.

- THE POWER METER consists of a 15 dB switchable gain stage (U9), an 8 bit DAC used as a variable attenuator (U10), a 100 mV comparator (U14B), and a latch (half of U17). Two variable attenuators are used, on counters equipped with the option 02 power meter, to provide greater resolution (U10, U12).

  When the detected signal from the microwave converter enters U9 the power meter is first set for maximum gain and minimum attenuation. Next the latch (U17) is reset. If the input to the comparator (U14B) is greater than 100mV, latch U17 will be set. The signal amplitude to the comparator is then reduced, and the process is repeated until latch U17 no longer gets set. The input amplitude can then be calculated from the switch and DAC settings. On counters without the power meter option the amplitude is calculated to a 3dB resolution. On counters with the power meter option the amplitude is calculated to a resolution of 0.1dB.

- The POWER METER PROM (Option 02 only) contains a logic comparator (U21), a 2K x 8 PROM (U20), and a bus driver (U19). The logic comparator is connected to the microprocessor address bus, and is configured to decode the 2K address range from 4000 Hex to 47FF Hex. The comparator output drives the chip select of the PROM and the bus driver.The PROM contains the Power Meter program as well as the power correction factors. Bus driver U19 is used as a buffer for driving the microprocessor data bus.

PERIPHERAL INTERFACE ADAPTER (PIA)

The Peripheral Interface Adapter (U18) is used as the microprocessor I/O port. It has an address range from 9900 Hex to 9903 Hex. Peripheral Port A is at address 9900, and Peripheral Port B is at address 9902.

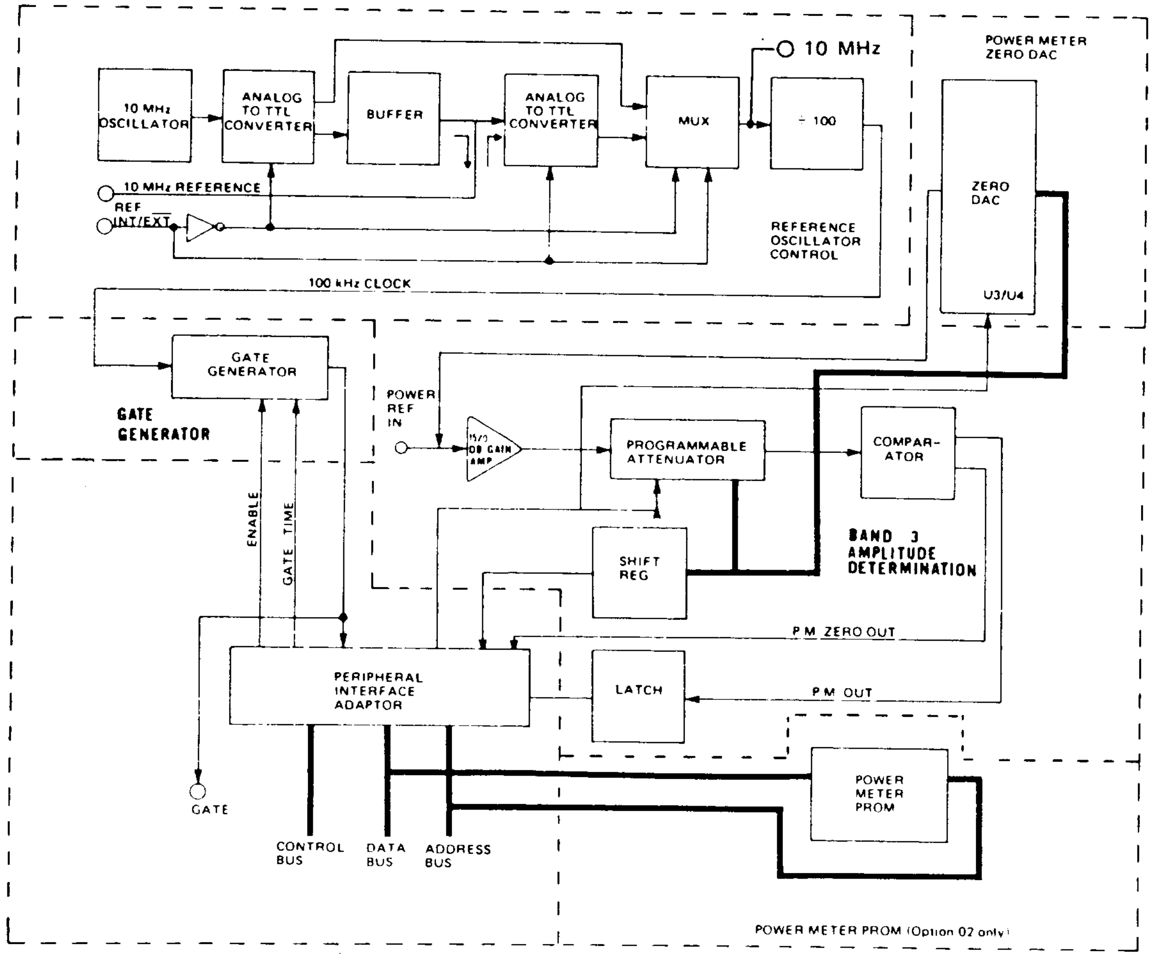


Figure 107-2. Gate Generator Block Diagram

A107 GATE GENERATOR

2020197-09 B

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A107	Gate Generator Assy -05/06	2020197	1	EIP	34257
	A113 Crystal Osc	2030002	Ref		
C1	Cer, .01μF, 20%, 100V	2150003	15	TG - S10	72982
C2	C1				
C3	Tant, 33μF, 20%, 10V	2300015	4	TAPA33M10	14433
C4 thru C7	C1				
C8	Mica, 22pF, NOM, 5%, 500V, SAT	2269999	1		
C9	Tant, 1μF, 20%, 35V	2300008	1	TAPA 1.0M35	14433
C10	Mica, 33pF, 5%, 500V	2260021	2	CD10ED330J03	72136
C11	Mica, 100pF, 5%, 500V	2260034	1	CD10FD101J03	72136
C12	C10				
C13 thru C15	C1				
C16	Tant, 10μF, 20%, 25V	2300029	2	DF106M25S	NEC
C17	C1				
C18	C3				
C19	C3				
C20	C1				
C21	C1				
C22	C3				
C23	C1				
C24	C1				
C25	C16				
C26	C1				
CR1	Hot Carrier	2710004	1	5082-2835	28480
CR2	Hot Carrier	2710006	1	5002-2800	HP
CR3	Not Used				
CR4	Zener, 6.2V	2700827	1	IN827	
R1	Comp, 10 ohm, 5%, 1/4W	4010100	2	RC07GF100J	81349
R2	Comp, 1K, 5%, 1/4W	4010102	2	RC07GF102J	81349
R3	Comp, 620, 5%, 1/4W	4010621	2	RC07GF621-J	81349
R4	Comp, 2.2K, 5%, 1/4W	4010222	3	RC07GF222J	81349
R5	Comp, 220, 5%, 1/4W	4010221	2	RC07GF221J	81349
R6	Comp, 510, 5%, 1/4W	4010511	2	RC07GF511J	81349
R7	Comp, 200, 5%, 1/4W	4010201	1	RC07GF201J	81349
R8	Comp, 27, 5%, 1/4W	4010270	1	RC07GF270J	81349
R9	Comp, 300, 5%, 1/4W	4010301	1	RC07GF301J	81349
R10	Comp, 4.7K, 5%, 1/4W	4010472	6	RC07GF472J	81349
R11	R1				
R12	Comp, 2K, 5%, 1/4	4010202	2	RC07GF202J	81349
R13	R10				
R14	R4				
R15	R5				
R16	R6				
R17	R3				
R18	Met Ox, 5.6K, 2%, 1/4W	4130562	1	C4/2%/5.6K	24546
R19	Met Ox, 3.3K, 2%, 1/4W	4130332	1	C4/2%/3.3K	24546
R20	Met Ox, 27, 2%, 1/4W	4130270	1	04/1%/27	24546
R21	Comp, 2.7K, 5%, 1/4W	4010272	1	RC07GF272J	81349
R22	R10				
R23	R10				
R24	R2				

A107 GATE GENERATOR continued

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R25	R12				
R26	R4				
R27	Met Ox, 30K, 2%, 1/4W	4130303	1	C4/2%/30K	24546
R28	Met Ox, 39K, 2%, 1/4W	4130393	1	C4/2%/39K	24546
R29	Prec, 1.69K, 1%, 1/10W	4051691	1	RN55C1691F	81349
R30	Prec, 1.82K, 1%, 1/10W	4051821	1	RN55C1821F	81349
R31	Prec, 57.6K, 1%, 1/10W	4055762	1	RN55C5762F	81349
R32	Comp, 36K, 5%, 1/4W	4010363	1	RC07GF363F	81349
R33	Comp, 15K, 5%, 1/4W	4010153	1	RC07GF153F	81349
R34	Met Ox, 750, 2%, 1/4W	4130751	1	C4/2%/750	24546
R35	Prec, 6.19K, 1%, 1/8W	4056191	1	RN55C6191F	81349
R36	Prec, 100, 1%, 1/8W	4051000	1	RN55C1000F	81349
R37	R10				
R38	R10				
R39	Met Ox, 10K, 2%, 1/4W	4130103	2	C4/02/10K	24546
R40	R39				
R41	Comp, 10K, 5%, 1/4W (option only)	4010103	1	RC07GF103J	81349
RN1	5 x 10 K, 0.3W, 2%	4170005	1	4608X-101-682	57924
Q1	NPN - General Purpose	4704124	4	2N4124	
Q2	PNP - General Purpose	4704126	3	2N4126	
Q3	Q1				
Q4	Q2				
Q5	Q1				
Q6	Q2				
Q7	Q1				
Q8	DMOS, FET SW	4710031	1	SD215	18324
U1	Quad Schmitt NAND	3084132	1	SN74LS132	01295
U2	Dual Decade Counter	3084490	1	SN74LS490N	01295
U3	8 Bit DAC	3057524	3	AD7524JN	
U4	U3				
U5	Digital P Chan. MOS Divider	3035009	1	MK5009P	
U6	D Type Pos Flip-flop	3087474	2	SN74LS74N	01295
U7	Quad 21NP NOR Gate	3087402	1	SN74LS02N	01295
U8	Digital Dal D Flip-flop	3110131	1	MC10131L	04713
U9	Dual Low Noise Op Amp	3045534	1	NE5534N	
U10	8 Bit DAC Buff	3057524		AD7524LN	
U11	Op Amplifier	3040308	2	LM308AN	27014
U12	U10 (Option 02 only)				
U13	U11				
U14	Comparator	3050393	1	LM393N	27014
U15	Hex Buffer/Driver	3007407	1	DM7407N	27014
U16	Dual 4 Bit Static S/R	3034015	1	MC14015B	04713
U17	U6				
U18	Periph. Interface Adaptor	3086821	1	MC68B21P	04713
U19	Not Used				
U20	Not Used				
U21	Not Used				
U22	Quad Dual Flip-flop	3084175	1	SN74LS175	01295
U23	Op Amp/Lin	3040741	1	LM741CN	27014
TP1 thru TP4	.040 D Pin, Gold	2620032	4	460-2970-02-03	71279

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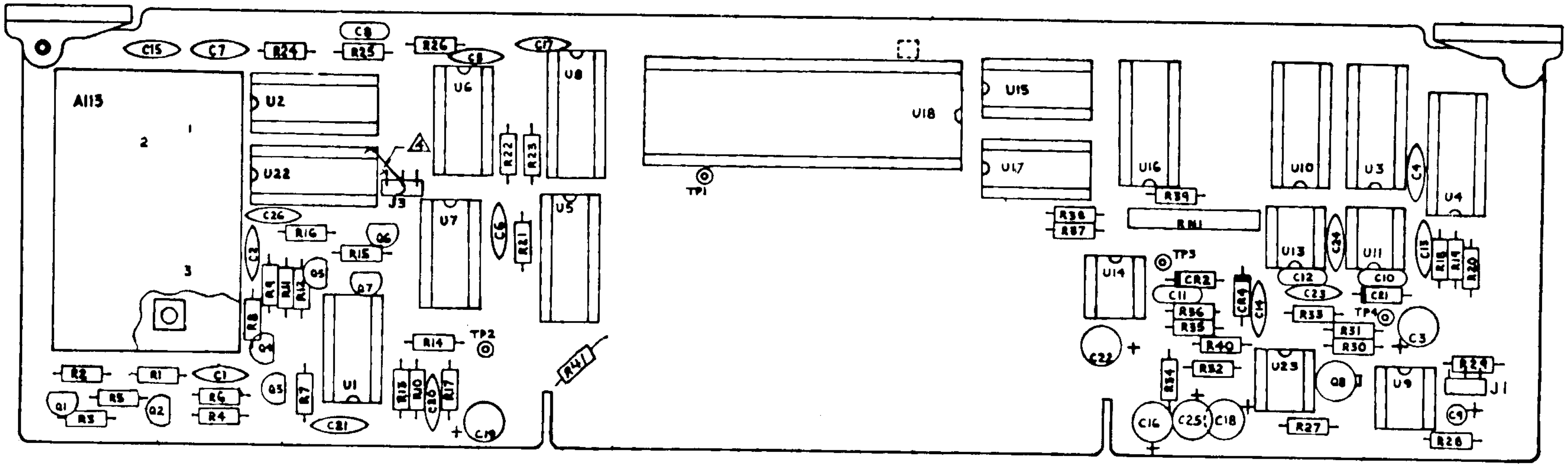
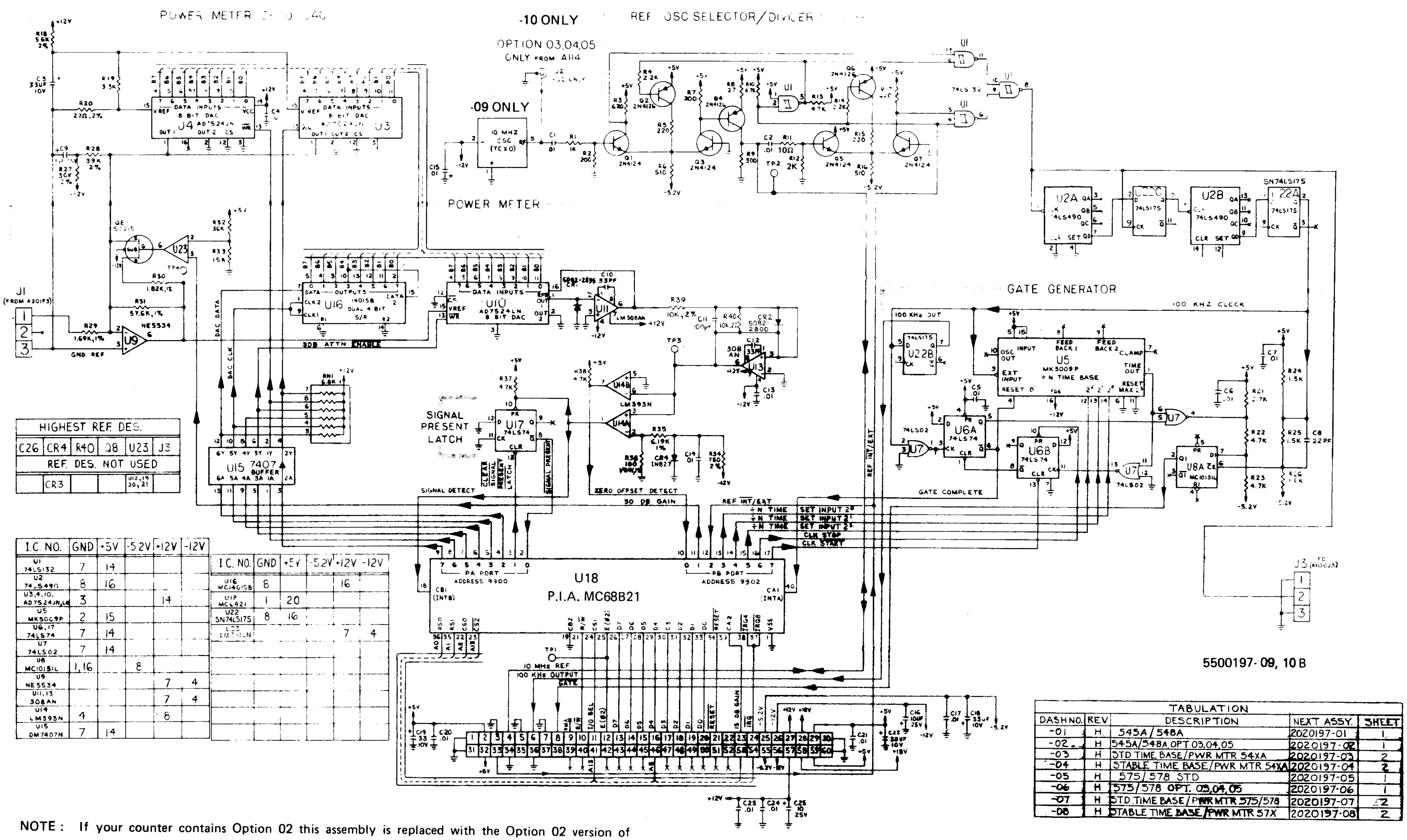


2020197-09 B

Figure 107-3. Gate Generator Component Locator

NOTE : If the counter contains Option 02 this board is replaced with 2020197-03/04.
Refer to Section 10, Option 02 for the 03/04 version of this assembly.



HIGHEST REF. DES.					
C26	CR4	R40	Q8	U23	J3
REF. DES. NOT USED					
	CR3			U12,19 20,21	

I.C. NO.	GND	+5V	-5.2V	+12V	-12V
U1 74LS132	7	14			
U2 74LS490	8	16			
U3,4,10. AD7524JN,LN	3			14	
U5 MK5009P	2	15			
U6,17 74LS74	7	14			
U7 74LS02	7	14			
U8 MC10131L	1,16		8		
U9 NE5534				7	4
U11,13 308AN				7	4
U14 LM393N	4			8	
U15 DM7407N	7	14			

I.C. NO.	GND	+5V	-5.2V	+12V	-12V
U16 MC14015B	8			16	
U18 MC6821	1	20			
U22 SN74LS175	8	16			
U23 [illegible]				7	4

5500197-09, 10 B

TABULATION				
DASH NO.	REV	DESCRIPTION	NEXT ASSY.	SHEET
-01	H	545A/548A	2020197-01	1
-02	H	545A/548A OPT 03,04,05	2020197-02	1
-03	H	STD TIME BASE/PWR MTR 54XA	2020197-03	2
-04	H	STABLE TIME BASE/PWR MTR 54XA	2020197-04	2
-05	H	575/578 STD	2020197-05	1
-06	H	575/578 OPT. 03,04,05	2020197-06	1
-07	H	STD TIME BASE/PWR MTR 575/578	2020197-07	2
-08	H	STABLE TIME BASE/PWR MTR 57X	2020197-08	2

NOTE : If your counter contains Option 02 this assembly is replaced with the Option 02 version of the Gate Generator part number 5500197-03/04. See Section 10 for Option 02.

Figure 107-4. Gate Generator Schematic

A108
CONVERTER CONTROL
(2020200)

The Converter Control performs two major functions. One of the functions is to provide a precise yig tuning current which is controlled by the microprocessor via P.I.A. U4. The other function is to phase lock the VCO in the microwave converter to a selected harmonic of a 50 kHz reference signal to provide a synthesized L.O. The converter control also permits the microprocessor to control the L.O. power amplifier and provides the microprocessor input for the I. F. threshold signal.

YIG FREQUENCY CONTROL DAC and DRIVERS

The yig tuning current is supplied by the yig driver (U3, Q1, Q2, & Q3) which is controlled by the DAC. The DAC is composed of a 12 bit monolithic DAC (U2), summing amplifier (U1) and resistors to provide a total resolution of 14 bits. PA ports 0 and 1 of the P.I.A. (U4) are used to drive the 2 least significant bits of the DAC directly. A change in the least significant bit of the DAC corresponds to a yig frequency change of 2 MHz. A voltage analog of yig current appears across R25 and is compared to the DAC output at the summing junction of U3, with resistors R1 and R19.

The slope of yig current vs DAC voltage is compensated with corrections through software.

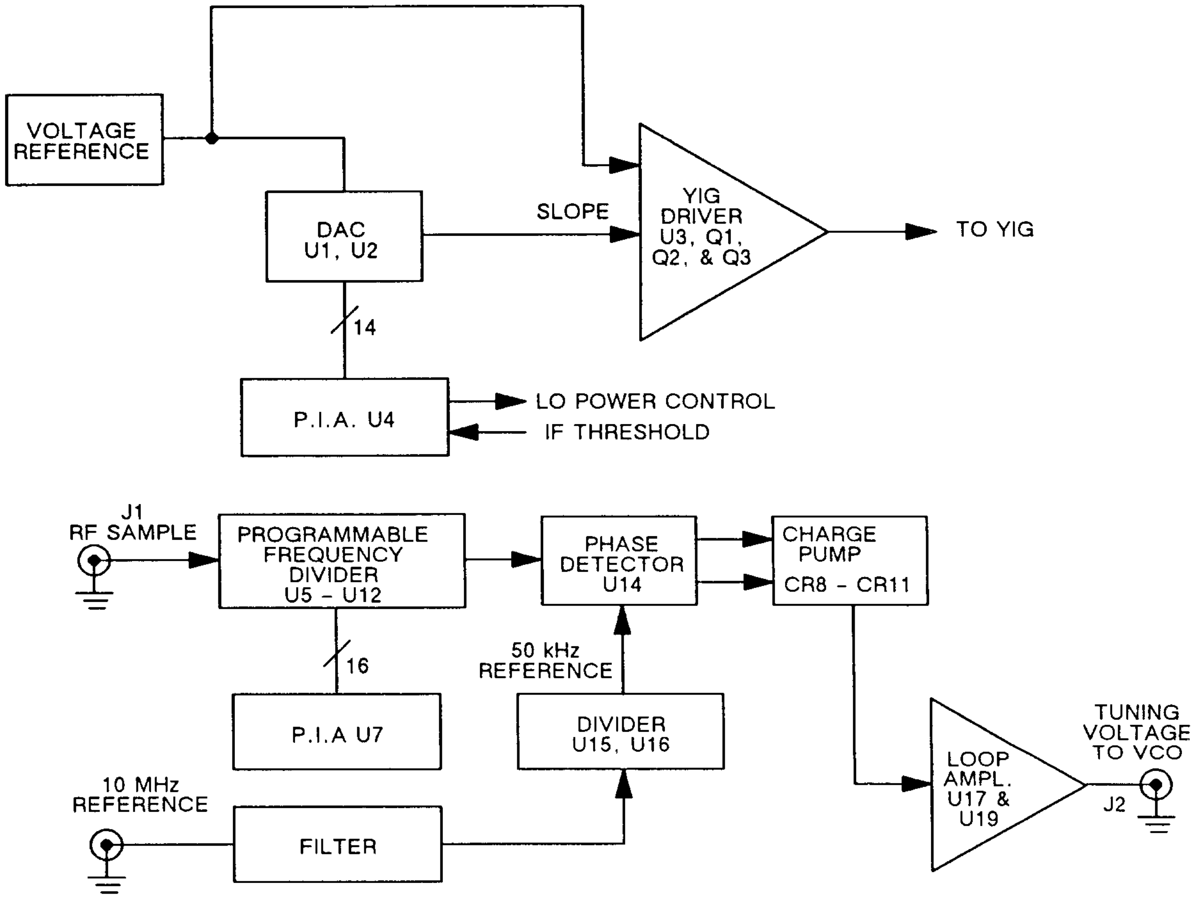


Figure 108-1. Converter Control Diagram

VCO CONTROL

The VCO control, together with the VCO, form a phase lock loop frequency synthesizer. The frequency range over which the synthesizer is used is from 370 MHz to 500 MHz.

An output of the VCO (via a buffer amplifier Q2 on the Band 2 converter board) is applied to the programmable frequency divider (U5-U13). The programmable frequency divider is programmed by the microprocessor via P.I.A. U7. The output of the programmable frequency divider is compared to the 50 kHz reference (derived from a 10 MHz clock from the gate generator board) in the phase detector U14. A phase difference between the divided down VCO and the 50 kHz reference will result in an output from the phase detector. The phase detector has two output ports, a pump-up port and a pump-down port. Pump-down is U14, pin 2. Pump-down is normally high and goes low to reduce the VCO frequency. Pump-up is U18, pin 3. Pump-up is normally low and goes high to increase the VCO frequency. The outputs of the phase detector go to the charge pump, which converts them to a single tri-state output. The charge pump output is open with no pump command, sources current with pump-up, and sinks current with pump-down. The output of the charge pump is connected to the input of the loop amplifier U19 and U17. The loop amplifier provides the proper gain and filtering to achieve the desired loop response. The output of the loop amplifier is the VCO tuning voltage.

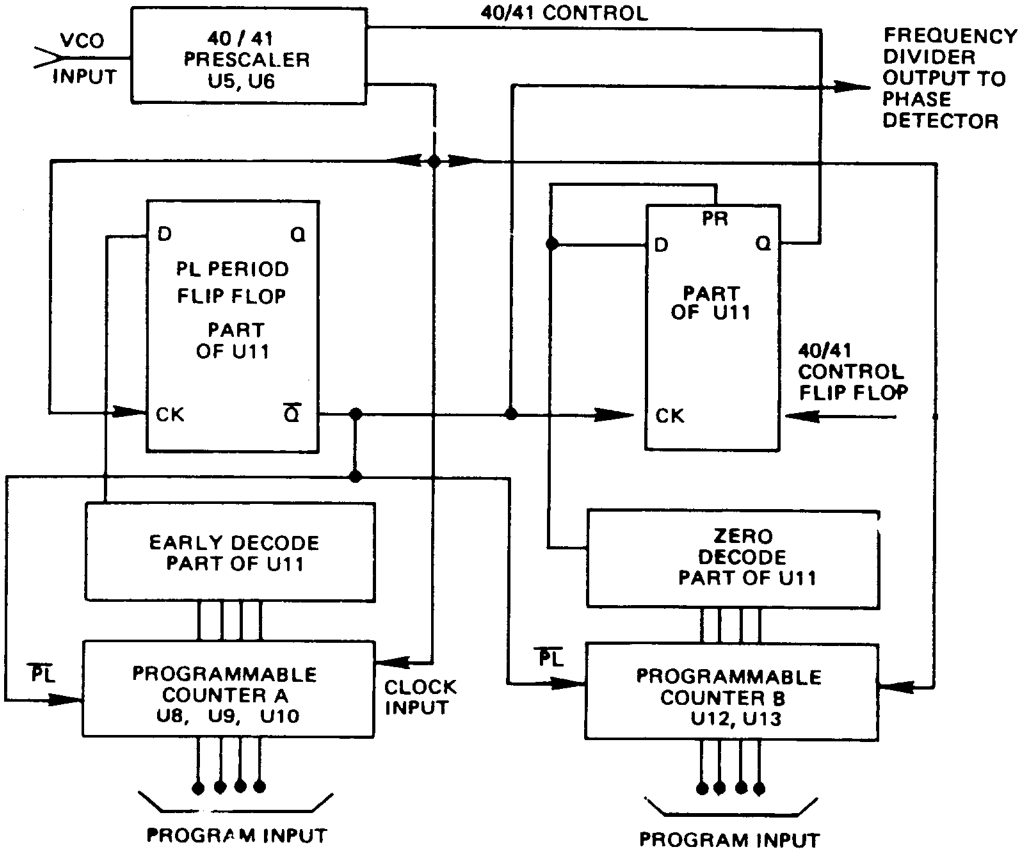


Figure 108-2. Programmable Frequency Divider Diagram

PROGRAMMABLE FREQUENCY DIVIDER

The programmable frequency divider uses a two modulus (divide number) prescaler (U5, U6) and two programmable counters (A & B). The prescaler is used to divide the VCO frequency down to a lower frequency which can be handled by low power Schottky TTL programmable counters. The two modulus prescaler permits prescaling without loss of resolution. At the start of the programmable frequency divider cycle, the prescaler is set to divide by the larger modulus (41), and both programmable counters have been loaded with their respective program numbers from the PIA. The programmable counters each decrement 1 count for each output pulse from the prescaler. When programmable counter B (U12, U13) reaches the count of zero the 40/41 control flip-flop (part of U11)changes state and causes the prescaler to divide by the lower modulus (40). When programmable counter A reaches the count of 2 the D input of the PL period flip-flop (part of U11) goes high, so that on the count of 1 the flip-flop changes state, which causes both programmable counters to be reloaded with their respective program numbers and the 40/41 control flip-flop to reset (prescaler in ÷ 41 state). The very next count causes the PL period flip-flop to reset, starting the programmable frequency divider cycle over again. The equation for the divide ratio of the programmable frequency divider N_d is:

$$N_d = 40 (N_{\text{counter A}}) + N_{\text{counter B}}$$

with the condition that:

$N_{\text{counter B}}$ must not exceed $N_{\text{counter A}}$

The weighting of the command bits is:

U9 P_1 – 400MHz
U9 P_0 – 200MHz
U8 P_3 – 160MHz
U8 P_2 – 80MHz
U8 P_1 – 40MHz
U8 P_0 – 20MHz
U10 P_3 – 16MHz
U10 P_2 – 8 MHz
U10 P_1 – 4MHz
U10 P_0 – 2MHz
U13 P_3 – 1.6MHz
U13 P_2 – 0.8MHz
U13 P_1 – 0.4MHz
U13 P_0 – 0.2MHz
U13 P_1 – 100KHz
U13 P_0 – 50KHz

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A108 CONVERTER CONTROL

2020200-04 B

REF DES	DESCRIPTION	EIP NO.	PER ASSY	TYP MFG NO.	TYP FSCM NO.
A108	CONVERTER CONTROL ASSY	2020200-02	1	EIP	34257
C1	Disc, .005µF, 20%, 100V	2150008	1	TG-D50	56289
C2	Disc, .01µF, 20%, 100V	2150003	14	TG-S10	56289
C3	Cer, .047 µF, 10%, 50V	2150090	1	6123X7R473KA50K	13011
C4	Tant, 1µF, 10%, 35V	2300008	3	TAPA 1.0M35	14433
C5	C4				
C6	C2				
C7	Cer,.001 µF, 20%, 100V	2150001	4	5GA-D10	56289
C8	C4				
C9	Tant, 33µF, 10%, 10V	2300015	2	TAPA 33M10	14433
C10	C7				
C11	C7				
C12	C7				
C13 thru C17	C2				
C18	Tant, 10pF, 20%, 25V	2300029	4	DF106M25S	72136
C19	C18				
C20	C9				
C21	C18				
C22 thru C24	C2				
C25	Cer, 560pF, 5%, 100V	2150029	2	SR211A561JAA	14158
C26	Tant, .47µF, 20%, 35V	2300005	1	TAPA-47M35	14433
C27	Cer .022 µF, 15%, 50V	2350027-00	1	2130X7R050R223K	26654
C28	C18				
C29	C2				
C30	Cer, 330pF, 10%, 100V	2150030	1	SR211A331KAA	14158
C31	Tant, 2.2µF, 50%, 16V	2300012	1	TAPA 2-2M16	14433
C32	Mica, 82pF, 5%, 500V	2260032	2	CD10ED820J03	72136
C33	C2				
C34	Mica, 430-470 pF, 5%, 500V, SAT	2259999	1		
C35	Mica, 470 pF, 5%, 500V	2250018	1	DM-15-471J	72136
C36	Mica, S.A.T.	2269999	1	30pF, NOM.	
C37	Cer, .1µF, 10%, 50V	2150028	1	RC50104KB	Murata
C38	C2				
C39	Cer, 2200pF, 5%, 100V	2150026	1	SR211A22JAA	14158
C40	C25				
C41	C2				
C42	C32				
CR1	Hot Carrier	2710004-00	1	5082-2835	28480
CR2	Zener, 56V	2704758-00	1	IN4757	07263
CR3	General Purpose	2704148	14	IN4148	07263
CR4	Zener, 6.2V	2700827	1	IN827	07263
CR5	Power Rectifier	2704001	1	IN4001	07263
CR6 thru CR18	CR3				
L1	Inductor, 100µH	3520007	1	1537-76	99800
L2	Inductor, 1µH	3510018	1	1537-12	99800
L3	Inductor, 4700µH	3510017	2	1641-475	99800
L4	L3				
Q1	PNP	4710009	1	MJE350	04713
Q2	PNP Amplifier	4710018	1	MPSL51	04713
Q3	NPN General Purpose	4704124	1	2N4124	04713

A108 CONVERTER CONTROL

2020200- 04 B

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R1	Res, 8.00K, 1/10W, 1%	4120022	1	VAR-1/10C-6-1%-723K	ACI
R2	Comp, 4.7K, 5%, 1/4W	4010472	1	RC07GF472J	81349
R3	Comp, 1K, 5%, 1/4W	4010102	6	RN55C4992F	81349
R4	Not Used				
R5	Met Ox, 390 ohm, 2%, 1/4W	4130391	2	C4/2%/390	24546
R6	Not Used				
R7	Not Used				
R8	R3				
R9	Not Used				
R10	Not Used				
R11	Not Used				
R12	Not Used				
R13	R5				
R14	Comp, 750, 5% 1/4W	4010751	1	RC07GF751J	81349
R15	Comp, 820K, 5%, 1/4W	4010824	1	RC07GF824J	81349
R16	R3				
R17	Met Ox, 1.6K, 2%, 1/4W	4130162	1	C4/2%/1.6K	24546
R18	Comp, 1.60K, 5%, 1/4W	4010164	1	RC07GF164J	81349
R19	Prec, 3.01K, 1%, 1/10W	4120020	1	VAR-1/10C-6-1%	ACI
R20	Comp, 10K, 5%, 1/4W	4010103	3	RC07GF103J	81349
R21	Comp, 82K, 5%, 1/4W	4010823	1	RC07GF823J	81349
R22	R20				
R23	R20				
R24	R3				
R25	Wire Wound 5, 1%, 7W	4110003	1	T7 (10 PPM)	12463
R26	Comp, 2.7K, 5%, 1/4W	4010272	1	RC07GF272J	81349
R27	Comp, 51, 5%, 1/4W	4010510	2	RC07GF510J	81349
R28	Comp, 390, 5%, 1/4W	4010391	3	RC07GF391J	81349
R29	R28				
R30	R28				
R31	R3				
R32	Comp, 100, 5%, 1/4W	4010101	3	RC07GF101J	81349
R33	R3				
R34	Comp, 2.4K, 5%, 1/4W	4010242	1	RC07GF242J	81349
R35	R32				
R36	Comp, 220K, 5%, 1/4W	4010224	1	RC07GF224J	81349
R37	R32				
R38	Comp, 4.3K, 5%, 1/4W NOM S.A.T.	4010999	1	SAT	81349
R39	Comp, 2K, 5%, 1/4W	4010202	1	RC07GF202J	81349
R40	R27				
R41	Comp, 1.5M, 5%, 1/4W	4010155	1	RC07GF155J	81349
R42	Comp, 300, 5%, 1/4W	4010301	1	RC07GF301J	81349
R43	Comp, 8.2K, 5%, 1/4W	4010822	1	RC07GF822J	81349
R44	Comp, 51K, 5%, 1/4W	4010513	2	RC07GF513J	81349
R45	Comp, 5.1K, 5%, 1/4W	4010512	1	RC07GF512J	81349
R46	R44				
R47	Comp, 3.3K, 5%, 1/4W	4010332	1	RC07GF332J	81349
U1	Prec, J-FET Op Amp	3041016	1	OP16FJ	06665
U2	12 Bit DAC	3050012	1	H57541-J	0000X
U3	Op Amp, Lin.	3040741	1	LM741CN	27014
U4	Peripheral Interface Adaptor	3086821	2	MC68B21P	04713
U5	Two-Mod Prescaler	3112013-02	1	MC12013L	04713
U6	Digital Dual "D" Flip-flop	3110131	1	MC10131L	04713
U7	U4				
U8 thru U10	UP/DOWN Counter	3084192	4	DM74LS192N	27014

A108 CONVERTER CONTROL

2020200-04 B

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
U11	Counter Control Logic	3112014	1	MC12014P	04713
U12	UP/DOWN Counter	3084193	1	DM74LS193N	27014
U13	U8				
U14	Phase Frequency Detector	3014044	1	MC4044P	04713
U15	Quad Dual Flip-flop	3084175	1	SN74LS175	01295
U16	Decade Counter	3084490	1	SN74LS490N	01295
U17	J-FET Op Amp	3040071	2	TL071CP	01295
U18	Quad 2 INP NAND	3087400	1	DM74LS00	27014
U19	U17				

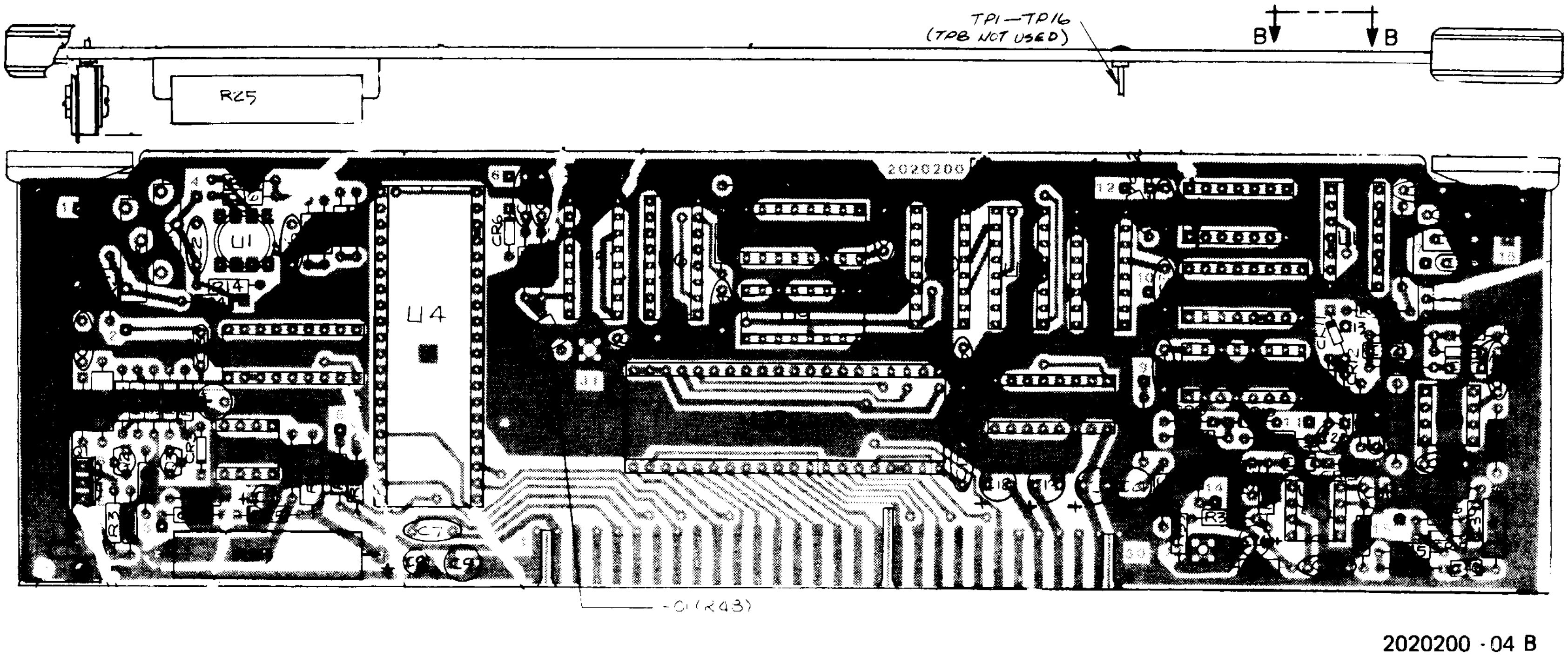
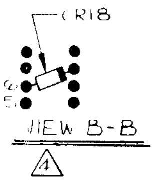


Figure 108-3. Converter Control Component Locator



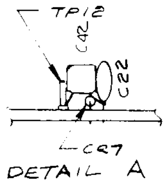
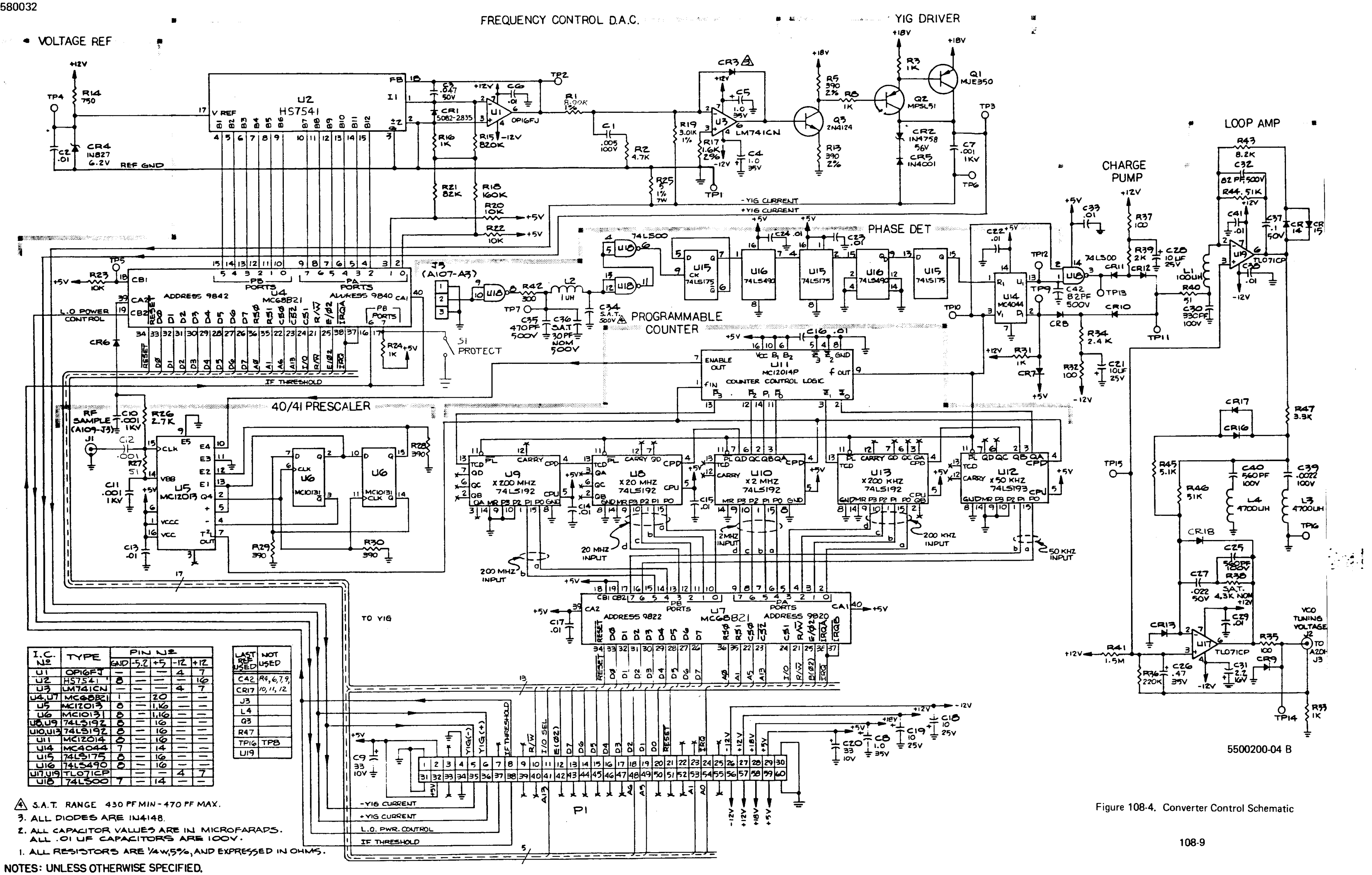


Figure 108-4, Schematic Diagram, Converter Control, is changed from Rev. K to Rev. L, but this does not change any part of the drawing shown in this figure.



I.C. №	TYPE	PIN №				
		GND	-5.2	+5	-12	+12
U1	OP16FJ	—	—	—	4	7
U2	HS7541	8	—	—	—	16
U3	LM741CN	—	—	—	4	7
U4, U7	MC68B21	1	—	20	—	—
U5	MC12013	8	—	1,16	—	—
U6	MC10131	8	—	1,16	—	—
U8, U9	74LS192	8	—	16	—	—
U10, U13	74LS192	8	—	16	—	—
U11	MC12014	8	—	16	—	—
U14	MC4044	7	—	14	—	—
U15	74LS175	8	—	16	—	—
U16	74LS490	8	—	16	—	—
U17, U19	TL071CP		—	—	4	7
U18	74LS00	7	—	14	—	—

LAST REF USED	NOT USED
C42	R4, 6, 7, 9, 10, 11, 12
CR17	
J3	
L4	
Q3	
R47	
TP16	TP8
U19	

4 S.A.T. RANGE 430 PF MIN - 470 PF MAX.

3. ALL DIODES ARE 1N4148.

2. ALL CAPACITOR VALUES ARE IN MICROFARADS. ALL .01 UF CAPACITORS ARE 100V.

1. ALL RESISTORS ARE 1/4W, 5%, AND EXPRESSED IN OHMS.

NOTES: UNLESS OTHERWISE SPECIFIED.

5500200-04 B

Figure 108-4. Converter Control Schematic

A109
BAND 2 CONVERTER
(2020139)

The Band 2 Converter accepts Band 1 and Band 2 RF signals from the front panel, and local oscillator (LO) signal from the Band 3 Converter (A203). The appropriate signal is selected and processed to produce an IF signal between 10 Hz and 200 MHz. The IF signal output is sent to the Count Chain board (A106), and lock information is routed through the PIA (peripheral interface adapter) U2 to the Microprocessor (A105).

IMPEDANCE CONVERTER

Band 1 input from the front panel enters the converter at J6 and is terminated by R75. The signal is coupled to the input of a field effect transistor (FET) amplifier (Q15) through an RC network (R73, C42). Two limiter diodes (CR4, CR5) protect the FET against large input signals. The FET is a source follower with slightly less than unity gain. The FET drives a buffer amplifier (Q14) which has enough gain to increase the impedance converter overall gain to near unity. A decoupling capacitor (C39) controls the amplifiers low frequency cutoff, and C41 provides high frequency peaking to keep the gain flat to frequencies above 100 MHz.

SIGNAL SELECT

The output of the impedance converter circuit drives one input of the signal select circuitry. Signal selection is made by enabling one of three differential amplifiers, U4A, U4B, or U5A. When Band 1 is selected, a logic high signal on the PIA (U2 pin 2) turns on Q16. Q16 biases on the current source in U4A. This current source generates an 11mAcurrent which is split between the two differential amplifier transistors in U4A. The currents from pins 5 and 6 flow through matched collector loads (R94, L7/R95, L8). R94 and R95 are equal, and are selected for the proper low frequency gain during board alignment. Inductors L7 and L8 provide peaking to give an approximate flat gain through 200MHz.

The next stage is a differential amplifier similar to U4A, but it is driven differentially. To generate a single ended output signal, one output of U5B (pin 12) is passed through a current mirror (Q18). The output of the current mirror is then added to the second output of U5B (pin 11) at J5. The load for this stage is a 51 ohm resistor located on the A106 Count Chain board in order to terminate the coax for RF signals. In the quiescent state, the current from Q18 equals the collector current of the differential amplifier U5B, and the output current is zero. When a signal is applied, the current will be unbalanced to generate a signal at the load resistor. To provide frequency compensation of the current mirror, an RC network (R108, C54) is connected between the emitter of Q18 and ground.

BAND 1 LOCK DETECTOR

The output signal at J5 is coupled to detector CR12. Amplifier U6 is a threshold comparator that will produce a logic low signal when the IF output from J5 is more than −6dBm. The output of U6 goes through a resistor divider network to generate a 5V TTL logic signal for the PIA. R90 provides about 1 dB of positive feedback at threshold level to prevent erratic output from the comparator.

ISOLATION AMPLIFIER

The Band 2 input signal enters on J4. This RF signal is terminated in 50 ohms by the combination of R1 and the input impedance of the amplifier. The input signal level is detected by CR1, filtered by C3, and applied to one input of the Band 2 lock detector (U1).

The isolation amplifier is a common base amplifier with a gain of −10 dB. An input signal range of +10 to −20dBm is translated to a 0 to −30dBm range into the mixer so the mixer will be in its linear range for all signal input levels. The amplifier peaks slightly near 1 GHz to overcome an increase in mixer conversion loss at these frequencies.

MIXER OPERATION

The local oscillator (LO) is applied to the IF terminal and the IF is removed from the LO terminal. This swap allows the mixer (MX1) to be unbalanced and act as a low loss attenuator for signals between 10MHz and 200MHz where no mixing is necessary. The mixer has a nominal 400MHz LO for signals between 200MHz and 600MHz; and has a nominal 800MHz LO for signals between 600MHz and 1GHz. A 980MHz LO allows operation with input signals to 1160MHz.

IF AMPLIFIER

The output of the mixer drives an IF amplifier through a 7 section, 200MHz low-pass filter. The IF amplifier is a "feedback pair" amplifier whose gain is stabilized by feedback, to be equal to 24dB. Inductor L6 is used to extend the high frequency response to 200MHz. The 1 pF capacitor (C26) between R34 and R35 is a low pass filter to reduce the 1200 to 1500 MHz LO harmonics that reach the IF amplifier.

BAND 2 LOCK DETECTOR

The IF amplifier output goes to the signal select circuit and to the Band 2 Lock Detector. The Band 2 Lock Detector has a voltage proportional to the IF level on the positive input, and a voltage proportional to the RF signal on the negative input. The conversion gain from RF input to IF amplifier output is a +6dB for all valid signals, and less than −6dB for all spurious signals. The output of U1 is positive only when a valid IF signal is present. A small offset is added by R12 and R13 to guarantee a non lock condition when no signal is present. Resistor R9 provides about 1dB of positive feedback to prevent erratic output from noise at the point of threshold.

LO BUFFER

The VCO signal from the Band 3 Converter (A201A, J2) enters on J1. The signal goes through a 6 dB attenuator (R111, R112, R114), and a low pass filter (L1, C63, C64) to attenuate high order harmonics, and is terminated by a 51 ohm resistor (R16). Two high input impedance signal splitters (Q2, Q3) get their input signals from R16. Q2 and Q3 operate on the same basic principal. One output is taken from the emitter (acting as an emitter follower) that provides unity gain for the input signal. The AC terminating impedance on the emitter is adjusted to be 50 ohms so the amplifier will act as a unity gain amplifier for the 50 ohm load that terminates the collector when a coax cable is connected. Q2 has an additional transformer (T1) in its collector lead to increase the signal output to J3 by about 4 dB.

DIVIDE-BY-TWO

The emitter output of Q3 drives the input of a divide-by-two IC (U3). The impedance is held at 50 ohms by two terminating/biasing resistors (R61, R62). The resistors keep the input bias to U3 below the emitter-coupled logic (ECL) low level (approx. −2.0V). The microprocessor enables self-test by putting a low level signal on pin 5 of the PIA (U2). This turns on Q13, and raises the voltage at U3 pin 7 to the center of an ECL signal (approx. −1.2V). This allows U3 to divide the input signal by two. The output of U3 goes to the signal select circuits.

LO SELECT

The signal from the emitter of Q2 drives the LO select circuitry. The LO provides one (of three) signals to the mixer (MX1). In Band 2A a bias current is generated to unbalance the mixer and allow signals below 190MHz to pass. In Band 2B a 370MHz or 425MHz LO signal is generated that will mix with signals of 200 to 600MHz, and provide the 10 to 200MHz IF signal desired. In Band 2C a 750MHz, 850MHz or 980MHz LO signal is generated to mix with input signals between 600MHz and 1160MHz to provide the desired IF signal.

In Band 2A, the 3mAcurrent to bias mixer MX1 is generated when Q12 is turned on by the PIA, to apply +12V to MX1 through R57. This will allow signals to pass that are less than the cutoff frequency of the low pass filter (200MHz). The LO signal to mixer MX2 from Q2 is not allowed to pass MX2 because of the inherent balance of the mixer. No signal can enter pin 2 of MX2 because Q7 has been saturated, removing bias from buffer Q5, and shunting any RF signals to ground.

When Band 2B is selected, Q12 is turned off thus balancing mixer MX1; Q6 is turned on to unbalance mixer MX2. With MX2 unbalanced, the LO signal from Q2 can pass through MX2 and be amplified by Q10 and Q11, and be applied to mixer MX1.

When Band 2C is selected both Q6 and Q12 are off, and both mixers are balanced. In this mode Q7 is shut off and an LO signal is applied to pin 1 and 2 of MX2. The sum output of MX2 is selected by a DC blocking capacitor (C31). This sum (that is,two times the incoming LO frequency) is amplified by Q10 and Q11 and applied to MX1.

The Q10 and Q11 amplifier is a series shunt pair. Q10 applies most of the RF input signal across the emitter resistor R47. This determines the transistor emitter current, which will be the collector current if the output is terminated in a low impedance. Q11 is used as a current-to-voltage converter. The output voltage of this converter is the product of the input current times the feedback resistor (R51). Since the input of this stage is a summing junction, it appears very close to zero ohms to the previous stage, Q10. The voltage gain of the two transistors can be approximated by R51/R47, which is about 3 or 10dB. Since the gain required at 800MHz is slightly greater than required at 400MHz, a low pass matching network (consisting of L2 and C20) peaks the output signal current to MX1 at 800 MHz. The remaining components around Q10 and Q11 are used to bias the transistors. Shunt biasing is used to provide collector bias voltages of 3.4V for Q10, and 4.7V for Q11.

OPTION SELECTION

Provision has been made on this assembly for a set of jumpers that will let the microprocessor know when it has the components required for a 578B(26.5 GHz) counter, and if it has an extended frequency option (Option 06). These jumpers are read by the microprocessor when the counter is turned on, and it selects micro code which is applicable only when those options are available. A jumper from E1 to E3 (from pins 8 and 9 on the PIA U2) indicates that this is a 578B counter.

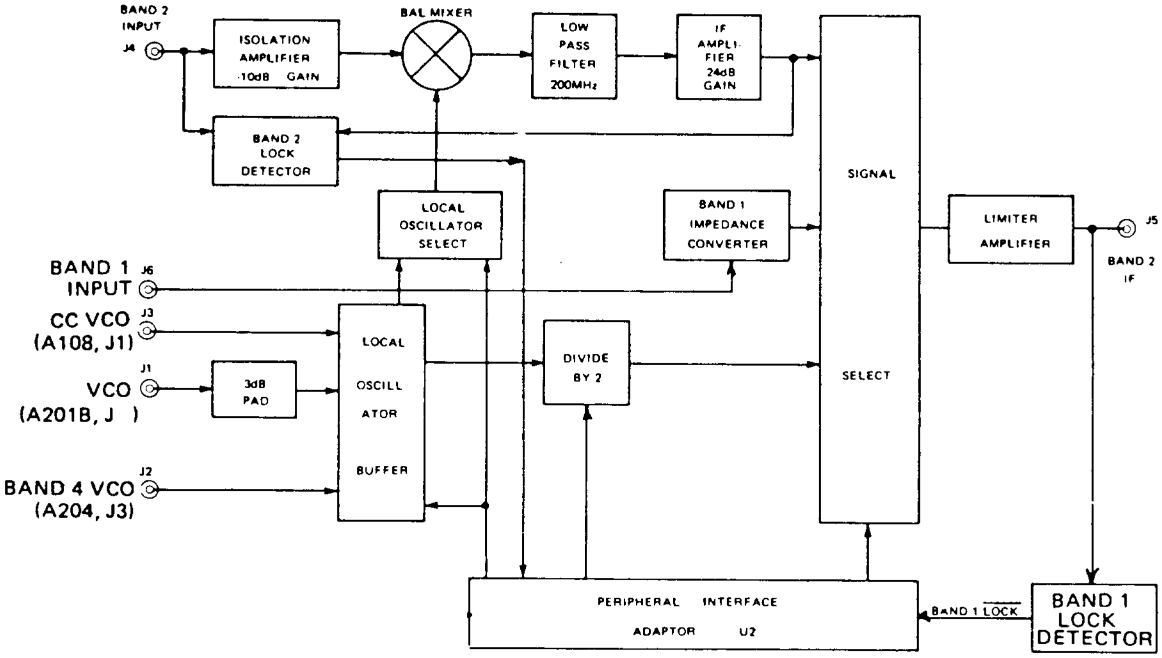


Figure 109-1. Band 2 Converter Block Diagram

A109 BAND 2 CONVERTER

2020139-05,06 A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A109	Band 2 Converter Assy	2020139-03	1	EIP	34257
C1	Cer, .01μF, 10%, 100V	2150014	9	6123X7R103KA100	26654
C2	C1				
C3	Cer, .001μF 10%, 100V	2150015	11	6183X7R102KA100	26654
C4 thru C6	C1				
C7	Mica, 100pF, 5%, 500V	2260034	3	FD101J03	72136
C8	Disc, .001μF, 20%, 1KV	2150001	8	SGA - D10	56289
C9	Disc, .01μF, 20%, 100V	2150003	11	TG - S10	56289
C10	C8				
C11	C8				
C12	C7				
C13	C8				
C14	C7				
C15 thru C18	C3				
C19	C8				
C20	Mica, 1pF, 100%, 500V	2260005	2	CD010C03 (2260015)	56289
C21	Mica, 18pF, 5%, 500V, NOM - S.A.T.	2260999	1	CD180J03 (2260021)	56289
C22	Mica, 33pF, 5%, 500V, NOM - S.A.T.	2260999	2	ED330J03	56289
C23	C22				
C24	Mica, 27pF, 5%, 500V, NOM - S. A. T	2260999	1	CD270J03	56289
C25	C1				
C26	C20				
C27	Not Used				
C28	C1				
C29	C9				
C30	C1				
C31	C3				
C32	C3				
C33	C1				
C34 thru C36	C3				
C37	C9				
C38	C3				
C39	Tant, 100μF, 20%, 6.3V	2300024	1	TAG20 - 47/6.3 - 50	14433
C40	C9				
C41	Mica, 22pF, 5%, 500V	2660017	1	ED220J03	72136
C42	Mica, 47pF, 5%, 500V	2260004	1	DM10 - 470J	72136
C43	Tant, 33μF,10%, 10V	2300015	6	TAG20 - 33/10 - 50	14433
C44	C9				
C45	C43				
C46	C8				
C47 thru C49	C9				
C50	Tant, 10μF, 20%, 25V	2300029	3	TAG20 - 10/25	14433
C51	C43				
C52	C9				
C53	C9				
C54	Mica, 18pF, 5%, 500V	2260015	1	CD180J03	56289
C55	C8				
C56	C8				
C57	C50				

A109 BAND 2 CONVERTER, continued

2020139-05, 06 A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
C58	C43				
C59	C9				
C60	C43				
C61	C50				
C62	C43				
C63	Mica, 8pF, 5%, 500V	2260011	2	CD080J03	56289
C64	C63				
CR1	Mix UHF	2710038	3	ND4991	00005
CR2	Not Used				
CR3	CR1				
CR4	General Purpose	2704148	3	1N4148	07263
CR5	CR4				
CR6 thru CR10	Not Used				
CR11	CR4				
CR12	CR1				
L1 thru L5	Part of Board				
L6	Inductor, 0.47 μH	3510006	1	DD - 0.47	99800
MX1	Balanced Mixer	2030016	2	TFM -2	
MX2	MX1				
Q1	NPN, RF	4710030	8	BFR-90	04713
Q2	Q1				
Q3	Q1				
Q4	PNP, General Purpose	4704124	1	2N4124	04713
Q5	Q1				
Q6	PPNP, General Purpose	4704126	7	2N4126	04313
Q7	Q1				
Q8	Q1				
Q9	Q1				
Q10	NPN, RF, graded	4710030-02	1	BFR90	04713
Q11	Q1				
Q12	Q6				
Q13	Q6				
Q14	NPN, RF	5280047	2	2N4261	01295
Q15	NN-Channel, JFET	4704416	1	2N4416	04713
Q16	Q6				
Q17	Q6				
Q18	Q14				
Q19	Q6				
Q20	Q6				
R1	Comp, 150, 5%, 1/8 W	4000151	1	RC05GF151J	81349
R2	Res, MF, 75.0, 1%, 1/8W	4067509	1	RN55D7509F	24546
R3	Res, 1.1K, 2%, 1/4W	4130112	1	C4/2%/10	24546
R4	Res, 820, 2%m 1/4W	4130820	4	C4/2%/820	24546
R5	Comp, 33, 5%, 1/8 W	4000330	1	RC05GF330J	81349
R6	Comp, 51, 5%, 1/8 W	4000510	1	RC05GF510J	81349
R7	Comp, 10K, 5%, 1/4 W	4010103	3	RC07GF103J	81349
R8	Met Ox, 8.2K, 2%, 1/4 W	4130822	2	C4/2%/8.2K	81349
R9	Met Ox, 30K, 2%, 1/4 W	4130303	1	C4/2%/30K	24546
R10	Met Ox, 43K, 2%, 1/4 W	4130433	2	C4/2%/43K	24546
R11	Comp, 43K, 5%, 1/4 W	4010433	1	RC07GF433J	81349
R12	Met Ox, S.A.T., Nom, 15K	4130999	4	C4/2%/15K	24546
R13	MF, 12.1, 1%, 1/8W	4061219	1	RN55D1219F	24546

A109 BAND 2 CONVERTER, continued

2020139-05,06 A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R14	Comp, 36, 5%, 1/4 W	4010360	1	RC07GF36J	81349
R15	Comp, 11, 5%, 1/4 W	4010110	2	RC07GF110J	81349
R16	MF, 51.1, 1%, 1/8W	4065119	2	RN55D51R1F	24546
R17	Comp, 1K, 5%, 1/4 W	4010102	4	RC07GF102J	81349
R18	R4				
R19	R15				
R20	Res, CC SAT, 1/4W, 5%	4010999	1		
R21	Comp, 220, 5%, 1/4 W	4010221	2	RC07GF221J	81349
R22	Comp, 20K, 5%, 1/4 W	4010203	1	RC07GF203J	81349
R23	Res, CC 820, 1/4W, 5%	4010821	2	RC07GF821J	
R24	Comp, 10, 5%, 1/8 W	4010100	11	RC07GF100J	81349
R25	Met Ox, 750, 2%, 1/4 W	4130751	2	C4/2%/750	24546
R26	Comp, 11k, 5%, 1/4 W	4010113	3	RC07GF113J	81349
R27	Met Ox, 4.7K, 2%, 1/4 W	4130472	1	C4/2%/4.7K	24546
R28	MF, 33.2,1%, 1/8W	4063329	2	RN55D3329F	24546
R29	Comp, 4.7K, 5%, 1/4 W	4010472	2	RC07GF472J	81349
R30	R26				
R31	Comp, 8.2K, 5%, 1/4 W	4010822	2	RC07GF822J	81349
R32	R7				
R33	R7				
R34	MF, 27.4, 1%, 1/8W	4062749	1	RN55D2749F	24546
R35	MF, 24.3, 1%, 1/8W	4062439	1	RN55D24R3F	24546
R36	R24				
R37	Comp, 10, 5%, 1/8 W	4000100	1	RC05GF100J	81349
R38	R17				
R39	R4				
R40	R4				
R41	R24				
R42	R16				
R43	R24				
R44	Comp, 910, 5%, 1/4 W	4010911	1	RC07GF911J	81349
R45	Comp, 3.9K, 5%, 1/4 W	4010392	3	RC07GF392J	81349
R46	Comp, 27K, 5%, 1/4 W	4010273	1	RC07GF273J	81349
R47	R28				
R48	Comp, 3.3K, 5%, 1/4 W	4010332	1	RC07GF332J	81349
R49	Comp, 390, 5%, 1/4 W	4010391	1	RC07GF391J	81349
R50	Comp, 13K, 5%, 1/4 W	4010133	1	RC07GF133J	81349
R51	MF, 121, 1%, 1/8W	4061210	1	RN55D1210F	24546
R52	R24				
R53	R31				
R54	R26				
R55	R25				
R56	R24				
R57	Met Ox, 4.3K NOM, SAT	4130999	1	C4/2%/4.3K	24546
R58	R17				
R59	R45				
R60	R12 300 or 560 NOM SAT	4130999			
R61	MF, 82.5, 1%, 1/8W	4068259	1	RN55D82R5F	24546
R62	MF, 130, 1%,1/8W	4061300	2	C4/1%/130	24546
R63	Comp, 510, 5%, 1/4 W	4010511	1	RC07GF511J	81349
R64	Comp, 51, 5%, 1/4 W	4010510	2	RC07GF510J	81349
R65	Comp, 200, 5%, 1/4 W	4010201	1	RC07GF201J	81349
R66	Comp, 160K, 5%, 1/4 W	4010164	1	RC07GF160K	81349
R67	Met Ox, 1.8K, 2%, 1/4 W	4130182	1	C4/2%/1.8K	24546
R68	R24				
R69	Met Ox, 510, 2%, 1/4 W	4130511	2	C4/2%/510	24546
R70	Met Ox, S.A.T. Nom 1.2K	4130999	1	C4/2%/1.2K	24546
R71	R29				
R72	R24				

A109 BAND 2 CONVERTER, continued

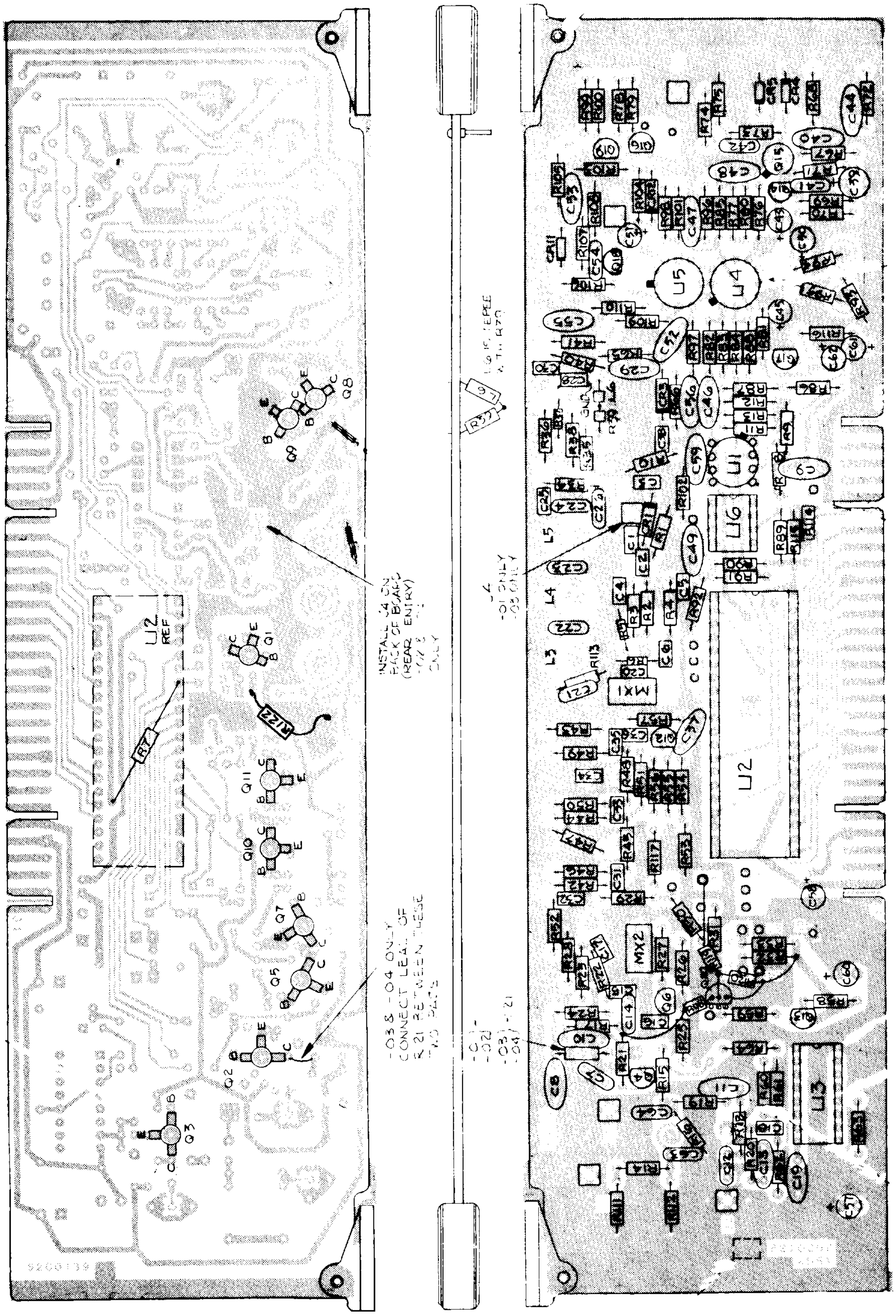
2020139-05,06 A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R73	Comp, 1M, 5%, 1/4 W	4010105	2	RC07GF105J	81349
R74	R64				
R75	R73				
R76	Met Ox, 2.2K, 2%, 1/4 W	4130222	3	C4/2%/2.2K	24546
R77	Met Ox, 3.9K, 2%, 1/4W	4130392	3	C4/2%/3.9K	24546
R78	Comp, 5.6K, 5%, 1/4 W	4010562	1	RC07GF562J	81349
R79	Comp, 3.6K, 5%, 1/4 W	4010362	3	RC07GF362J	81349
R80	Met Ox, 7.5K, 2%, 1/4 W	4130752	3	C4/2%/7.5K	24546
R81	R76				
R82	R24				
R83	Met Ox, 200, 2%, 1/4 W	4130201	3	C4/2%/200	24546
R84	R77				
R85	Met Ox, 330, 2%, 1/4 W	4130331	1	C4/2%/330	24546
R86	Comp, 6.8K, 5%, 1/4 W	4010682	2	RC07GF682J	81349
R87	R79				
R88	R80				
R89	R8				
R90	Comp, 75K, 5%, 1/4 W	4010753	1	RC07GF753J	81349
R91	Met Ox, 33K, 2%, 1/4 W	4130333	1	C4/2%/33K	24546
R92	Met Ox, 160, 2%, 1/4 W	4130161	1	C4/2%/161	24546
R93	R21				
R94	MF, 12.1, NOM, 1%, 1/8 W	4069999	2		
R95	R94				
R96	R83				
R97	R83				
R98	R77				
R99	R86				
R100	R79				
R101	R80				
R102	R10				
R103	R76				
R104	Comp, 180, 5%, 1/4 W	4010181	1	RC07GF181J	81349
R105	R24				
R106	MF, 90.9, 1%, 1/8W	4069099	1	RN55D9099F	24546
R107	R62				
R108	R24				
R109	R69				
R110	R17				
R111	Comp, 160, 5%, 1/4 W	4010161	2	RC07GF161J	81349
R112	R111				
R113	MF, 20, 1%, 1/8W	4062009	1	RN55D2009F	24546
R114	Met Ox, 2K, 2%, 1/4 W	4130202	2	C4/2/2K	24546
R115	R114				
R116	Met Ox, 9.1K, 2%, 1/4 W	4130912	2	C4/2%/9.1K	24546
R117	R116				
R118	Comp, 300Ω, 5%, 1/4 W	4010301	1	RC07GF301J	81349
R119	R45				
R120	R23				
R121	Comp, 68, 5%, 1/4W	4010680	1	RC07GF680J	81349
R122	Comp, 100Ω, 5%, 1/4W	4010101	1	RC07GF100J	81349

A109 BAND 2 CONVERTER, continued

2020139-05, 06 A

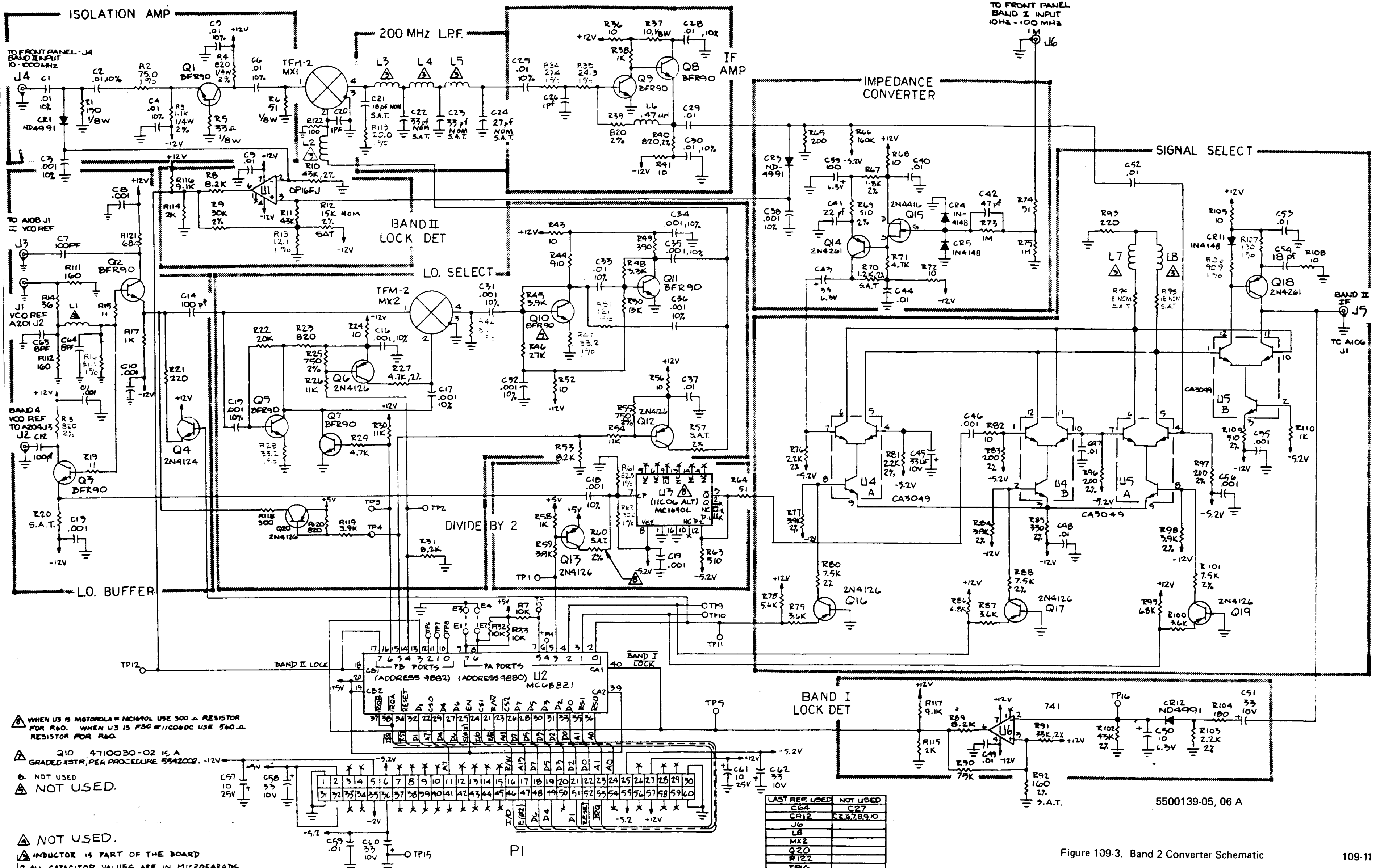
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
T1	Not Used				
TP1 thru TP16	Conn, Pin, .04D	2620032	16	460 - 2970 - 02 - 03	71279
U1	Prec, JFET Op Amplifier	3041016	1	OP16FJ	06665
U2	Periph. Interface Adaptor	3086821	1	MC6821	04713
U3	750 MHz, D-Type Flip Flop	3001106	1	11C06 - Alt. MC1690L	07263
U4	Dual/Diff. Amplifier	3043049	2	CA3049	0000X
U5	U4				
U6	Op Amplifier	3040741	1	LM741CN	0000X



WHEN U3 IS MOTOROLA # MC1690L USE 300 Ω RESISTOR FOR R60. WHEN U3 IS FSC #11C06DC USE 560 Ω RESISTOR FOR R60.

2020139-05, 06 A

Figure 109-2. Band 2 Converter Component Locator



8 WHEN U3 IS MOTOROLA # MC1690L USE 300 Ω RESISTOR FOR R60. WHEN U3 IS FSC #11C06DC USE 560 Ω RESISTOR FOR R60.

7 Q10 4710030-02 IS A GRADED XSTR, PER PROCEDURE 5542002.

6. NOT USED

5 NOT USED.

4 NOT USED.

3 INDUCTOR IS PART OF THE BOARD

2. ALL CAPACITOR VALUES ARE IN MICROFARADS.

1. ALL RESISTORS ARE 1/4W, 5%, RESISTANCE IS EXPRESSED IN OHMS.

NOTES: UNLESS OTHERWISE SPECIFIED.

LAST REF. USED	NOT USED
C64	C27
CR12	C2,6,7,8,9,10
J6	
L8	
MX2	
Q20	
R122	
TP16	
U6	

5500139-05, 06 A

Figure 109-3. Band 2 Converter Schematic

A110
FRONT PANEL
DISPLAY AND KEYBOARD
(2020140)

The Front Panel Display and Keyboard assembly (A110) is divided into two functional sections.

- Numeric display and annunciators
- Keyboard

NUMERIC DISPLAY AND ANNUNCIATORS

This section of the assembly contains twelve common anode 7-segment numeric display units (DS1-DS12), two green LED's (DS37 and DS38), and a maximum of twenty-four yellow LED's (DS13-DS36).

The twelve 7-segment LED's are mounted side by side, with space between each third digit from the right. The corresponding cathode segments of the 7-segment LED's are connected, and the drive signals come from the segment drivers Q3 through Q10. The signals to drive the digits come from the digit drivers located on the Front Panel Logic board (A111).

The twenty-four yellow LED's (DS13-DS36) are divided into three groups of 8 LED's each. The anodes of all LED's in each group are connected. The cathode of each LED in a group are connected to one of the segment drivers (Q3-Q10). With this arrangement each group of annunciator lights can be regarded as similar to one 7-segment LED. The digit drives for the 3 groups of annunciator lights also come from the Front Panel Logic board (A111).

The two green LED's (DS37 and DS38) are driven by Q1 and Q2. When these LED's light they indicate that GATE and CONVERTER SEARCH are in operation.

KEYBOARD

This section of the assembly makes provision for a maximum of twenty-five (single-pole double-throw) switches of which only 21 are used. The switches are arranged in a 4 row by 6 column matrix, with the extra switch taking the row 4 column 7 position. The columns are connected to +5V through the resistor network (RN1) on the Front Panel Logic board (A111).

The keyboard is continuously scanned. The signals scanning the keyboard are derived from A111. To scan the keyboard the 4 rows are grounded sequentially. When a row is grounded, and a key in that row is pushed, one of the columns will be grounded. This information is sent to the A111 board where key debouncing is performed.

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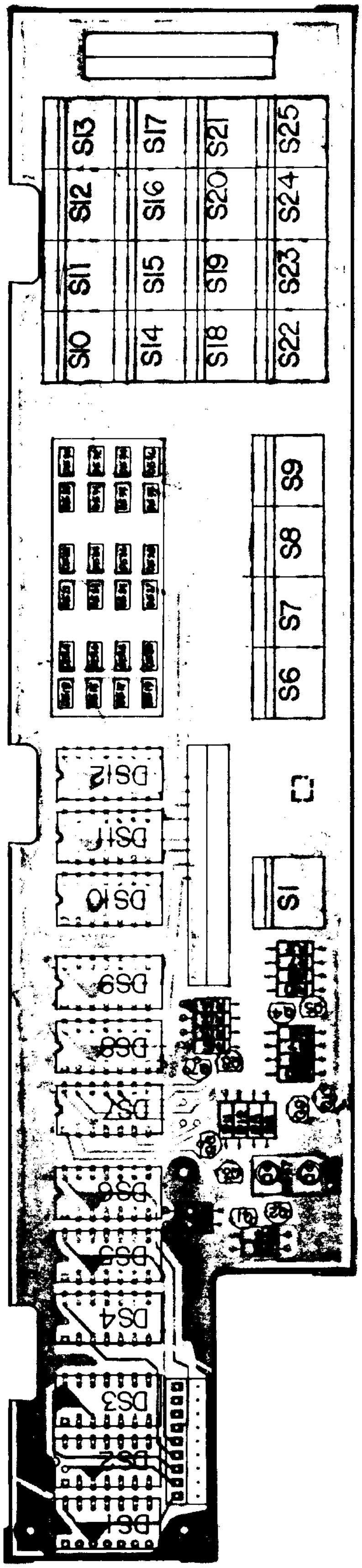
A110 FRONT PANEL DISPLAY AND KEYBOARD

2020140-02 · C

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A110	Front Panel Display & Keyboard	2020140-01	1	EIP	34257
Q1 thru Q10	PNP, RF, Amp.	4710019	10	2N4402	04713
R1	Comp, 4.7K, 5%, 1/4 W	4010472	2	RC07GF472J	81349
R2	Comp, 130, 5%, 1/4 W	4010131	2	RC07GF131J	81349
R3	R1				
R4	R2				
R5	Comp, 240, 5%, 1/4 W	4010241	8	RC07GF241J	81349
R6	Comp, 18, 5%, 1/4 W	4010180	8	RC07GF180J	81349
R7	R5				
R8	R6				
R9	R5				
R10	R6				
R11	R5				
R12	R6				
R13	R5				
R14	R6				
R15	R5				
R16	R6				
R17	R5				
R18	R6				
R19	R5				
R20	R6				
DS1 thru DS12	LED, Numeric, Red	2800024-01	12	TIL-312	01295
DS13 thru DS36	LED, Lamp, Yel	2800020	24	MV57124	50522
DS37	LED, Lamp, Grn	2080018	2	MV5274	50522
DS38	DS37				
S1	Switch, Mon., SPDT	4500013	21	REK	
S2 thru S5	Not Used				
S6 thru S25	S1				
	Spacer, Led Alignment	5100084	1		
P1	9 pin Recept.	2620065	1	22 - 14 - 209	0000A
P2	17 pin Recept.	2620067	1	22 - 14 - 2171	0000A
P3	13 pin Recept.	2620066	1	22 - 14 - 212	0000A



2020140-02-C

Figure 110-1. Front Panel Display and Keyboard Component Locator

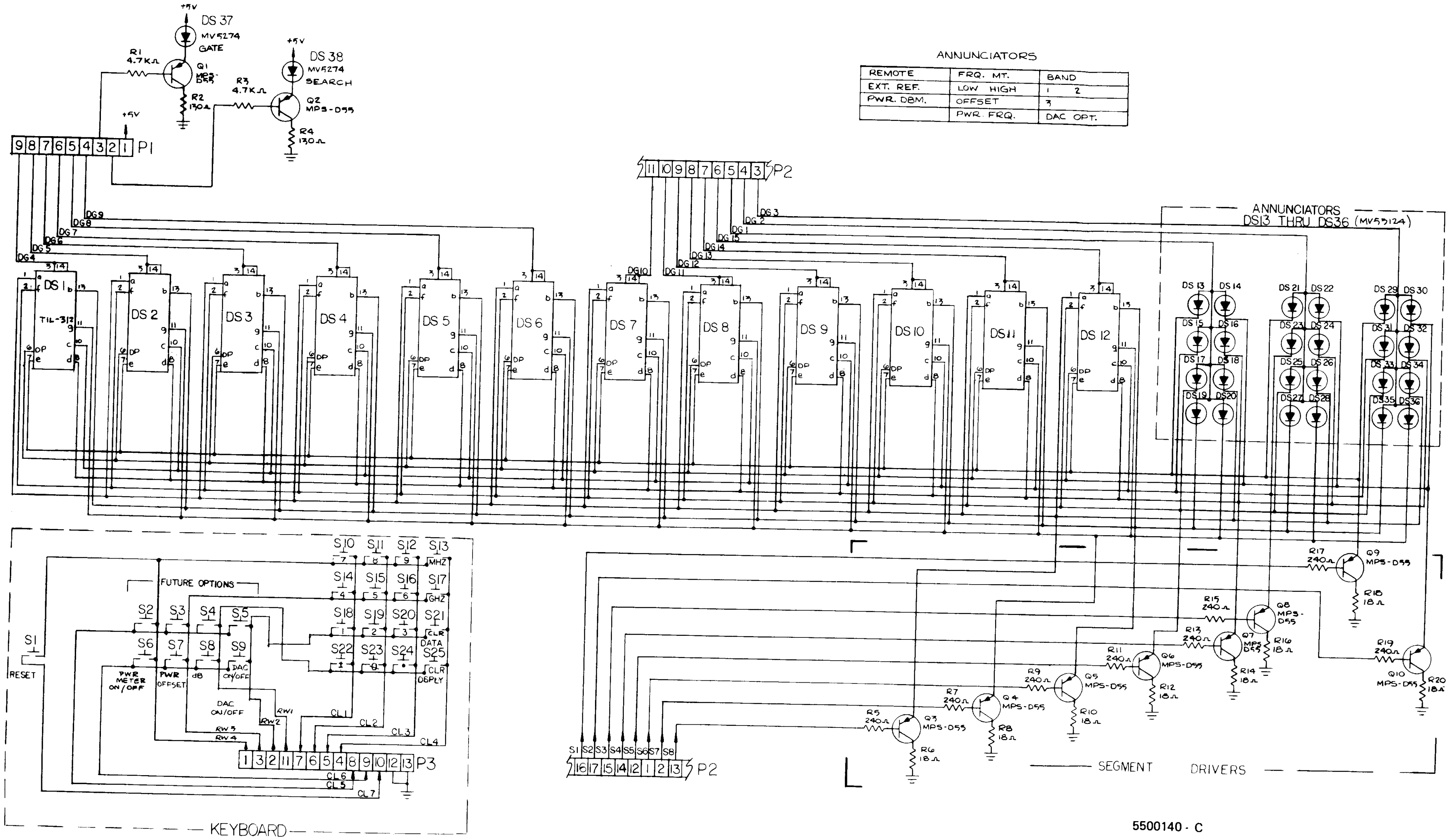


Figure 110-2. Front Panel Display and Keyboard Schematic

A111
FRONT PANEL LOGIC
(2020191)

The Front Panel Logic assembly (A111) contains logic circuitry for control of two functions.

- DISPLAY CONTROL
- KEYBOARD CONTROL

The +5 V power supply to the front panel assemblies (A110 and A111) is regulated by a voltage regulator that is located behind the A111 board. For heatsinking purposes, this voltage regulator is mounted on the chassis. Please refer to figure 111-2, Front Panel Logic block diagram on page 111-3.

DISPLAY CONTROL

The twelve 7-segment LEDs and the three groups of annunciator lights on A110 are multiplexed. To turn on a particular segment in a digit, both the digit driver for that digit and the segment driver for that segment must be on.

The display logic is in constant operation in either the self-scan mode or the memory update mode.

SELF-SCAN MODE

This is the normal operating mode. In this mode the display scan clock is clocking the display counter (U6). The state of the display counter determines which digit will be turned on.

The state of the display counter is decoded by 4 to 16 line multiplexer (U2), and the appropriate digit driver is turned on. At this time the display memory (U7 and U8) is read, and the on/off information (stored in the display memory for that specific digit), turns the segment drivers (A110) on or off.

The display intensity is controlled by varying the duty cycle of the multiplexing. This is done by varying the resistance of the potentiometer (R4) which, in turn, varies the length of time the decoder (U2) and the display memories (U7, U8) are disabled between each scan clock cycle.

At the start of each gate operation the GATE light control is triggered, and the GATE LED lights for the length of the GATE.

MEMORY UPDATE MODE

In this mode the multiplexer logic is disabled by setting the display scan/update control line (PA4) to logic 0. The microprocessor controlled clock (clock, PA1) is used to clock the display counter(U6).

Before updating the display memory (U7 and U8), the display counter is cleared by setting the clear/load control line (PA5) to logic 1, and clocking the clock input of U6. Update mode timing is illustrated in figure 111-1.

KEYBOARD CONTROL

When the keyboard is not being read by the microprocessor, the Keyboard READ/$\overline{\text{SCAN}}$ control line (PA0) is at logic 0. All the outputs of the shift register are at logic 0. If no key on the keyboard is pushed, all the inputs to the 8-input NAND gate (U13) are at logic 1 level. When a key is pushed, the column containing that key will be grounded. The output of U13 goes to logic 1 and C7 (in the debounce circuit) starts to discharge. When the voltage across C7 reaches approximately +0.7 V above ground, the debounce circuit will trigger the interrupt input on the PIA (U11, pin 18) indicating that a key is being pushed.

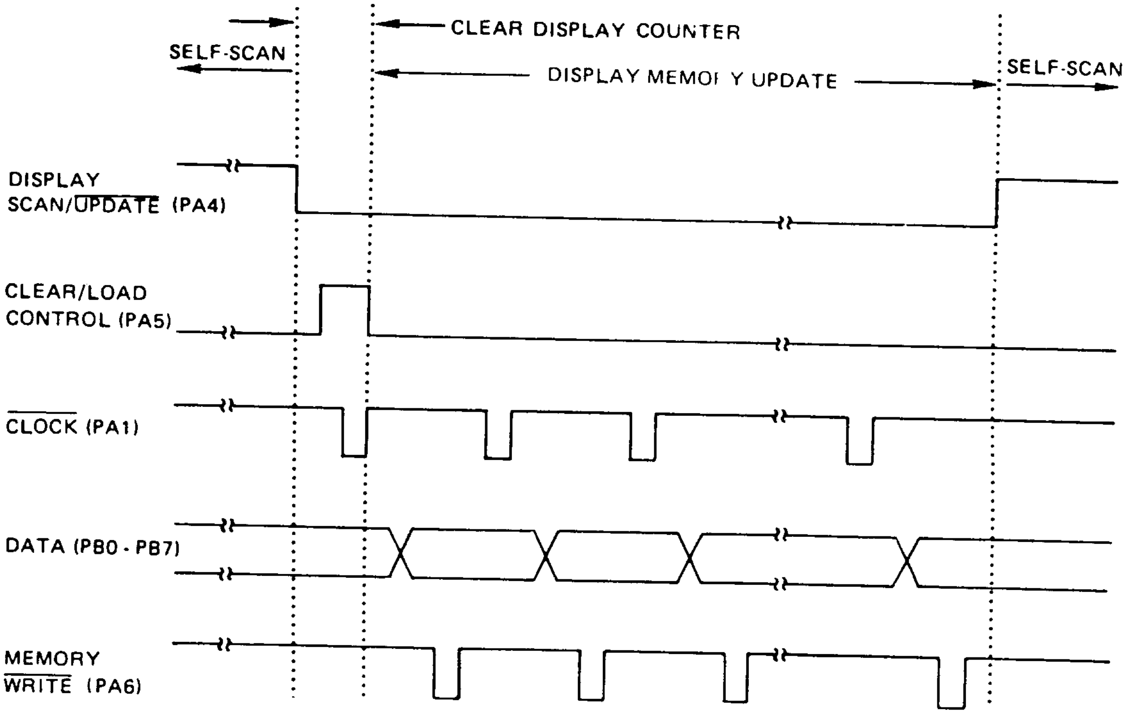


Figure 111-1. Memory Update Mode Sequence

READ KEYBOARD

When the microprocessor needs to read the keyboard, a logic 1 is put on the keyboard READ/$\overline{\text{SCAN}}$ control line (PA0). This enables the data buffer (U9). A 0111 is then loaded into the shift register (U3) by putting a logic 1 on the CLEAR/LOAD control line (PA5) and clocking the clock input of U3. The logic 0 at the output of the shift register (U3) is shifted through the shift register once. The microprocessor reads the keyboard row and column information with the logic 0 at each of the 4 outputs of U3 to determine the coordinate of the key pushed. After the keyboard is read, the keyboard READ/$\overline{\text{SCAN}}$ line is returned to logic 0.

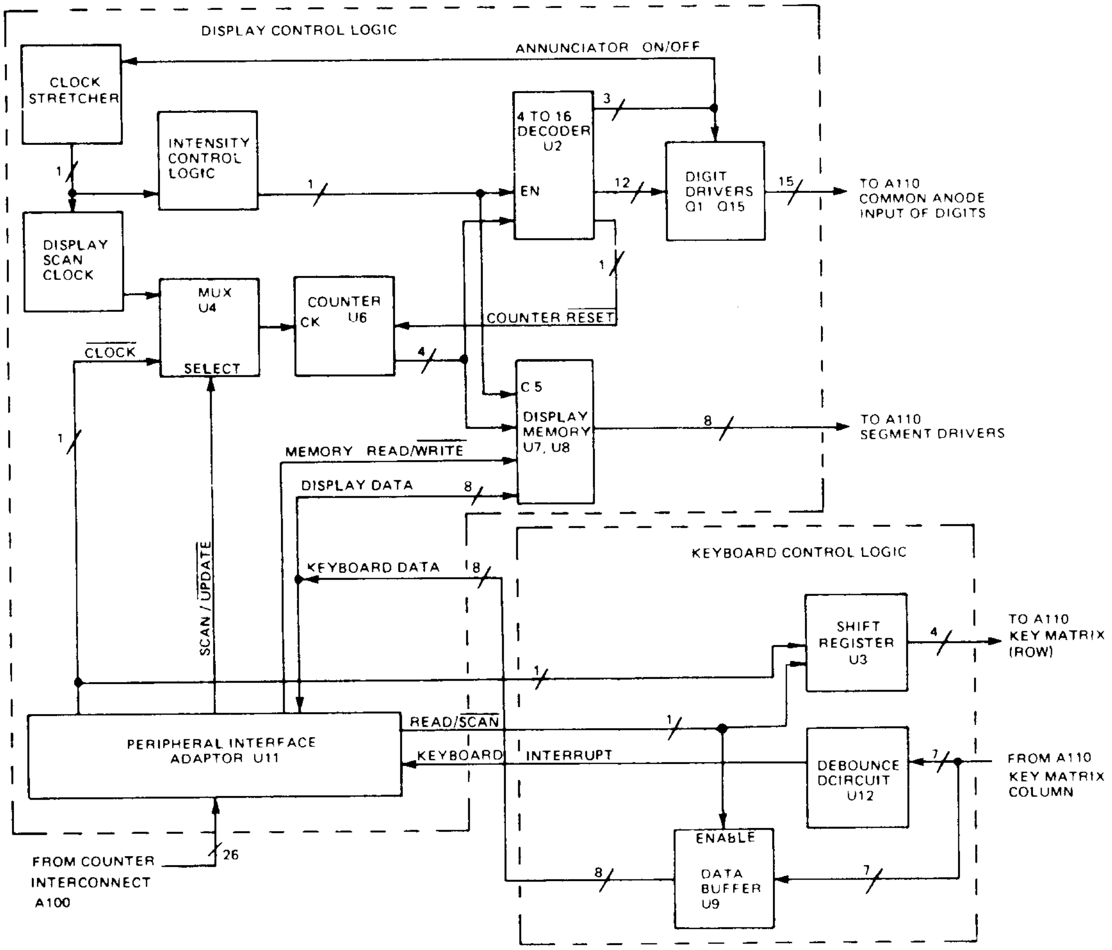


Figure 111-2. Front Panel Logic Block Diagram

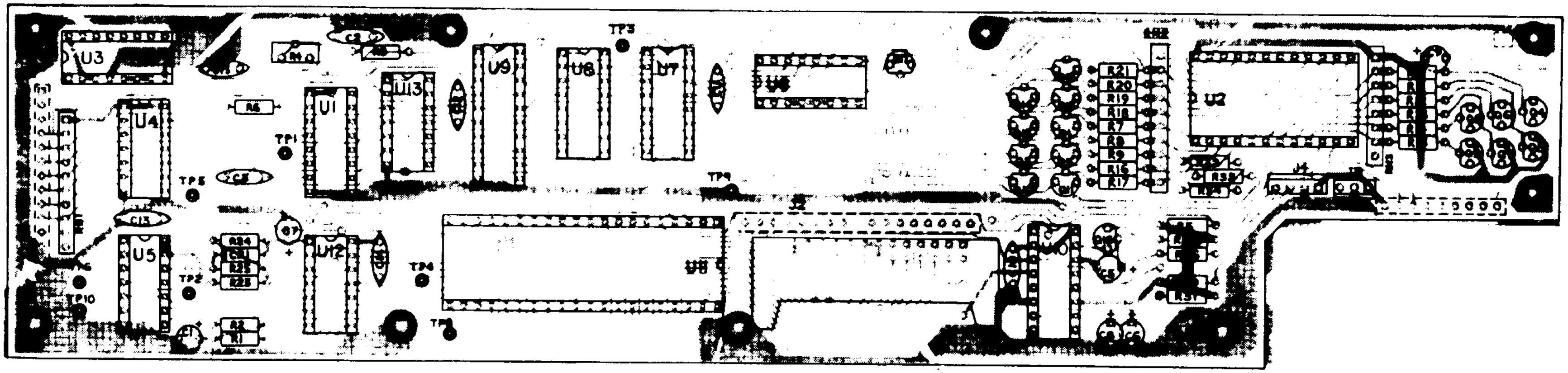
A111 FRONT PANEL DRIVER

2020191-02 A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A111	Front Panel Driver Assy	2020191	1	EIP	34257
C1	Tant, 0.1μF, 10%, 35V	2300020	1	TAPA .10M35	14433
C2	Cer., .002μF, 20%, 1KV	2150005	2	TG - S20	56289
C3	C2				
C4	Not Used				
C5	Tant, 47μF, 20%, 16V	2300025	1	TAPA 47M16	14433
C6	Tant, 2.2μF, 20%, 16V	2300012	1	TAPA 2.2M16	14433
C7	Tant, 22μF, 20%, 16V	2300030	1	TAPA 22M16	14433
C8	Tant, .33μF, 20%, 35V	2300031	1	TAPA .33M16	14433
C9	Tant, 33μF, 20%, 10V	2300015	1	TAPA 33M16	14433
C10 thru C15	Cer., .01μF, 20%, 100V	2150003	6	TG - S10	56289
CR1	Fast Switch	2704148	1	1N4148	07263
J1	9 Pin Male	2620062	1	22 - 03 - 2091	0000B
J2	17 Pin Male	2620064	1	22 - 03 - 2171	0000B
J3	13 Pin Male	2620063	1	22 - 03 - 2131	0000B
J4	4 Pin, FR. LOCK	2620068	1	640456-4	74868
J5	3 Pin	2620121	1	640456-3	74868
P2	26 Pin, Right Angle	2620131	1	3493 - 1002	76381
Q1 thru Q15	PNP, Power	4710027	15	MPS - D54	04713
Q16	NPN, General Purpose	4704124	2	2N4124	04713
Q17	Q16				
R1	Comp, 10K, 5%, 1/4W	4010103	2	RC07GF103J	81349
R2	Comp, 220, 5%, 1/4W	4010221	1	RC07GF221J	81349
R3	Comp, 75K, 5%, 1/4W	4010753	1	RC07GF753J	81349
R4	Variable, Cer., 200K	4250022	1	72XR200	73138
R5	Comp, 120K, 5%, 1/4W	4010124	1	RC07GF124J	81349
R6	Comp, 2.4K, 5%, 1/4W	4010242	1	RC07GF242J	81349
R7 thru R21	Comp, 1K, 5%, 1/4W	4010102	15	RC07GF102J	81349
R22	Not Used				
R23	Comp, 15K, 5%, 1/4W	4010153	1	RC07GF153J	81349
R24	Comp, 390, 5%, 1/4W	4010391	1	RC07GF391J	81349
R25	Comp, 200, 5%, 1/4W	4010201	1	RC07GF201J	81349
R26	Res, 820K, SAT 1;4W, 5%	4010999	1	RC07GF999J	81349
R27	R1				
R28	Not Used				
R29	Comp, 2.2K, 5%, 1/4W	4010222	1	RC07GF222J	81349
R30	Not Used				
R31	Comp, 27K, 5%, 1/4W	4010273	1	RC07GF273J	81349
R32 thru R34	Comp, 39K, 5%, 1/4W	4010393	3	RC07GF393J	81349
RN1	Network, 9 x 10 K	4170003	2	785-1-R10K	32997
RN2	RN1				
RN3	Network, 7 x 10K	4170004	1	784-1-R10K	32997

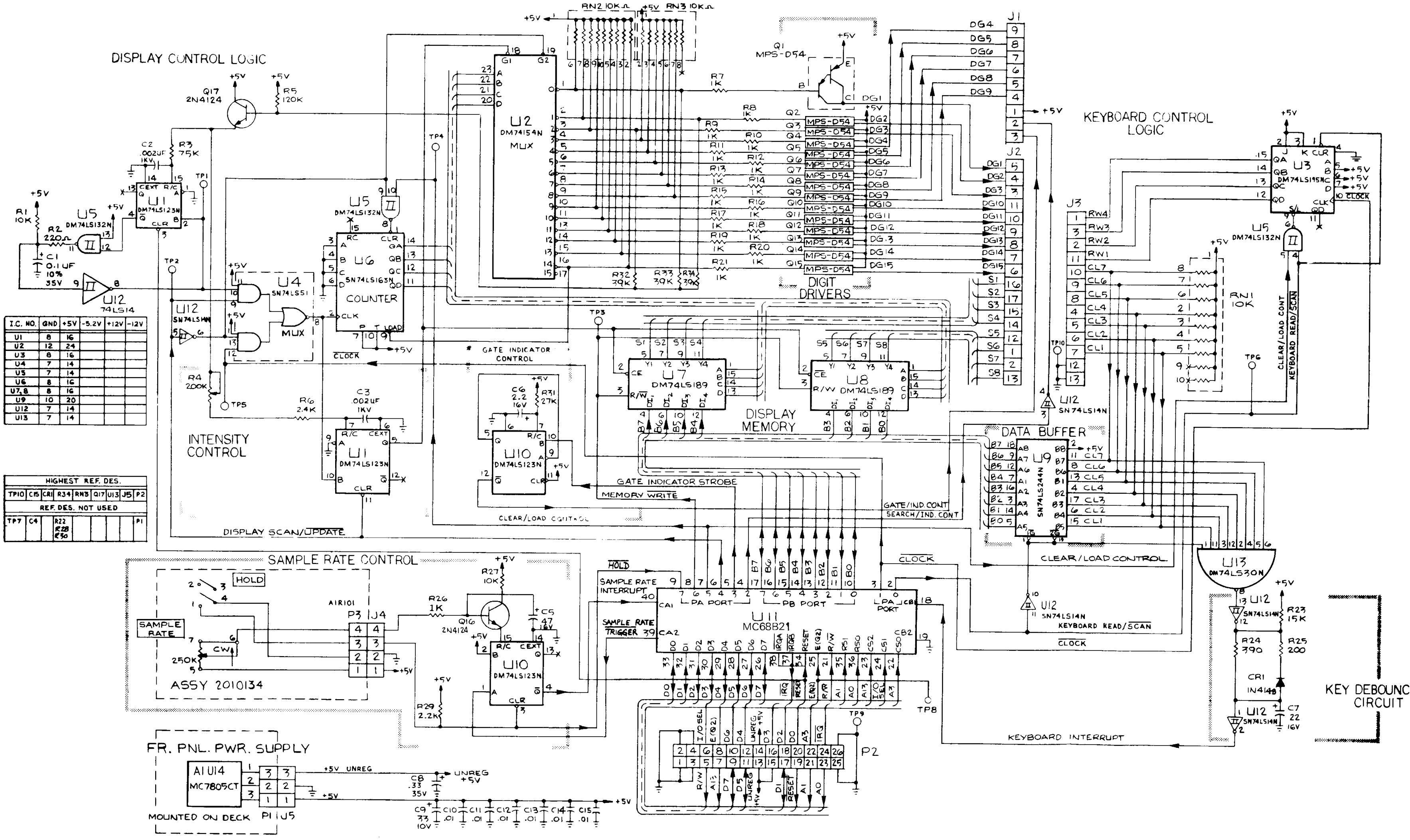
A111 FRONT PANEL DRIVER continued

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
TP1 thru TP6	.040D Pin	2620032	9	460-2970-02-03	71279
TP7	Not Used				
TP8 thru TP10	TP1				
U1	TTL, Monostable, MV	3084123	2	DM74LS123N	0000X
U2	4-16 Line Decoder	3074154	1	DM74154N	0000X
U3	IC,SR, PRL Access, 4-Bit, TI only	3084195	1	DM74LS195N	0000X
U4	AND - OR - INVERT Gates	3087451	1	SN74LS51N	01295
U5	Quad, 2 INP NAND Gate	3084132	1	DM74LS132N	0000X
U6	Binary Sync Clear	3084163	1	SN74LS163	01295
U7	Bipolar RAMS	3057489	2	DM74LS189	0000X
U8	U7				
U9	Oct Bus Trans	3084244	1	SN74LS244N	01295
U10	U1				
U11	Periph, Interface Adaptor	3086821	1	MC68B21P	04713
U12	Hex Inverter	3087414	1	SN74LS14N	01295
U13	8INP NAND Gates	3087430	1	DM74LS30N	0000X
U14	Pos. Voltage Regulator (reference only - U14 part of front panel power supply)	3057805	1	MC7805CT	04713



2020191 -02 A

Figure 111-3. Front Panel Component Locator



I.C. NO.	GND	+5V	-5.2V	+12V	-12V
U1	8	16			
U2	12	24			
U3	8	16			
U4	7	14			
U5	7	14			
U6	8	16			
U7,8	8	16			
U9	10	20			
U12	7	14			
U13	7	14			

HIGHEST REF. DES.								
TP10	C15	CR1	R34	RN3	Q17	U13	J5	P2
REF. DES. NOT USED								
TP7	C4		R22 R28 R30					P1

5500191-02 A

Figure 111-4. Front Panel Logic Schematic

A203
BAND 3 MICROWAVE CONVERTER

The A203 Microwave Converter consists of three functional sections:

Voltage Control Oscillator

IF Amplifier

Microwave (YIG)

CAUTION

Disassembly of the A203 Microwave Converter
will void the EIP warranty.

The assembly drawing and schematic for both the VCO and IF circuits are not available. The entire A203 assembly must be tested as a complete unit to ensure proper performance of the counter. Repair of the Microwave (YIG) module can only be done at the factory. The VCO and IF Amplifier boards require special test equipment, therefore field repair is not recommended.

The Band 3 Converter is a complete microwave subsystem (see Figure 203-1) which converts an input signal in the 1 to 20 (26.5) GHz range down to an IF of 127 MHz. Down conversion is achieved in this heterodyne system by combining the input signal with a harmonic of a precisely known reference signal (F_{VCO}). The mixer then produces a signal (F_{IF}) equal to the difference between the input and reference harmonic. If this difference is close to 127 MHz, it is amplified to a level of about 0 dBm and then counted. The input signal is then determined from the equation $F_{IN} = NF_{VCO} + F_{IF}$. F_{VCO} is set by the instrument program via a phase locked loop located on the converter control board (A108) and is thus known exactly. harmonics of the VCO are produced by the comb generator and coupled to the mixer. The frequency ranges of the VCO and IF are such that for any VCO frequency and any input frequency, only one harmonic can produce an IF frequency. The YIG filter located between the RF input and the mixer is used to approximately determine the input frequency and from this information the desired values of N, F_{VCO} and +/- are determined.

Two other outputs are obtained from the Band 3 Converter. The first is an analog signal which is a measure of input RF power. The second is a digital signal ($\overline{\text{IF THRESHOLD}}$) which indicates that an IF signal exists at a level of -3 dBm or greater.

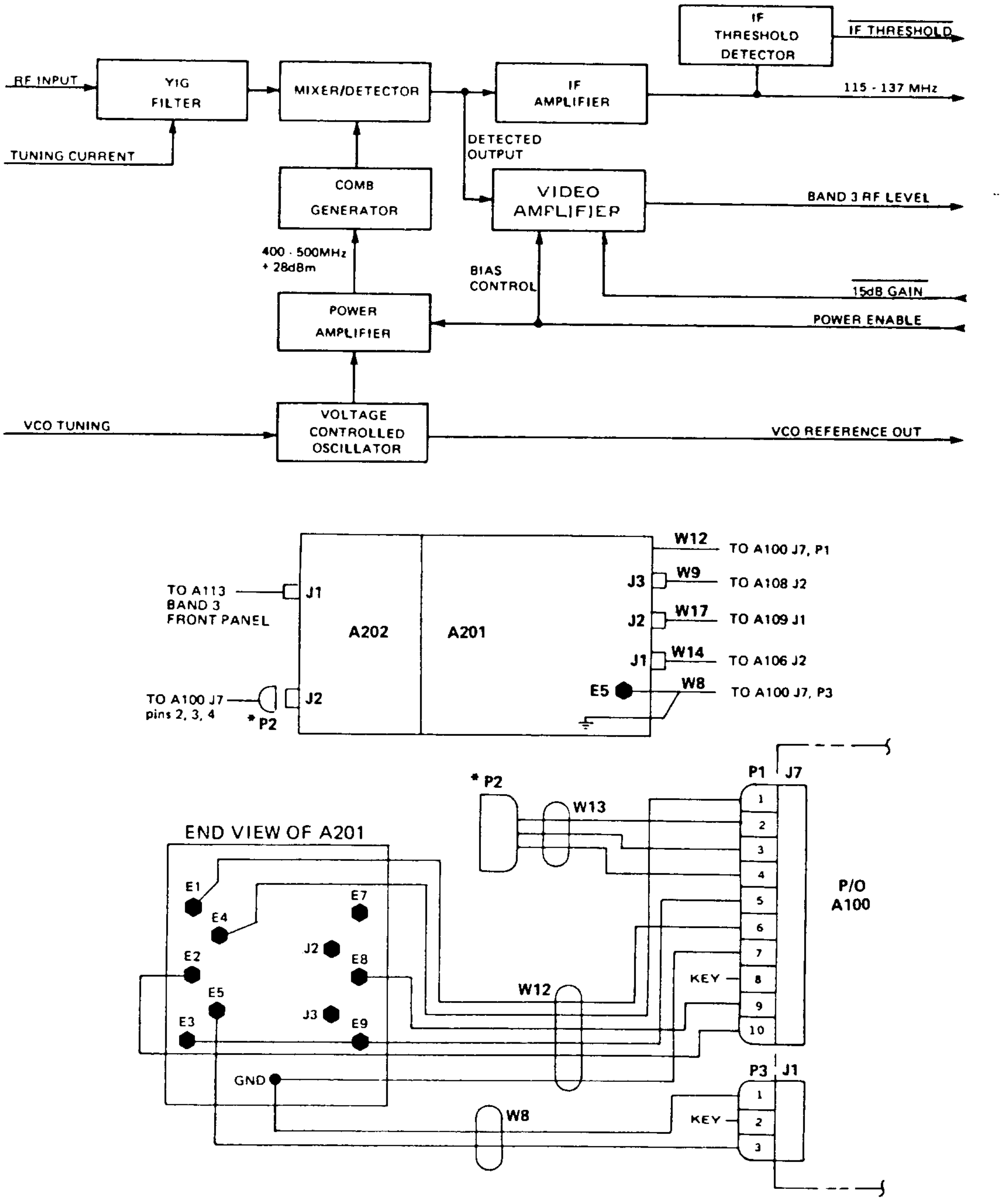


Figure 203-1. Band 3 Microwave Converter Diagram

Section 10
Options

Section 10 provides descriptions, specifications (where applicable), schematic diagrams and component locators for the options available for use with the Model 575B or 578B counter.

OPTION

01 D TO A CONVERTER

DAC will convert any three consecutively displayed digits into an analog voltage output on rear panel.

02 POWER MEASUREMENT

1 to 20/26.5 will measure sine wave amplitude to 0.1 dBm resolution and display simultaneously with frequency.

Power offset to 0.1 dB resolution, selectable from front panel.
Option will not degrade the basic performance of the counter.

03 TIME BASE OSCILLATOR $<5 \times 10^{-9}$ (2010143-03)

04 TIME BASE OSCILLATOR $<1 \times 10^{-9}$ (2010143-04)

05 TIME BASE OSCILLATOR $<5 \times 10^{-10}$ (2010143-05)

06 EXTENDED FREQUENCY CAPABILITY - 578B

Use in conjunction with model 590 Frequency Extension Cable Kit and optional Remote Sensors models 91 thru 94.

07 NOT USED

08 NOT USED

09 REAR PANEL INPUT

10 CHASSIS SLIDES

13 MATE-CIIL INTERFACE

OPTION 01
DIGITAL TO ANALOG CONVERTER

Option 01 will convert three consecutive digits to an analog voltage, available on the rear panel. The output will reflect the display, substituting zeros for any non-numeric characters that appear. The output will be updated after every display update.

SPECIFICATIONS

Output Voltage	0.000 volts to 0.999 volts
Accuracy (25° C)	± 0.5 % ±1 mV
Temp. Stability (0-50° C)	± 0.01 % / °C
Resolution	1 mV
Load Impedance	1 K ohm minimum
Connector	BNC female (on rear panel)
Protection	± 10 V AC or DC applied to output connector will not cause damage. No damage will occur by any load.

OPERATION

On power up the DAC is in off state.

KEYBOARD OPERATION

A three key sequence selects the location of the most significant digit in the three digits desired. Digits are numbered 01 through 12.

PRESS : $\overset{\text{DAC}}{\boxed{}}$ $\boxed{\text{X}}$ $\boxed{\text{X}}$ XX can vary from 01 to 12.

EXAMPLES : $\overset{\text{DAC}}{\boxed{}}$ $\boxed{0}$ $\boxed{1}$ 1 Hz digit selected

$\overset{\text{DAC}}{\boxed{}}$ $\boxed{0}$ $\boxed{2}$ 10 Hz, 1 Hz digits selected

$\overset{\text{DAC}}{\boxed{}}$ $\boxed{0}$ $\boxed{3}$ 100 Hz, 10 Hz, 1 Hz digits

$\overset{\text{DAC}}{\boxed{}}$ $\boxed{0}$ $\boxed{4}$ 1 kHz, 100 Hz, 10 Hz digits

•
•
•

$\overset{\text{DAC}}{\boxed{}}$ $\boxed{1}$ $\boxed{2}$ 100 GHz, 10 GHz, 1 GHz digits

After pressing $\overset{\text{DAC}}{\boxed{}}$, the display will show the present DAC status, such as DAC OFF or DAC XX. Three decimal points will show the locations of the currently selected digits (if DAC is on).

After pressing the first $\boxed{X}$, the display will show the temporary entry e.g., DAC X, but the three decimal points will still show the previous DAC status.

After pressing the second $\boxed{X}$, the display will show the new entry, e.g., DAC X X. The three decimal points will move to the newly selected locations. The DAC output will be updated accordingly. Release of the last key pressed will return the display to display measurements.

Any illegal key strokes will result in displaying ERROR 10. The operator must restart the key sequence to enter the correct data.

To clear display of DAC data, ERROR display, or an unfinished key sequence, press **CLEAR** $\boxed{}$ **DISPLAY**. Display to return to display measurements, and DAC status will not be changed.

To turn off DAC option Press: **DAC** $\boxed{}$ **DATA** $\boxed{}$ **CLEAR** OR **DAC** $\boxed{}$ $\boxed{0}$ $\boxed{0}$

GPIB OPERATION

To enable the DAC option through GPIB, input DC followed by two decimal digits. The two digits correspond to the location of the most significant digit in the three digits desired. To turn the DAC option off, input DC00 or DCP.

DC00 – turns DAC option off
DC01 – selects 1 Hz digit
thru
DC12 – selects 100, 10 and 1 GHz digits.

THEORY OF OPERATION

A simplified block diagram of the DAC portion of the A103 board is shown in Figure 01-1.

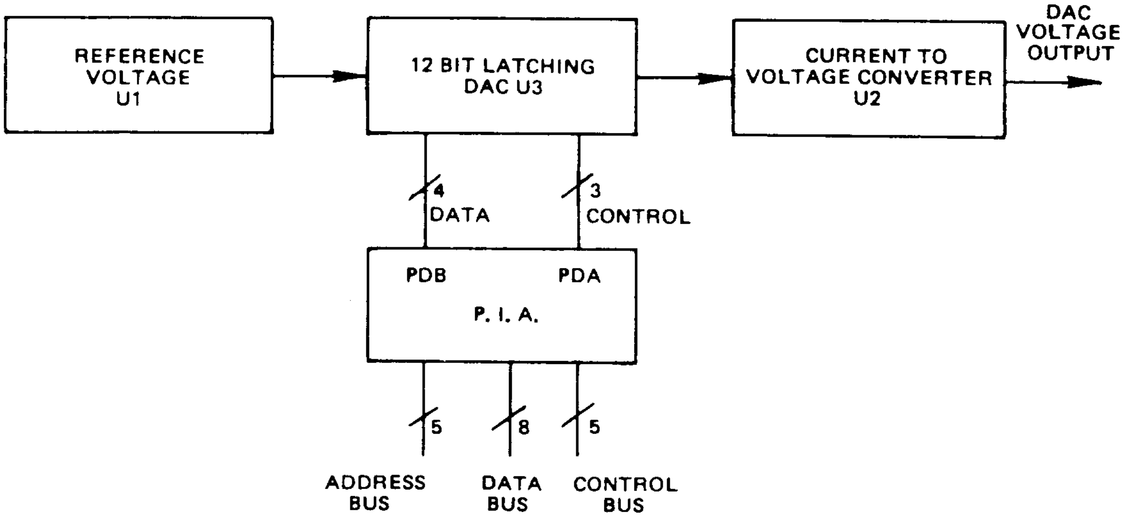


Figure 01-1. DAC Option, Simplified

HARDWARE

The DAC is referenced to a 1 volt reference voltage generated by U1. A gain adjustment, R5, is provided to calibrate the reference to 1 volt. U3 consists of a 12 bit multiplying DAC, three individual four bit registers, and address decoding. The digital data is written to the DAC four bits at a time and stored in the appropriate registers. The data is then transferred simultaneously to the DAC and in conjunction with U2 converts the digital data to an analog voltage corresponding to the three digits selected on the front panel. When the DAC option exists, U12 Pin 5 has to be grounded.

SOFTWARE

The DAC software is described in Figures 01-2 and 01-3.

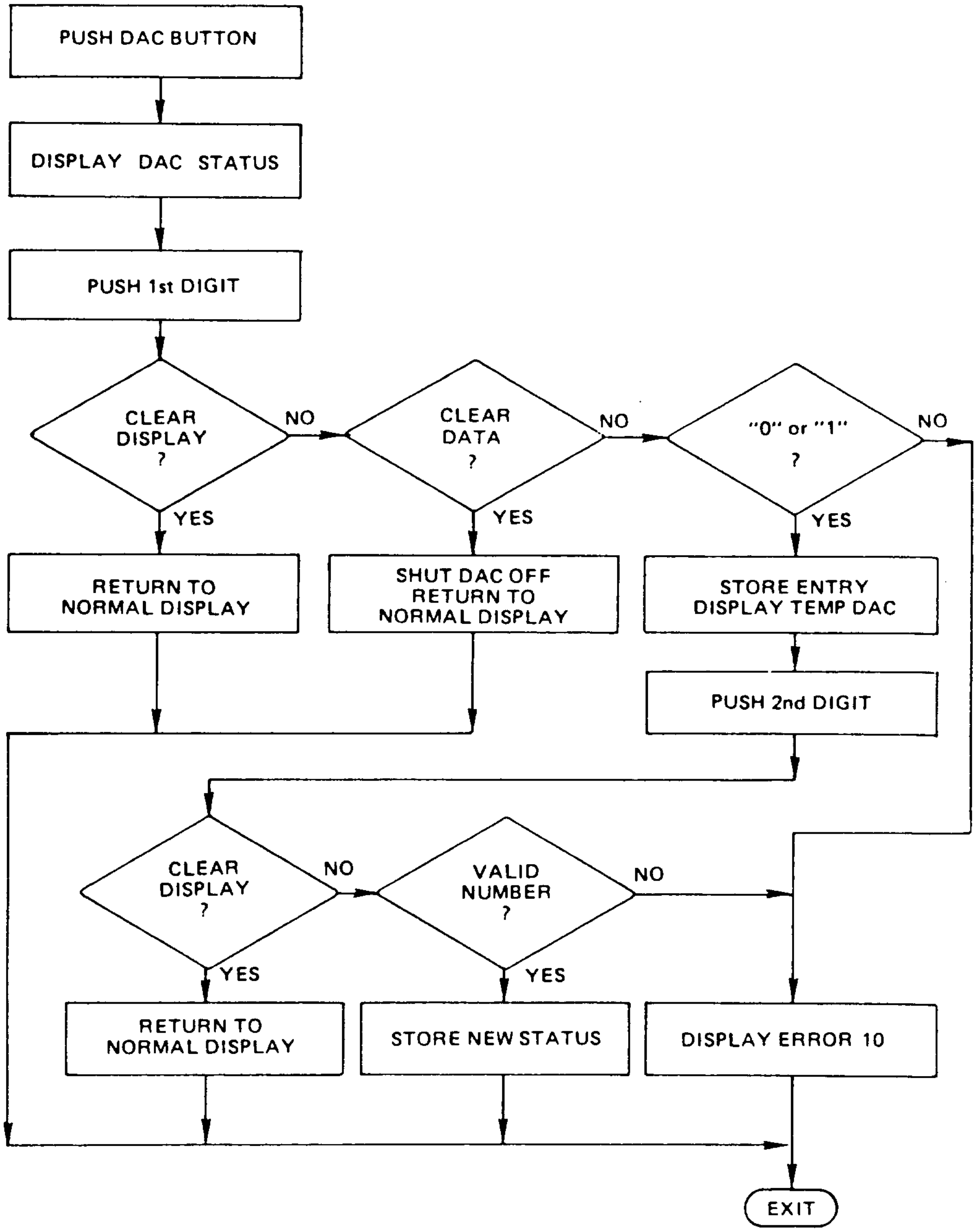


Figure 01-2. Keyboard Control

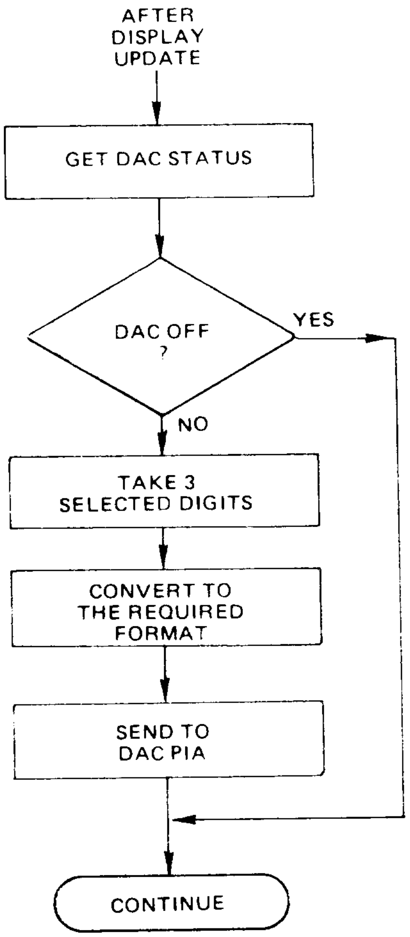


Figure 01-3. DAC Board Update

CALIBRATION

The following instruments or their equivalents are required to perform calibration of the DAC board. Calibration is required every six months or after the board has been repaired.

BRAND	MODEL	TYPE	SPECIFICATIONS
Fluke	8050A	DVM	4½ digit resolution

FULL SCALE CALIBRATION

1. Enter: DAC 0 3 FREQ OFFSET 9 9 9
2. Connect the DVM to the DAC output on the rear panel.
3. Adjust R5 until the DVM reads .9990 Volts.

The calibration for the DAC board is complete.

PERFORMANCE TESTS

1. Enter: DAC 0 3 FREQ OFFSET

   The DAC output should be .000 V.

2. Enter: 9 9 9

   The DAC output should be .999 V.

3. Enter: DAC 5 5 5

   The DAC output should be .500 V.

   ENTER: TEST 2 1

   A continuous count ramp from 000 to 999 is sent to the DAC board, regardless of DAC status or display.

   Connect the DAC output to an oscilloscope. A ramp should be observed going from 0 to .999 volts. The ramp is built with 1 mV amplitude steps. Any failure in one or more of the digital lines on the board will cause either breaking in the ramp or multiple amplitude steps (2 mV, 4 mV).

   During this test signature analysis can be used to determine if the DAC (A103U3) is receiving the correct digital information. Figure 01-4 contains the trigger points and the correct signatures for all of the digital lines to the DAC (A103U3).

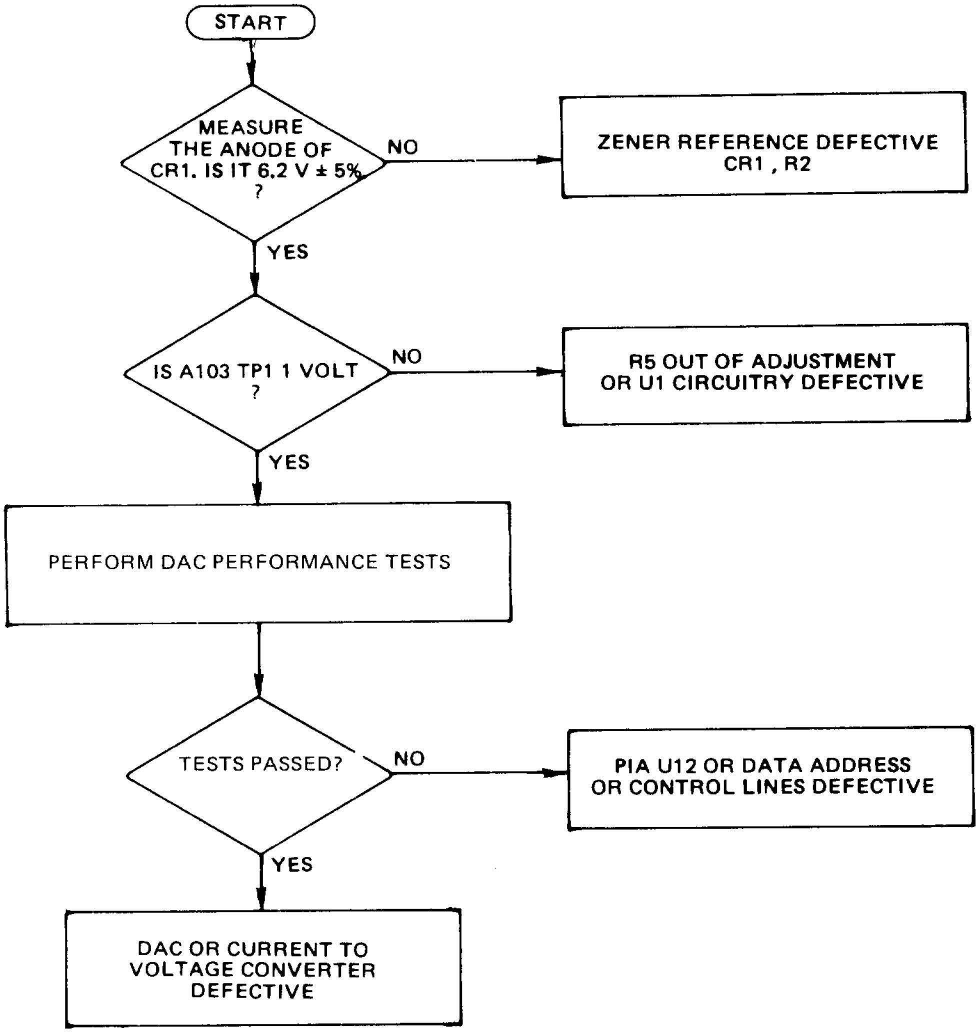


Figure 01-4. DAC Troubleshooting Tree

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OPTION 01 – REFERENCE LOOP/DAC

2020201-03 A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A103	Ref. Loop/Digital to Analog Converter	2020201-02	1	EIP	34527
C1	Cer, .01µF, 20%, 100V	2150003	14	TG-S10	56289
C2	Mica, 33pF, 5%, 500V	2260021	1	CD10ED330J03	72136
C3	Mica, 100pF, 5%, 500V	2260034	1	CD10ED101J03	72136
C4	Tant, 33µF, 10%, 10V	2300015-00	4	TAPA 33M10	14433
C5 thru C12	C1				
C13	Tant, 10µF, 20%, 25V	2300029	4	DF106M25S	72136
C14	C13				
C15	C1				
C16	C1				
C17	C4				
C18	C4				
C19	C1				
C20	C1				
C21	Tant, 1µF, 10%, 35V	2300008	1	TAPA 1.0M35	14433
C22	Cer, .047µF, 10%, 50V	2150090	2	5020EM50RD473K	EMCAP
C23	Met Film, .47µF, 10%, 63V	2350010	1	MKT-1819-447-06	0000B
C24	C22				
C25	C4				
C26	Cer, .001µF, 20%, 100V	2150001	2	5GA-D10	56289
C27	Tant, 100µF, 20%, 10V	2300039-00	1	TAPA100M10	14433
C28	C13				
C29	C1				
C30	C13				
C31	C26				
C32	Cap, Mica 47pF, 500V	226004-00	1		
CR1	Zener, 6.2V	2700827	1	IN827	
CR2	Dual, Low Leak	2710013-00	1	IDI00	32293
CR3	General Purpose	2704148-00	3	IN4148	07263
CR4	Varactor	2710025	1	MV1404	04713
CR5	CR3				
CR6	CR3				
CR7	Zener, 5.1V	2705231-00	1	IN5231	04713
L1	Not Used				
L2	Inductor, .18µH	3150013	1	DD-0.18	72259
R1	Met Film, 39.2K, 1%, 1/4W	4053922	1	RN55C3922F	81349
R2	Comp, 750, 5%, 1/4W	4010751	2	RC07GF751J	81349
R3	Met Film, 6.19K, 1%, 1/4W	4056191	1	RN55C619F	81349
R4	Comp, 1K, 5%, 1/4W	4010102	3	RC07GF102J	81349
R5	Variable, 500 ohm, 10 Turn	4280009	1	89PR500	73138
R6	Comp, 10K, 5%, 1/4W	4010103	2	RC07GF103J	81349
R7	Comp, 510 ohm, 5%, 1/4W	4010511	8	RC07GF511J	81349
R8	Comp, 4.7K, 5%, 1/4W	4010479-00	2	RC07GF479J	81349
R9	R4				
R10	Comp, 4.3K, 5%, 1/4W	4010432	1	RC07GF432J	81349
R11	R7				
R12	Comp, 220K, 5%, 1/4W	4010224	1	RC07GF224J	81349
R13 thru R16	R7				
R17	Comp, 1.5M, 5%, 1/4W	4010155	1	RC07GF155J	81349
R18	R8				
R19	Comp, 1.2K, 5%, 1/4W	4010122	1	RC07GF122J	81349
R20	R2				
R21	R7				
R22	R7				
R23	Comp, 150 ohm, 5%, 1/2W	4020151-00	1	RC07GF151J	81349

OPTION 01 – REFERENCE LOOP/DAC

2020201-03 A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MPG NO.	TYP FSCM NO.
R24	Comp, 100 ohm, 5%, 1/4W	4010101	2	RC07GF101J	81349
R25	Met Ox, 2.4K, 2%, 1/4W	4130242	1	C4/2%/2.4K	24546
R26	R24				
R27	R4				
R28	Met Ox, 2K, 2%, 1/4W	4130202	1	C4/2%/2K	24546
R29	R6				
U1	Op Amplifier	3040741	1	LM741CN	0000X
U2	Op Amplifier/Buffer	3040308	1	LM308AN	0000X
U3	12 Bit Latching DAC	3057542	1	AD7542JN	AD
U4	8 Bit Latch	3034373	2	74C373	27014
U5	U4				
U6	UP/DOWN Counter	3084192	4	DM74LS192	27014
U7 thru U9	U6				
U10	2-Modulous Prescaler	3112013-02	1	MC12013	04731
U11	Counter Control	3112014	1	MC12014	04731
U12	P.I.A.	3086821	1	MC6821P	04731
U13	Dual Flip flop	3087474	1	DM74LS74	27014
U14	Phase Frequency/DET	3014044	1	MC4044L	04731
U15	Quad NAND, 2 INP	3087400	1	DM74LS00	27014
U16	Dual "D" Flip flop	3110131	1	MC10131L	04731
U17	Dual Decade Counter	3084490	1	SN74LS490N	01295
U18	Quad NOR, 2 INP	3110102	1	MC10102P	04731
U19	Op Amplifier, J-FET	3040071	1	TL071CP	01295
U20	Oscillator	3011648	1	MC1648P	04731
TP1 thru TP8	.040D Pin, Gold	2620032	8	460-2970-02-03	71279

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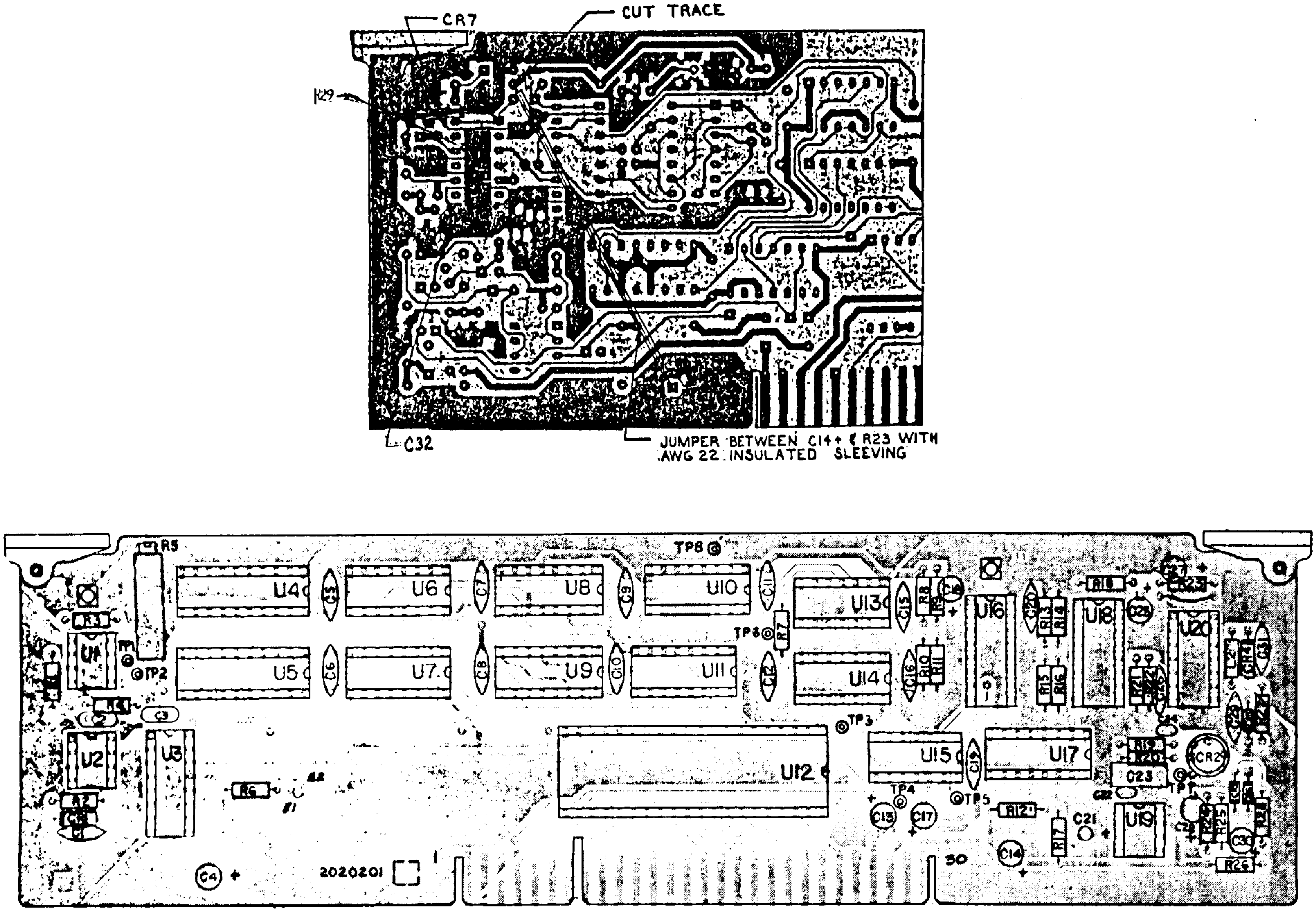
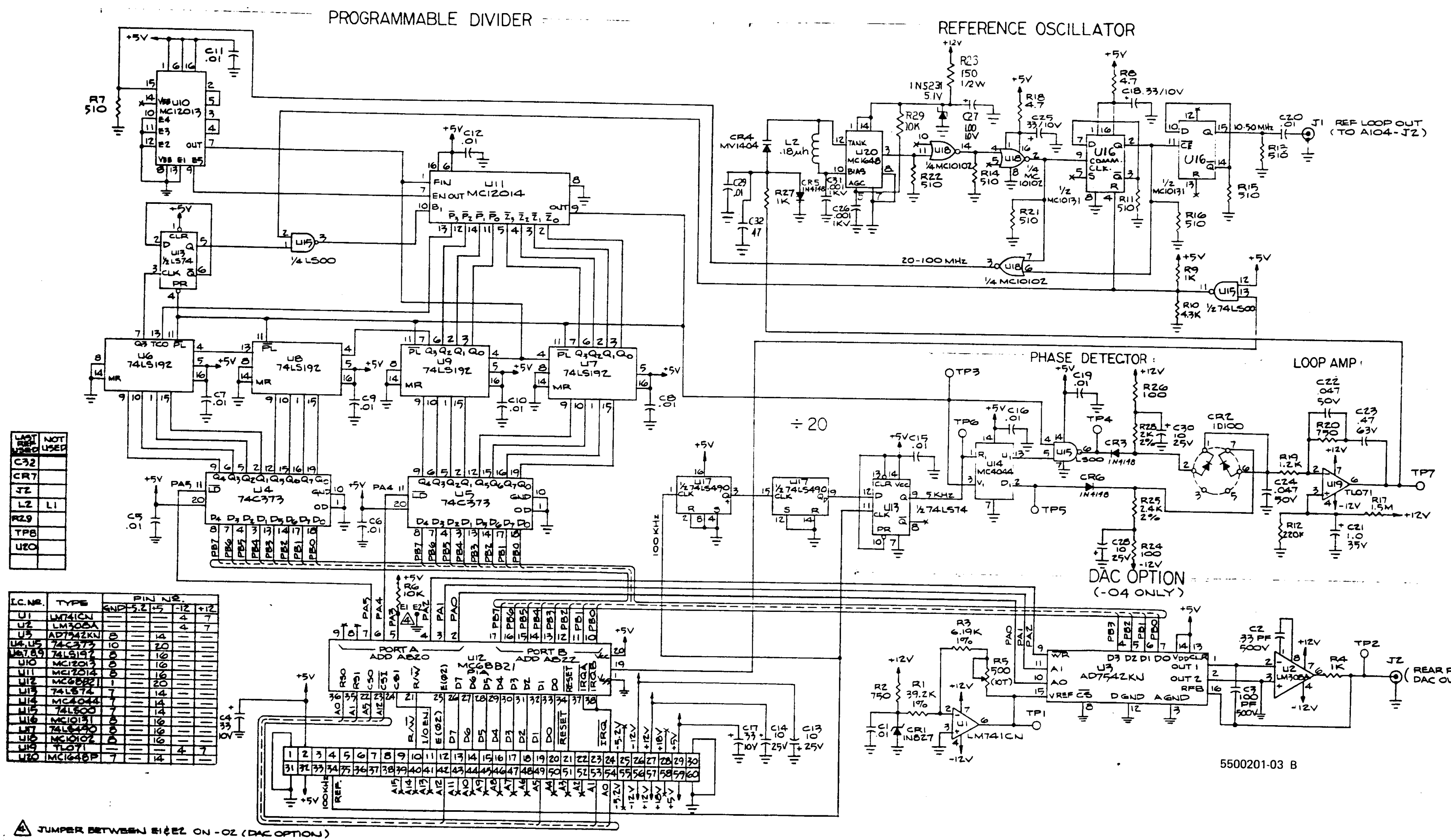


2020201-03 A

Figure 103-3. DAC / Reference Loop Component Locator

NOTE: C1 THRU C3, CR1, J2, R1 THRU R5, AND U1 THRU U3 ARE NOT USED ON -01.



LAST REF USED	NOT USED
C32	
CR7	
J2	
L2	L1
R29	
TP8	
U20	

I.C. NO.	TYPE	PIN NO.				
		GND	-5.2	+5	-12	+12
U1	LM741CN	—	—	—	4	7
U2	LM308A	—	—	—	4	7
U3	AD7542KN	8	—	14	—	—
U4, U5	74C373	10	—	20	—	—
U6,7,8,9	74LS192	8	—	16	—	—
U10	MC12013	8	—	16	—	—
U11	MC12014	8	—	16	—	—
U12	MC6821	1	—	20	—	—
U13	74LS74	7	—	14	—	—
U14	MC4044	7	—	14	—	—
U15	74LS00	7	—	14	—	—
U16	MC10131	8	—	16	—	—
U17	74LS490	8	—	16	—	—
U18	MC10102	8	—	16	—	—
U19	TL071	—	—	—	4	7
U20	MC1648P	7	—	14	—	—

5500201-03 B

4. JUMPER BETWEEN E1 & E2 ON -02 (DAC OPTION)

3. NOT USED.

2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
ALL .01 UF CAPACITORS ARE 100V.

1. ALL RESISTORS ARE 1/4 W, 5%, AND ARE EXPRESSED IN OHMS.

NOTES: UNLESS OTHERWISE SPECIFIED.

Figure 01-7. Reference Loop / DAC Schematic

OPTION 02
POWER MEASUREMENT

Option 02 measures the power of signals applied to Band 3. The power is displayed (to 0.1 dB resolution) simultaneously with frequency (to 100 kHz max. resolution). For A.M. and F.M. averaging purposes, gate time is controllable in the power meter mode, through the resolution function. Power gate time mirrors frequency gate time. For example, in resolution 0 the frequency gate time is 1 second, and the power gate time is 1 second. In resolution 1 the frequency gate time is 100 msec., and the power gate time is 100 msec. Option 02 allows power offsets from -99.9 dB to 99.9 dB, with a 0.1 dB resolution and will not degrade the basic performance of the counter.

SPECIFICATIONS

ACCURACY	± 1.2 dB Typical 0-50° C ± 0.5 dB Typical 25° C
TIME ADDED	1 GATE TIME + 50 msec.
RESOLUTION	0.1 dB POWER sensitivity to -10 dbm; 0.2 dbm -10 dbm to OVERLOAD Selectable 100kHz - 1 GHz Frequency
RANGE	ENTIRE OPERATING RANGE OF BAND 3

KEYBOARD OPERATION

To turn the power meter ON or OFF PRESS: **POWER METER ON/OFF** ☐

If the POWER METER option is off, pushing the POWER METER ON/OFF key will turn the POWER METER on. Pushing that key again will turn the POWER METER off. If the counter is displaying only frequency it will begin displaying frequency and power. If the counter is displaying frequency and power it will begin displaying frequency only.

Turn the power meter on. Observe the display. Frequency is displayed on the left, and power is displayed on the right. The dBm annunciator lights to indicate power meter operation. If the signal is too small to measure the power, the display will show EE.E in the power meter digits. (Since 0 dBm is a valid power, 00.0 cannot be used as a no power indicator.)

When the POWER METER option is on, the frequency measurements displayed on the front panel are to a maximum resolution of 100 kHz. The last selected gate time will be retained.

Power meter offset function enables the entry of a positive or negative power offset to 0.1 dB resolution. The offset will be incorporated into the power measurement after the next gate.

TO INPUT POWER OFFSETS

PRESS: **POWER METER OFFSET** ☐ Notice flashing annunciator and power offset last entered.

PRESS: [#] Number keys corresponding to desired power offset.

PRESS: **dB** ☐ To terminate input sequence. Notice OFFSET PWR annunciator solidly lit after terminator key is released.

TO RECALL STORED OFFSETS

PRESS: POWER METER OFFSEET ☐ Stored offset is displayed.

PRESS: CLEAR ☐ DISPLAY Returns counter to display measurements.

TO REMOVE POWER OFFSETS

PRESS: POWER METER OFFSEET ☐ DATA ☐ CLEAR OR POWER METER OFFSEET ☐ [0] dB ☐ OR POWER METER OFFSEET ☐ dB ☐

GPIB OPERATION

PA – Power Active. Turns POWER METER option on.

PP – Power Passive. Turns POWER METER option off

PO – Power Offset. Enables entry of positive or negative power offsets to 0.1 dB resolution. Take a new reading after data entry if counter is not in HOLD.

THEORY OF OPERATION

The power meter uses the Schottky diode in the microwave converter as its power sensor. The output of the diode detector is connected to a programmable gain attenuator, which consists of two switchable gain stages (one is in the IF Amplifier A201B and one is on the Gate Generator A107) and two 8 bit attenuators. A comparator, set to 100 mV, and a TTL latch provide output information to the microprocessor. See Figure 02-1.

After the counter has a signal, and has taken a frequency reading, it starts the power meter task. This triggers the gate time counter, resets the TTL power latch, moves the YIG ±50 MHz (to insure that the signal peak is passed through), then checks the TTL power latch. If the latch is set, the attenuation is increased in 3 dB steps (until the signal is attenuated below the level of the comparitor), then back one step. If maximum attenuation is reached, and the latch is still being set, the word OVERLOAD is displayed and the task is exited.

When the latch is first checked, if it is still reset, the attenuation is decreased in 3 dB steps until the comparator level is reached. If minimum attenuation (maximum gain) is reached, the display is set to EE.E and the task is exited.

After the attenuation is adjusted to a 3 dB resolution, a successive approximation is performed to find the attenuation to a 0.1 dB resolution. The attenuation is stored, and if the gate time counter is not finished, the cycle is repeated. When the gate time counter is finished all the readings are averaged to eliminate the effects of AM on the signal.

The "power vs power" and "power vs frequency" corrections are added, and the sum is displayed. A detailed flowchart of the power meter is shown in Figure 02-2.

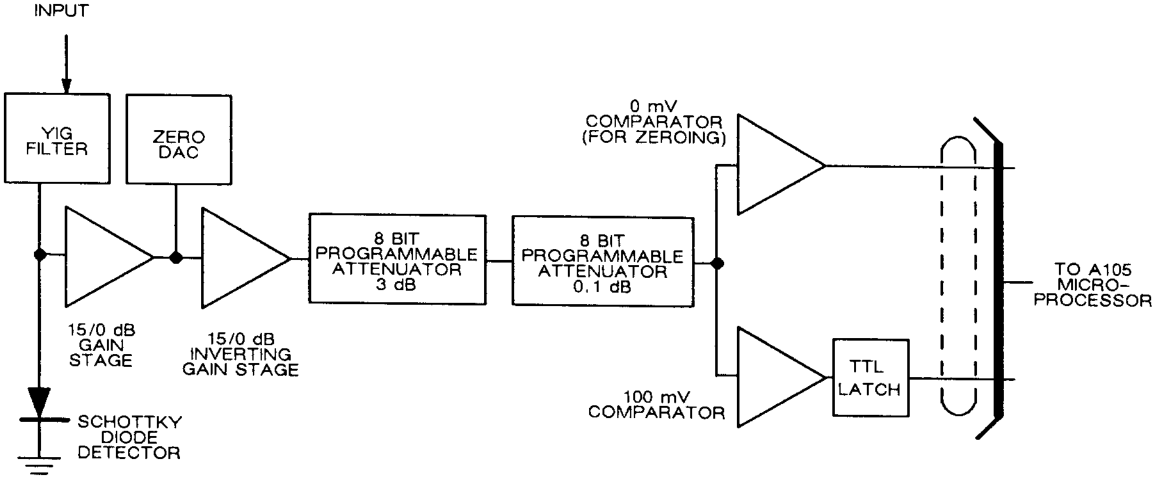


Figure 02-1. Power Meter hardware

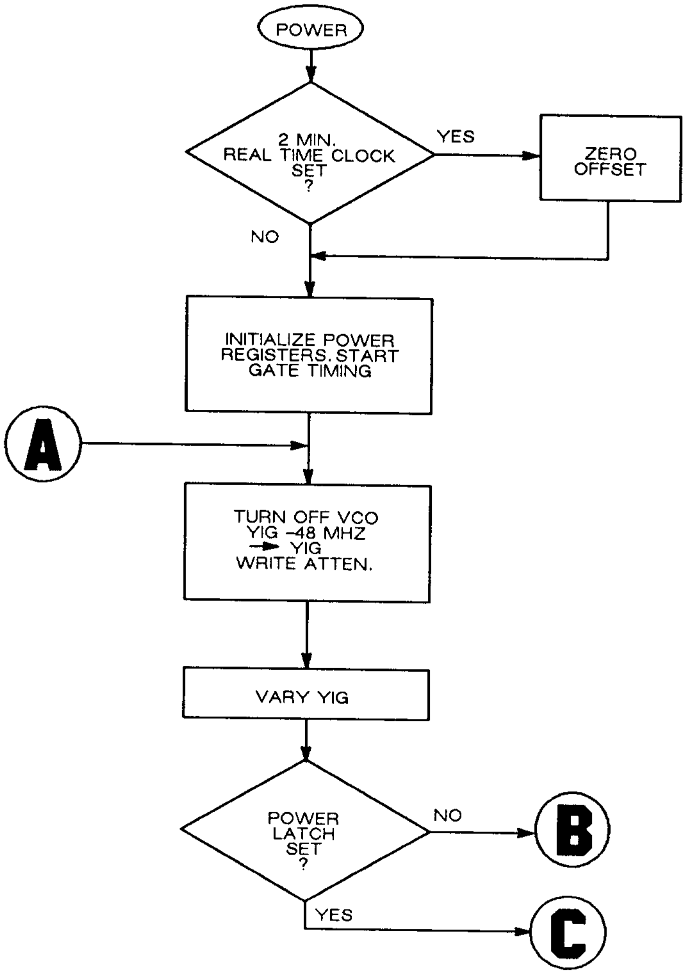


Figure 02-2. Power Meter Task

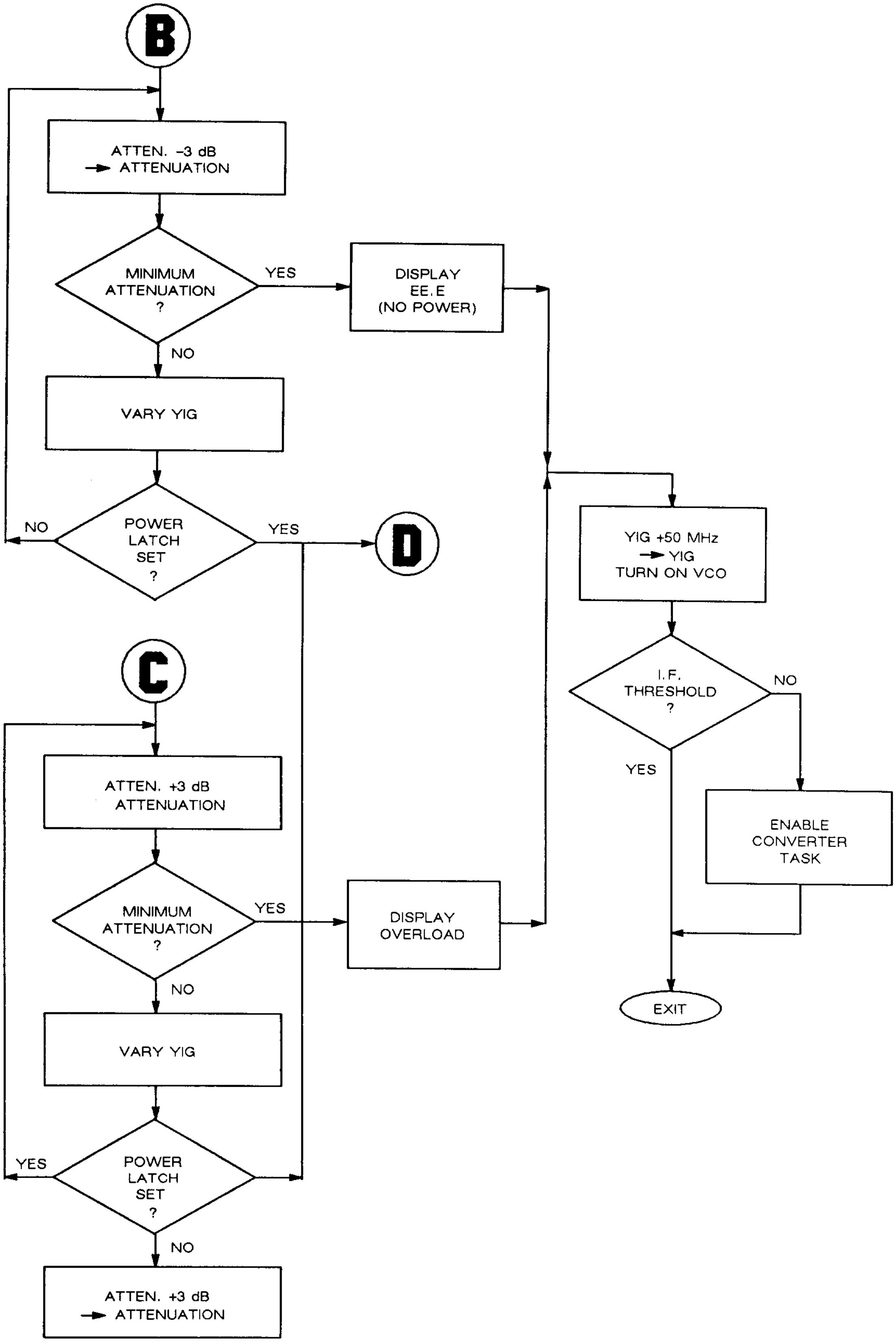


Figure 02-2. Power Meter Task, continued

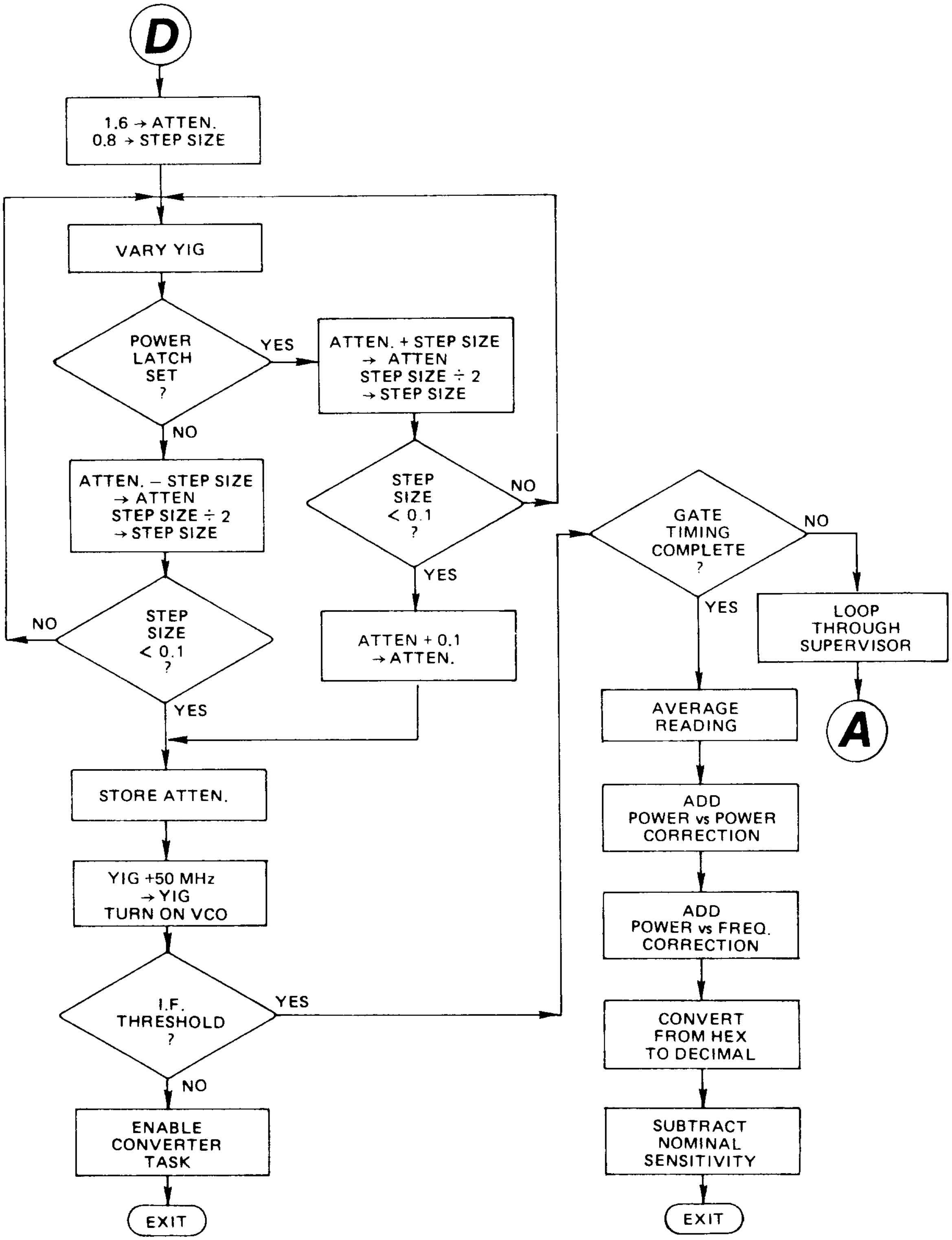


Figure 02-2. Power Meter Task, continued

CALIBRATION

The power meter contains 690 correction factors, stored in PROM.

The 150 "power vs power" correction factors compensate for variations from square law in the detector and power meter circuits. They are divided into three tables. The first table corrects variations below 10 GHz. The second corrects variations between 10 and 20 GHz. The third corrects variations above 20 GHz.

The 540 "power vs frequency" correction factors compensate for variations in the detector output at different frequencies. "Power vs frequency" corrections cover 0–27 GHz every 50 MHz.

The power meter is calibrated at the factory using specialized automatic test equipment. Recalibration in the field is not recommended.

(REFER TO SECTION 9, PAGES 107-5 AND 107-6 FOR PARTS LIST)

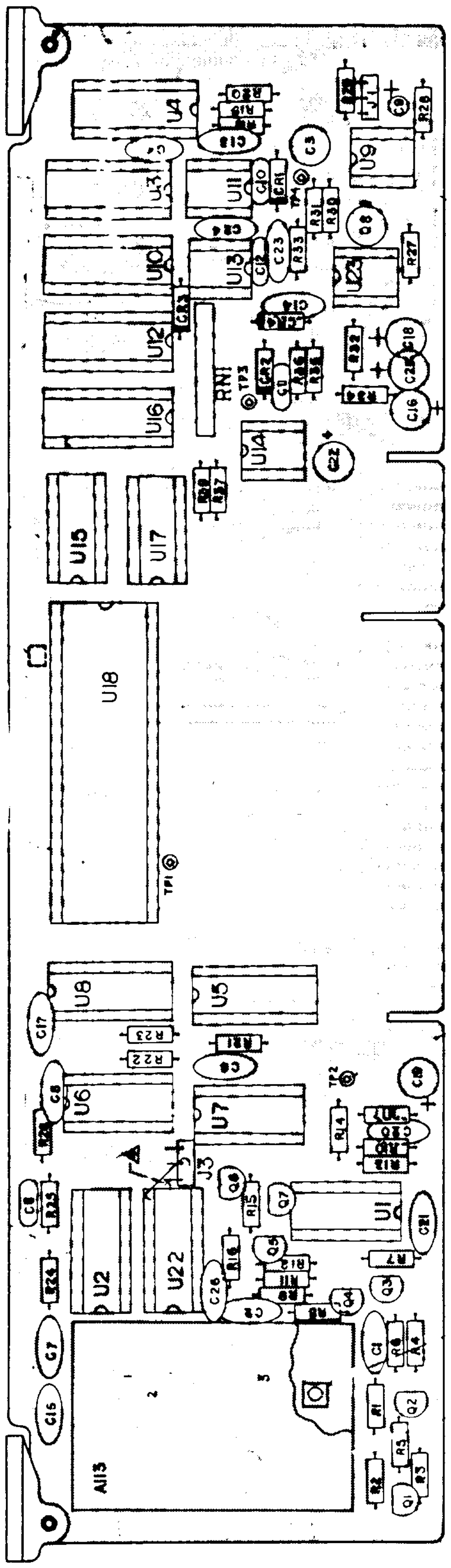
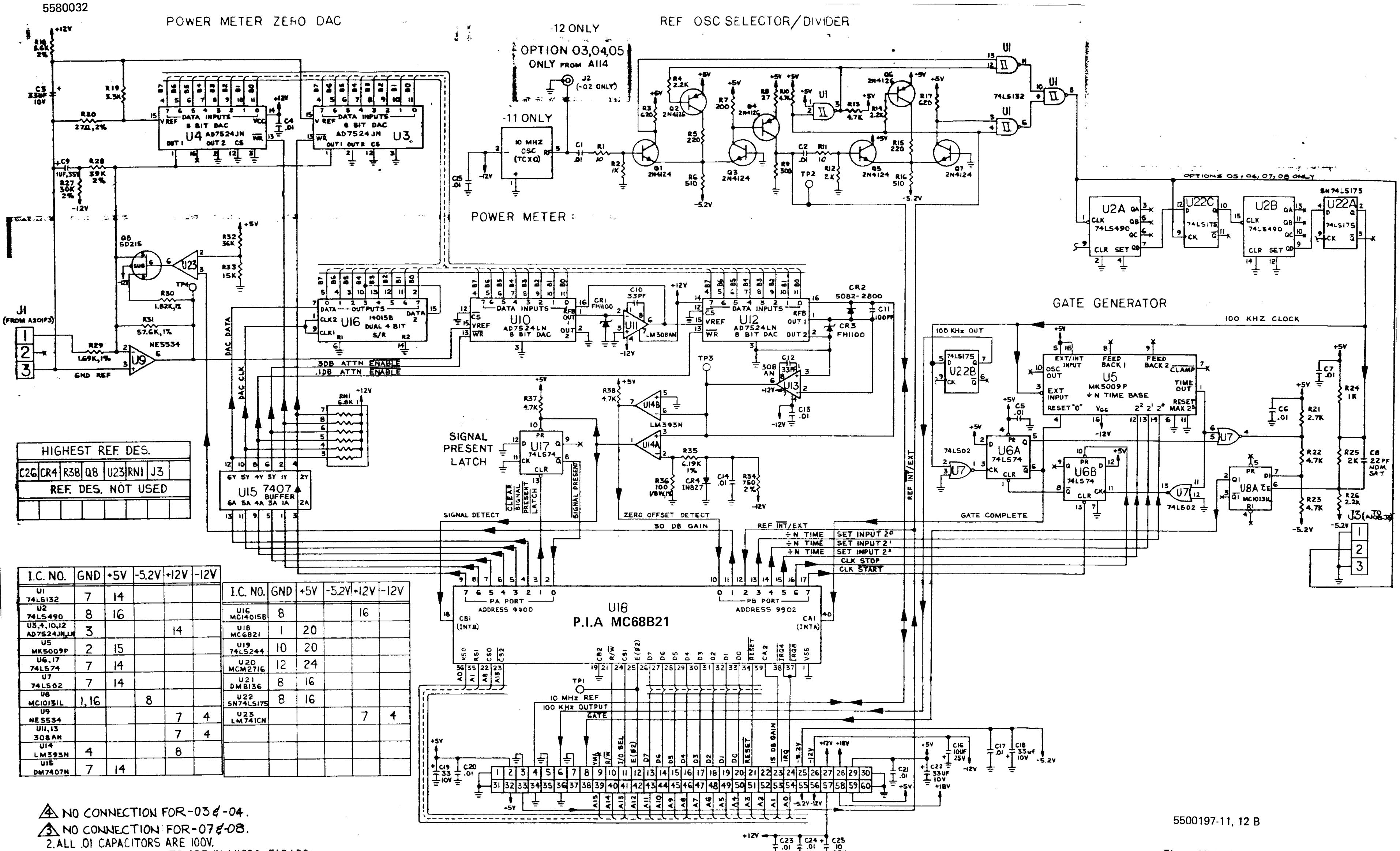


Figure 02-3. Gate Generator Component Locator



HIGHEST REF. DES.						
C26	CR4	R38	Q8	U23	RN1	J3
REF. DES. NOT USED						

I.C. NO.	GND	+5V	-5.2V	+12V	-12V
U1 74LS132	7	14			
U2 74LS490	8	16			
U3,4,10,12 AD7524JN,LN	3			14	
U5 MK5009P	2	15			
U6,17 74LS74	7	14			
U7 74LS02	7	14			
U8 MC10131L	1,16		8		
U9 NE5534				7	4
U11,13 308AN				7	4
U14 LM393N	4			8	
U15 DM7407N	7	14			

I.C. NO.	GND	+5V	-5.2V	+12V	-12V
U16 MC14015B	8			16	
U18 MC6821	1	20			
U19 74LS244	10	20			
U20 MCM2716	12	24			
U21 DM8136	8	16			
U22 SN74LS175	8	16			
U23 LM741CN				7	4

4. NO CONNECTION FOR-03&-04.
3. NO CONNECTION FOR-07&-08.
2. ALL .01 CAPACITORS ARE 100V.
ALL CAPACITOR VALUES ARE IN MICRO-FARADS;
1. ALL RESISTORS ARE ±5%,1/4W.
ALL RESISTOR VALUES ARE IN OHMS;
NOTES: UNLESS OTHERWISE SPECIFIED.

5500197-11, 12 B

Figure 02-4. Gate Generator Schematic

OPTIONS 03, 04, 05
TIME BASE OSCILLATORS

Three Time Base Oscillators are available as optitons for either the model 575B or 578B. These high stability options enhance the accuracy of the counter by the addition of oven stabilizied crystal oscillators. These oscillators improve counter operation by reducing both time and temperature variations.

When any one of these options is installed, the TCXO is removed from the Gate Generator board (A107) and the following components are added.

One of three Oven Oscillators (A114) mounted on the chassis.

- 28 VDC Power Supply board (A112), assembly part number 2010226.

Power Supply Transformer T1 (part number 4900006) mounted on A112.

Time Base Adjustment Pot J2 (part number 2010190) mounted on the rear panel.

Related interconnecting cable harnesses.

	OPTION 03	**OPTION 04**	**OPTION 05**
CHARACTERISTIC	2030010-01	2030010-02	2030010-03
AGING RATE/24 HOURS (After 72 hour warm-up)	$< \| 5 \times 10^{-9} \|$	$< \| 5 \times 10^{-9} \|$	$< \| 5 \times 10^{-10} \|$
SHORT TERM STABILITY (1 second average)	$< 1 \times 10^{-10}$ rms	$< 1 \times 10^{-10}$ rms	$< 1 \times 10^{-10}$ rms
0° to + 50° C TEMPERATURE STABILITY	$< \| 6 \times 10^{-8} \|$	$< \| 3 \times 10^{-8} \|$	$< \| 3 \times 10^{-8} \|$
± 10% LINE VOLTAGE CHANGE	$< \| 5 \times 10^{-10} \|$	$< \| 2 \times 10^{-10} \|$	$< \| 2 \times 10^{-10} \|$

Figure 03/04/05-1. Time Base Oscillator Option Specifications

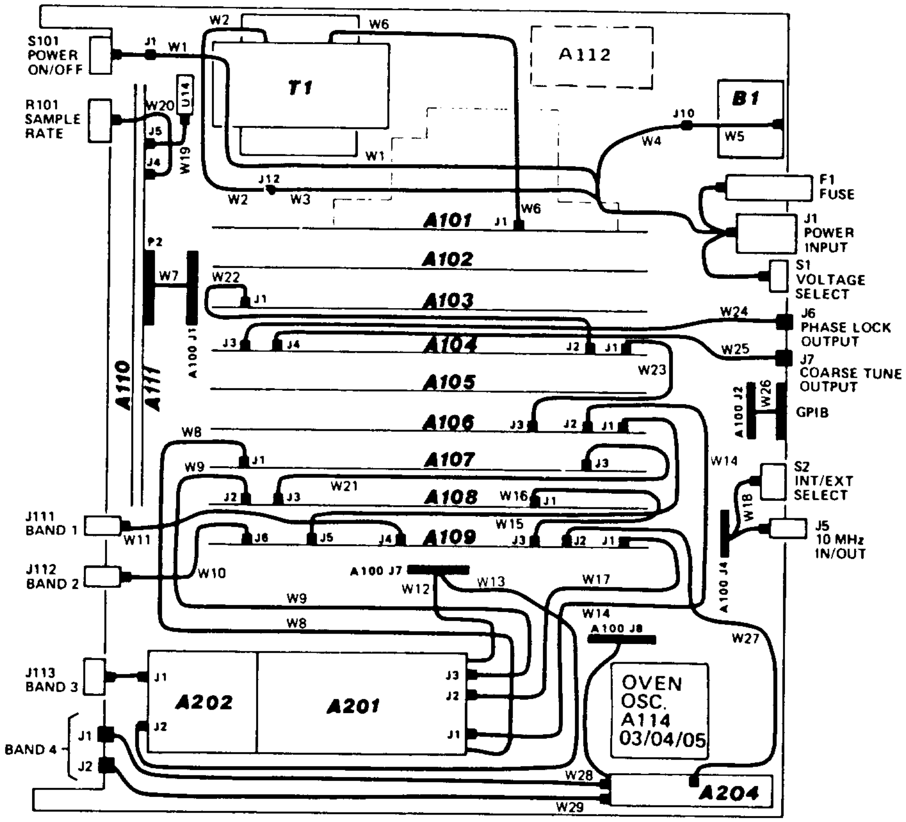


Figure 03/04/05-2. Component Location, Time Base Option

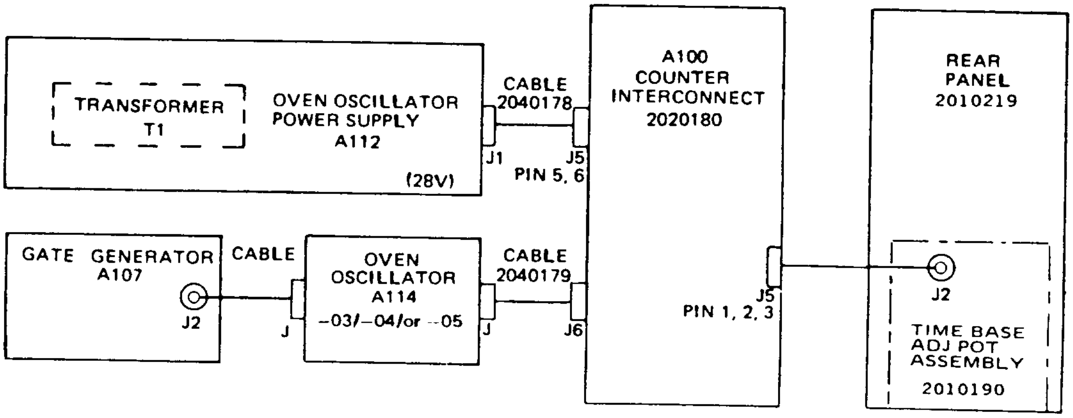


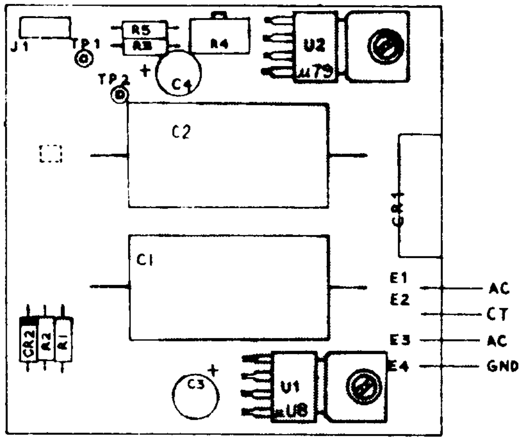
Figure 03/04/05-3. Time Base Option, Interconnection Diagram

OVEN OSCILLATOR POWER SUPPLY

The Oven Oscillator Power Supply board (A112) is a simple 28V regulated, current limited power supply. U1 and U2 provide voltage regulation, thermal protection and current limiting.

The transformer T1, CR1, C1 and C2 provide a 40V nominal unregulated DC voltage. The output voltage is set by voltage divider R5, R3 and R4. These resistors were selected so that 28V out provides 2.23V at U2 pin 2 (to U2 pin 1). Diode CR2 protects the supply from being pulled more negative than ground. See the schematic in figure 03/04/05-6.

The power supply (A112) is on and operating as long as the counter is connected to an active AC power source. The counter's POWER ON/OFF switch on the front panel does not control this assembly.



2020186

Figure 03/04/05-4. Oven Oscillator Power Supply (A112) Component Location

OVEN OSCILLATOR CALIBRATION

When options 03, 04 or 05 are installed in the counter, the effects of temperature perturbations and aging must still be considered, although the magnitude of the inaccuracies associated with each oscillator are greatly reduced.

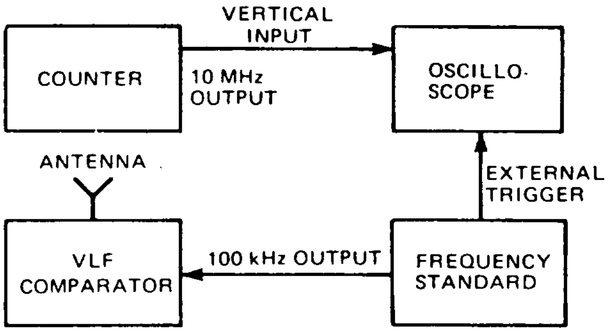
Full benefit of the oven stabilized oscillator characteristics can only be realized if the oscillator is running continuously (with counter always connected to a source of AC power). Under these conditions the perturbations in frequency will generally be in the positive direction for either an increase or decrease in temperature from + 25° C. The aging characteristic is also generally in the positive direction.

How frequently the oscillator is adjusted is determined by the level of accuracy required. To adjust the oscillator to an inaccuracy of less than 1 X 10^{-9} parts, relative to a standard, use this procedure. The test is illustrated in Figure 03/04/05-5.

Observe the drift of the oscilloscope pattern. The fractional frequency offset is computed from:

$$\frac{T_{\text{drift of zero crossing}}}{T_{\text{observation time of drift}}} = \frac{\Delta f}{f}$$

If the pattern drifts, at a rate of .01 microsecond every 10 seconds, the frequency is in error by 1 part in 10^9.



OVEN OSCILLATOR A114

Figure 03/04/05-5. Time Base Calibration.

All frequency checks and adjustments should be made only after the oscillator has been connected to its power source for 24 hours. If the oscillator has been disconnected from its power source for more than 24 hours it may require 72 hours of continuous operation to achieve the specified frequency aging rate.

To measure oscillator frequency:

1. Connect the counter's internal oscillator output signal from the 10 MHz IN/OUT connector (on the rear panel of the counter) to the vertical input of the oscilloscope.

2. Trigger oscilloscope externally with the frequency standard. The VLF comparator is used to determine the absolute frequency of the standard.

3. Set oscilloscope sweep rate to 0.01 µsec/cm.

4. Adjust oscilloscope vertical controls for maximum gain.

5. Determine the frequency difference (see page 6-24).

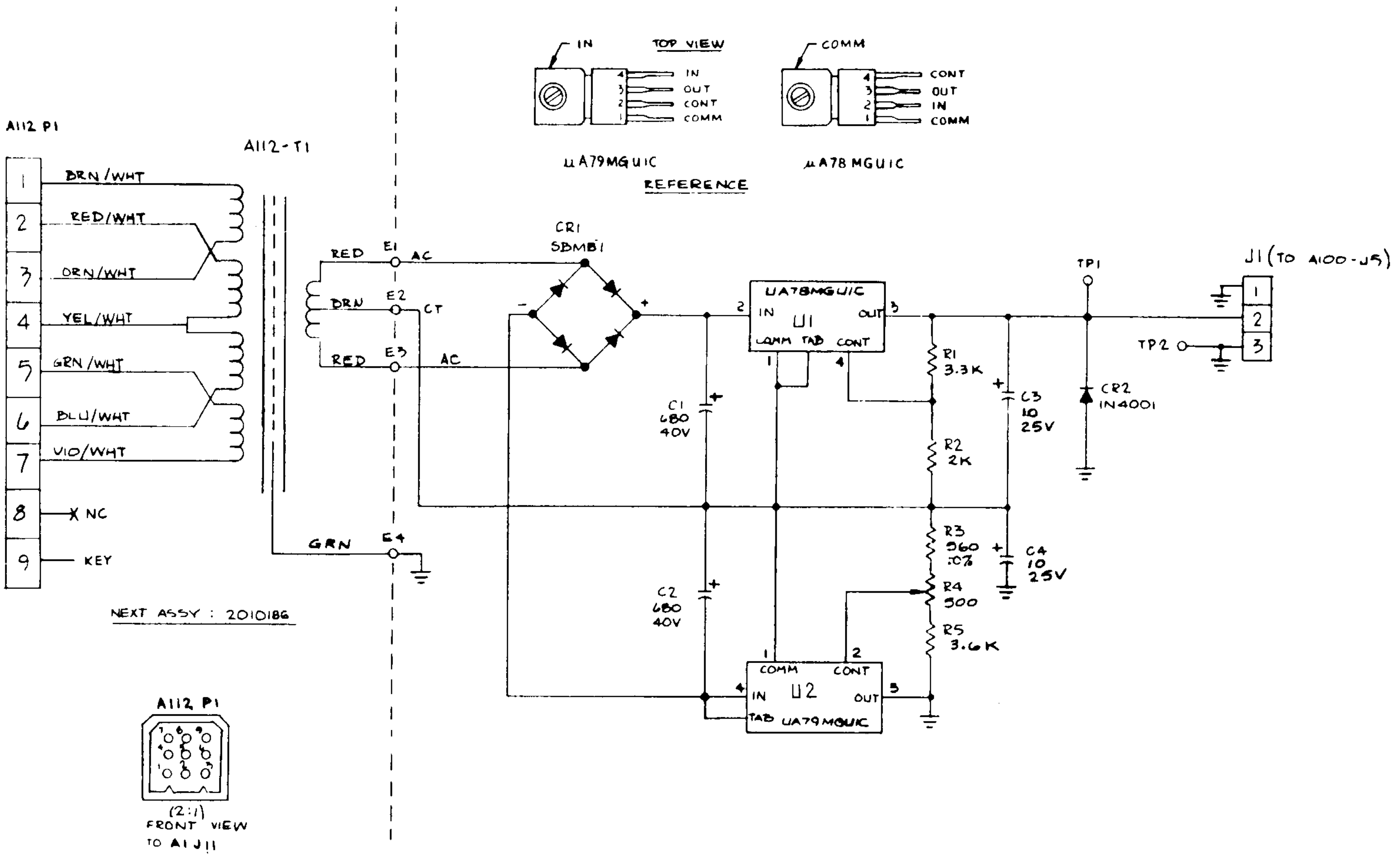
6. Horizontal drift of oscilloscope display in µsec/sec is a measure of the difference between the frequency standard and the counter oscillator frequency. If the difference is excessive for the desired counter application, vary the TIME BASE ADJUST control on the rear panel of the counter until the pattern stops drifting.

NOTE

For highest accuracy, the counter should be operated
for 72 hours prior to adjustment.

OPTION 03/04/05 - TIME BASE OSCILLATOR PCB ASSYs 2020186 - B

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A112	OSCILLATOR POWER SUPPLY	2020186	1	EIP	34527
C1	Elec, 680 uF, 40V	2200021	2	3074JH681T040JPB	80031
C2	C1				
C3	Tant, 10 uF, 25V	2300029	2	DF106M25S	NEC
C4	C3				
CR1	Bridge Rectifier	2710019	1	SBMB1	14099
CR2	Rectifier	2704001	1	IN4001	
R1	Met Ox, 3.3K, 2%,1/4W	4130332	1	C4/2%/3.3K	24546
R2	Met Ox, 2K, 2% ,1/4W	4130202	1	C4/2%/2K	24646
R3	Met Ox, 560, 2% ,1/4W	4130561	1	C4/2%/560	24546
R4	Variable, Cer, 500, 10%	4250014	1	72XR500	73138
R5	Met Ox, 3.6K, 2% 1/4W	4130362	1	C4/2%/3.6K	24546
U1	Positive Voltage Regulator	3040780	1	uA78MGUIC	07263
U2	Negative Voltage Regulator	3040790	1	uA79MGUIC	07263



5500186 - A

Figure 03/04/05-6. Time Base Option Schematic

OPTION 06

EXTENDED FREQUENCY CAPABILITY

The frequency range extension option is available on the 578B counter. This option, when used with the model 590 Frequency Extention Cable Kit and one of the optional remote sensors, enables the counter to operate above 26.5 GHz. The option consists of :

- Band 4 Converter Module
- Band 4 Software
- Modified Front Panel Overlay
- Coax Cable, Front Panel to A204 J1 – P/N 2040232
- Coax Cable, Front Panel to A204 J2 – P/N 2040231

KEYBOARD OPERATION

To operate the counter in one of the Band 4 frequency ranges, connect the short cable (supplied with the frequency extension kit) from the lower output jack on the front panel, to the Band 3 input. Connect the long cable from the upper jack to the remote sensor.

NOTE : Before connecting the remote sensor to the frequency source, verify that the power level is within the limits specified for the sensor. When you connect the sensor the counter will automatically display the reading.

To select Band 4:

PRESS : BAND ☐ Band annunciator flashes

PRESS : 4 Band 4 annunciator flashes

PRESS : # Selected Band 4 annunciator lights , stays on

The number should be between 1 and 4, corresponding to the desired frequency range. The counter is now in the proper mode for operation.

SPECIFICATIONS

BAND	FREQUENCY RANGE	SENSITIVITY (TYPICAL)	MAX. INPUT	REMOTE SENSOR MODEL
41	26.5-40 GHz	{ -25 dBm typ. -20 dBm min. }	+5 dBm	91
42	40-60 GHz	-25 dBm	+5 dBm	92
43	60-90 GHz	-25 dBm	+5 dBm	93
44	90-110 GHz	-25 dBm	+5 dBm	94

GPIB OPERATION

To select Band 4 through the GPIB, input B4 followed by one decimal digit between 1 and 4. The digit designates individual remote sensors.

EXAMPLE : B41 = remote sensor 1 which covers 26.5 to 40 GHz.

THEORY OF OPERATION – HARDWARE

When measuring a signal frequency greater than 26.5GHz, the 578B using the Option 06 Frequency Extension with a model 590 kit and a 91 remote sensor down converts the input to approximately 1.0 GHz. This signal is then fed to the Band 3 input, where a second conversion produces a 125 MHz IF.

A multiplier chain increases the VCO output frequency to the 5.28-6 GHz range, which is referenced to the time base. See Figure 06-1. This signal provides the local oscillator (LO) power, which is transmitted to the remote sensor, an external harmonic mixer. When the input frequency and harmonics of the LO, (generated in the mixer) combine, a first IF is generated in the range of 1.00-1.35 GHz.

A diplexer separates the LO and IF signals received from the harmonic mixer. The level of the IF is then increased to a minimum of -25 dBm via the IF amplifier, then supplied to the Band 3 converter input.

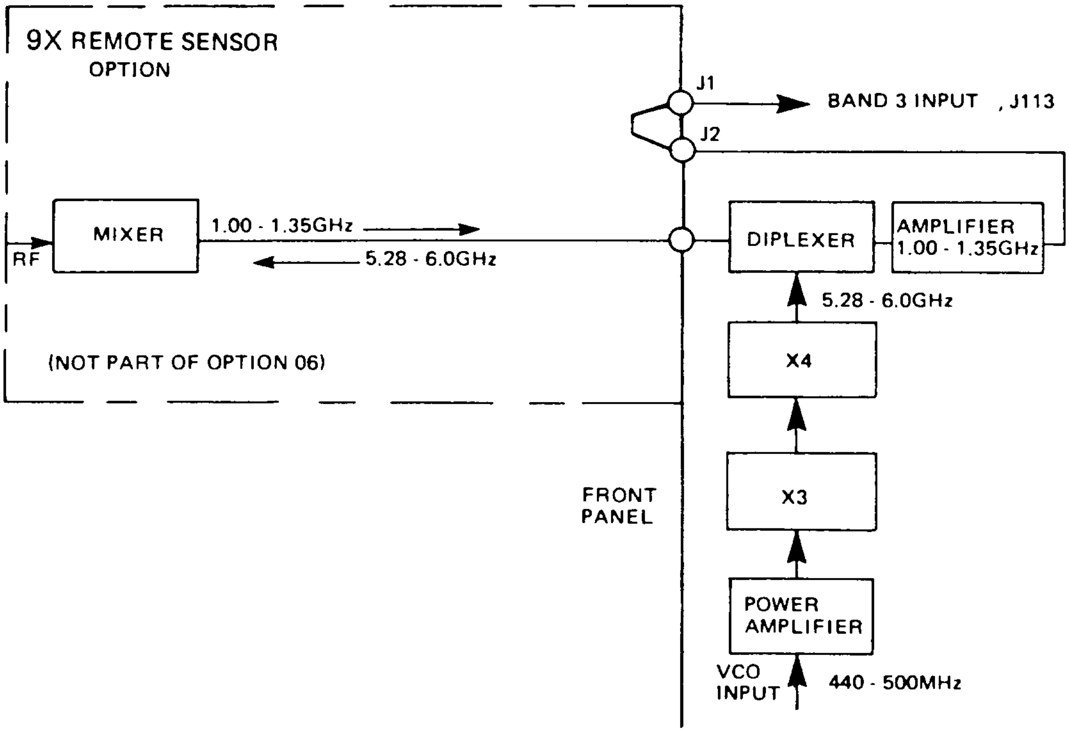


Figure 06-1. Frequency Extension Block Diagram

THEORY OF OPERATION - SOFTWARE (LOCKING ROUTINE)

The Band 4 software performs two main functions: it locks onto an incoming RF signal, and it tracks an RF signal once it is locked.

The locking routine is called by the supervisor when any of the following conditions are met:

1. Selection of Band 4
2. Software called from the source lock routine.
3. Lose of IF threshold after being locked.
4. Any reset condition.

LOCKING PROCESS

Initialization

The initialization routine clears the working table (BANDTB) for Band 4 and loads from PROM the table of constants that is used by the program for the selected Band 4 subband. BANDTB is an area in RAM that is 40 bytes long.

VCO Sweep

This routine steps the VCO frequency by a step size stored in BANDTB. After each step, it checks the VCO frequency for three stop points.

1. Top VCO frequency limit (depends on subband),
2. Wraparound frequency
3. Lockout frequency

If the top VCO frequency has been reached and no signal has been found, the program returns to the supervisor. If the top frequency is reached, and a signal has been detected, the VCO is set to its low limit and the bottom range is searched until the wraparound frequency is reached.

If the wraparound frequency has been reached (the frequency at which the last VCO frequency has produced the strongest IF signal), then the program stays at this frequency, and performs the centering and harmonic number calculation routines.

If a lockout frequency (a VCO frequency at which erroneous locking results) is detected, the VCO frequency will be incremented by :

8 * step size = new VCO frequency

and the program continues from this frequency.

After each VCO step, the YIG filter is swept to see if a signal is detected by the power DAC attenuator. If a signal is detected, the YIG is swept back and forth, and the attenuation is increased until the signal is lost. At this point a new VCO frequency is stepped and the process of signal detection continues and the power DAC is left at the last setting to detect the next highest signal.

Centering and Harmonic Numbering Determination

After the VCO sweep routine is complete and the VCO frequency is set, the incoming signal is mixed with a harmonic of the VCO frequency to produce a signal in a predetermined passband region (1.05 GHz to 1.25 GHz). Then a small VCO frequency is incremented to determine the mix side. After the VCO step, if the resulting IF increases, it is high side mix, otherwise, it is low side mix. The IF is then stepped to 1.05 GHz (or as close as possible) by using the following formula to calculate the VCO step size:

$$\frac{(\text{IF} - 1050\text{ MHz}) * 100}{12 * \text{N\_MAX}}$$

Where N_MAX is the highest harmonic number allowed in the subband.

The above calculation is performed at most twice to bring the IF to 1.05 GHz. At this point the YIG is centered and the centering frequency FYIG1 and VCO frequency FVCO1 are stored. Next the VCO is stepped to bring the IF to around 1.25 GHz and a new centering takes place. This second center frequency is stored for later calculation of the harmonic number. Next the signal is stepped to its previous position and centered. This center frequency is now compared to FYIG1, and must be within 6 MHz. If it is not within 6 MHz, it is assumed that the signal is moving, and the Band 4 program exited.

The IF frequency step size, caused by the VCO frequency step, is used to determine the harmonic number by the following equation.

$$\frac{\Delta \text{ IF FREQ. DUE TO VCO STEP}}{\text{HARMONIC SPACING}} = \text{HARMONIC \#(N)}$$

Where harmonic spacing = VCO step size X 12

CALCULATION ROUTINE – The calculation routine is used to find the approximate RF frequency F_{IN} in the following manner.

1. Compute $F' = 12 \text{ N X } F_{VCO}$
2. Center the YIG filter on the first IF
3. Convert the binary YIG frequency to BCD
4. Compute $F_{IN} = F' \pm F_{YIG}$ (where F_{YIG} gives the approximate value for the first IF).
5. Compute a corrected VCO frequency using the equation:

$$F_{VCO} = (F_{IN} \pm 127) / (12N \pm 2)$$

Then tune the VCO with the corrected frequency and center the first IF frequency in the YIG passband

SHALLOW SEARCH – This routine tests for a signal in the IF passband. If a signal is present, the routine is exited. If a signal is not present, the routine will search an RF range of ±60 MHz (in steps of 200 kHz), for the signal, and continues if a signal is found. If a signal is not found, the Band 4 program returns control to the supervisor.

BAND 4 TRACKING – The tracking routine centers the second IF in the following range.

$$115 \text{ MHz} < \text{2nd IF SIGNAL} < 135 \text{ MHz}$$

This routine is called from outside of the Band 4 program to track a signal. A test is first made to determine if an IF threshold is present. If IF threshold is present it continues, if not the program returns to the supervisor to start the locking process from the beginning.

This routine reads the second IF frequency and computes the new VCO frequency so that the second IF is in the range given above. A new YIG frequency is calculated and the VCO and YIG are "tuned" to produce a new IF. A new FLO (frequency added to the second IF to produce the displayed frequency), is calculated. The equation for this process is:

$$F_{LO} = F_{VCO} (12 \text{ N} \pm 2)$$

The YIG frequency is: NEW F_{YIG} = 2 (NEW VCO) + 127 MHz.

PERFORMANCE TESTS

The Band 4 converter module is not field repairable. When a malfunction is suspected, its operation can be checked from the front panel as follows:

IF AMPLIFIER — Apply a -50 dBm signal to the diplexer port (upper output jack) from 1.0 to 1.35 GHz. Output should be greater than -13dBm as checked on a spectrum analyzer to the IF output (lower jack).

LO SIGNAL — Connect a spectrum analyzer to the diplexer port (upper output jack). Using the following formula, set the VCO frequency between 440 and 500 MHz. The spectrum analyzer should show the 12th harmonic of the VCO frequency (5.28-6 GHz). The spectrum analyzer signal should be +8 dBm minimum, and free of breakup and spurious signals to -30 dBc.

To convert from the desired VCO frequency to the PIA program number:

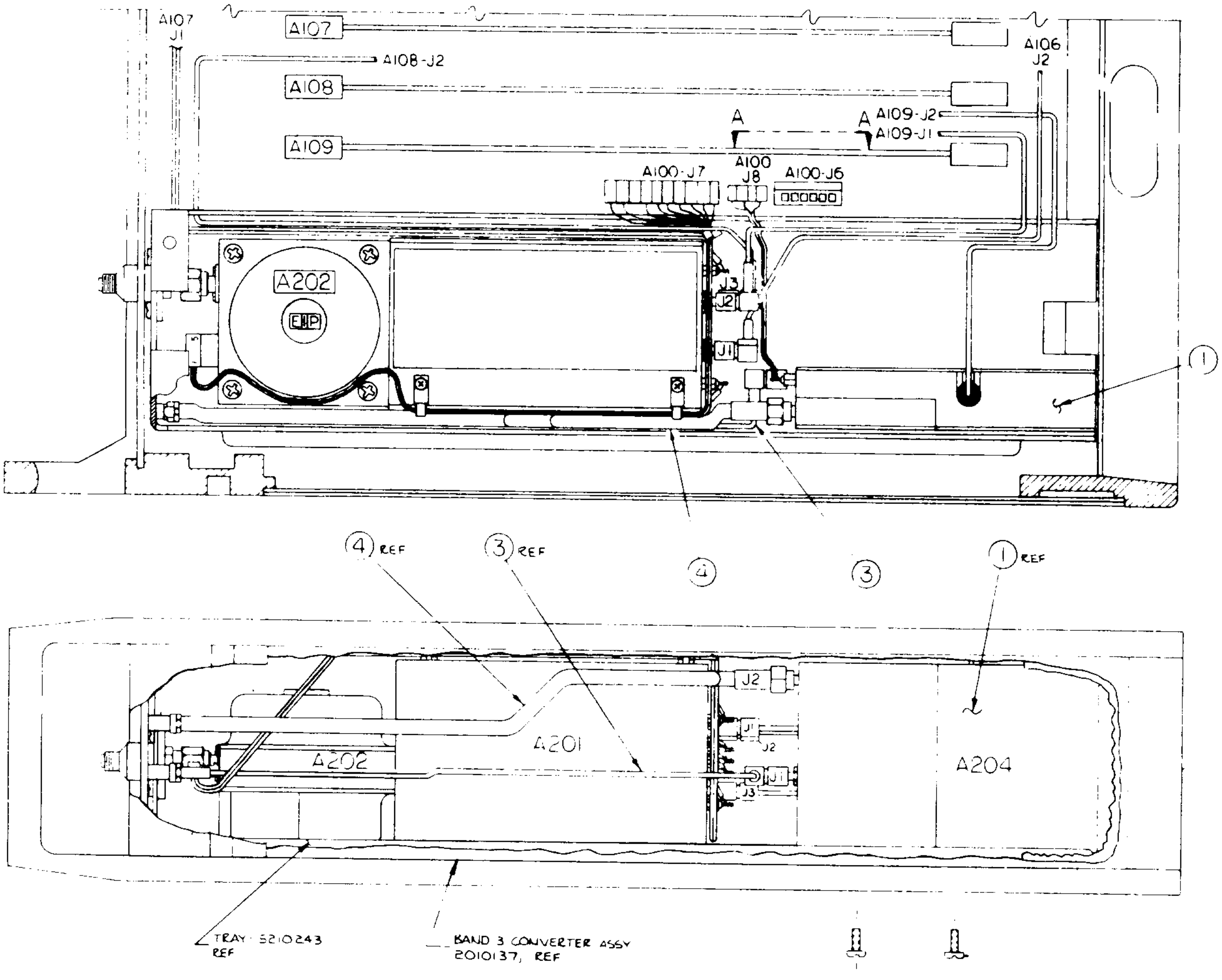
EXAMPLE (440.75 MHz)

1. Round the desired frequency to a multiple of 50 KHz (The resolution of the VCO frequency is 50 KHz).
2. Multiply the desired frequency (in MHz) by 5 . . . . 440.75 X 5 = 2203.75
3. If the result contains no fractional part, go to step 8.
4. Multiply only the fractional part by 16 .75 x 16 = 12
5. Add the result to the most significant digit from step 2 . . . . MSD of 2203.75 = 2 – 2 + 12 = 14
6. Convert the result to hexadecimal . . . . $14_{10} = E_{16}$
7. Replace the MSD from step 2 with the result from step 6 and drop the fractional part . . . . 2203.75 → E203
8. The two most significant digits are programmed to address 1822, and the two least significant digits are programmed to address 1820.

To remove a defective converter:

1. Remove the line cord and both the top and bottom cover of the counter.
2. Remove the two screws holding the converter in place from the bottom.
3. Remove coaxial cables and unplug DC harness.
4. Lift the converter out of the counter.

To replace, proceed in the reverse order. See Figure 06-5 for location of the converter in the counter.



① **Band 4 Converter** – 2010229

③ **Cable (FP to A204J1)** – 2040232-01

④ **Cable (FP to A204J2)** – 2040231-01

Figure 06-2. Location of Installed Band 4 Converter (A204)

OPTION 09
REAR PANEL INPUT

Option 09 provides rear panel input for 575B/578B counters, and counters equipped with Option 06 in the following manner:

575B/578B COUNTERS:

1. Reversing the converter assembly so that the Band 3 input connector protrudes through the hole in the rear panel that is identified as J113.
2. Reversing the Band 1 and Band 2 connectors to the holes marked J111 and J112 respectively on the rear panel.

Option 06 Equipped Counters:

1. Reversing the converter assembly so that the Band 3 input connector protrudes through the hole in the rear panel that is identified as J113. Reversing the Remote Sensor and Band 3 jumper connectors to the holes marked J114A (Rmt. Sensor) and J114B (Band 3 Connector) respectively.
2. Reversing the Band 1 and Band 2 connectors to the holes marked J111 and J112 respectively on the rear panel.

NOTE

The specifications for the counter do not change when the input is from the rear panel.

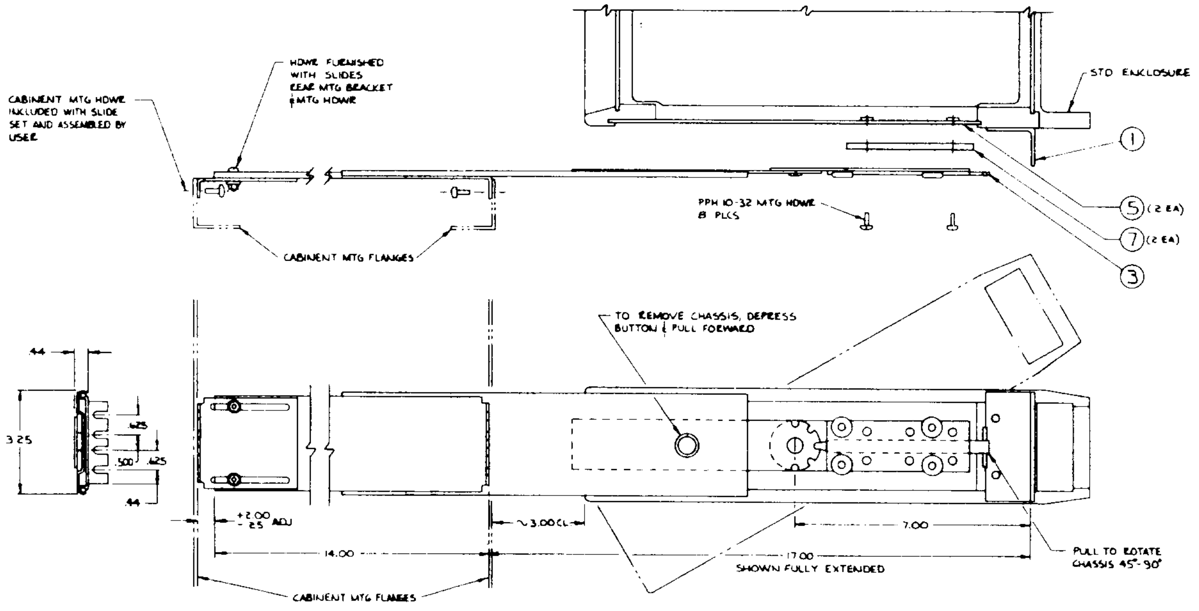
OPTION 10
CHASSIS SLIDE

Option 10 equips your counter with the hardware required to mount the unit in a standard 19" wide console. With the chassis slide installed the counter can be serviced without removing it from the rack.

The option consists of:

OPTION 10 – 2010147

①	Rack Mount Kit	– 2010008-01
③	Slide Set	– 5000189
⑤	Side Panels	– 5210179
⑦	Spacers	– 5210249



1. All MTG HDWR and hole spacing conforms to MIL-STD-189.
2. To install slides in field; Remove top cover and top frame; Mount special side panels (5210179) on Std. enclosure.
3. Item numbers within ○ symbol are on P/L 2010147. All other items assembled or exploded are shown for clarification or reference only.

Side View of Counter With Option 10 Installed

Appendix A
Accessories

MODEL 590 FREQUENCY EXTENSION CABLE KIT

The kit, part number 2000025 contains:

1 - LO Cable (long) - 2040217
1 - IF Cable (short) - 2040218
1 - Adaptor (SMA to TNC) - 2610063
0 - 5 - Remote Sensors (Options 91 thru 96)

REMOTE SENSOR OPTIONS

	PART NUMBER	FREQUENCY RANGE
91	2030022-00	26.5 - 40 GHz
92	2030029-00	40 - 60 GHz
93	2030030-00	60 - 90 GHz
94	2030031-00	90 - 110 GHz
95	2030038-00	50 - 75 GHz
96	2030059-00	33 - 50 GHz

SPECIFICATIONS

BAND 4
Used with 578B/06 Counter and 590 Frequency Extension Kit

OPTION	91	92	93	94	95	96
SELECT BAND	**41**	**42**	**43**	**44**	**42 or 43**	**41 or 42**
Waveguide Band	Ka	U	E	W	V	Q
Range	26.5-40 GHz	40-60 GHz	60-90 GHz	90-110 GHz	50-75 GHz	33-50 GHz
Sensitivity (typ)	-25dBm (-20 dBm min.)	-25 dBm	-25 dBm	-25 dBm	-25 dBm	-25 dBm
Waveguide Size	WR-28	WR-19	WR-12	WR-10	WR-15	WR-22
Waveguide Flange	UG-599/U	UG-383/U	UG-387/U	UG-387/U	UG-385/U	UG-383/U
Max. Input (typ)	+5 dBm	+5 dBm	+5 dBm	+5 dBm	+5 dBm	+5 dBm
Damage Level	+10 dBm	+10 dBm	+10 dBm	+10 dBm	+10 dBm	+10 dBm
Aquisition Time	<1 sec	<1 sec	<1 sec	<1 sec	<1 sec	<1 sec

INSTALLATION

Before connecting the remote sensor to the frequency source, verify that the power level is within the limits specified for the sensor.

Connect the long LO cable from the upper jack to the remote sensor. When using the sensor option 91, use the SMA-TNC adaptor in the 590 kit.

Connect the short IF cable from the lower jack to the Band 3 input.

CAUTION

Static discharge or ground loops can damage or destroy the diode in a remote sensor. ALWAYS connect the LO cable to the counter first, then touch the shield to the body of the sensor before connecting.

Be sure that the counter and waveguide port, to which the sensor will connect have a common ground. If in doubt, connect with a ground strap before connecting the remote sensor.

OPERATION

After connection, select Band 41, 42, 43 or 44 on the 578 counter (equipped with option 06). Select the band by:

BAND
PRESS: ☐ 4 1 or 42, 43 or 44.

Be certain that the band selected coincides with the remote sensor in use. See specifications Table.

NOTE

Frequency limits (low/high) and power meter function (Option 02) only operate to 26.5 GHz.

REPAIR

If loss of sensitivity occurs the diode in the sensor may be damaged. The 91 sensor diode can be replaced, all others require factory repair.

To replace the 91 sensor diode, unscrew the knurled cap and pull out the diode. Replace it with a 1N53B type diode that can be ordered from the manufacturer.

Alpha Industries, Inc.
20 Sylvan Road
Woburn, MA 01807

Or order from EIP by part number 2730053.

EIP has an assembly exchange program for rapid repair of damaged units. Consult factory for details.

SERVICE KIT

Th service kit for the 575B/578B counter contains the following items and the kit itself is useful as a carrying case.

2000017	Service Kit
2020147	GPIB/BCD Extender Board
2020184	Standard Extender Board
2020185	Band 2 Extender Board
2040221	Cable, BNC to Select
2040222	Cable, BNC to PC JK
2610054	Test Cable, BNC E/Z Hook
5000094	IC Extractor Tool

This kit comes in a useful carrying case.

Appendix **B**
List of Manufacturers

FSCM	MANUFACTURER
0000X	Any Manufacturer of this product.
00656	Aerovox Inc., 740 Belleville Ave, New Bedford, MA 02741
00809	Croven Ltd., Whitby, Ontario, Canada
01121	Allen-Bradley Co., South Milwaukee, WI 53204
01295	Texas Instruments Inc., Dallas, TX 75222
02660	Amphenol Connector Div., Bunker Ramo Corp., Broadview, IL 60153
02735	Solid State Div. RCA Corp., Somerville, NJ 08876
04618	American Pamcor Inc., Paoli, PA 19301
04713	Motorola Inc., Semiconductor Div., Phoenix, AZ 85008
06665	Precision Monolithic Inc., 1500 Space Park Drive, Santa Clara, CA 95050
07263	Fairchild Semiconductor, Mountain View, CA 94040
08717	Sloan Company, Sun Valley, CA 91352
09353	C & K Components Inc., Watertown, MA 02172
11236	CTS of Berne Inc., Berne, IN 46711
11237	CTS, Keen, Paso Robles, CA 93446
12463	Optronics Mfg., 2420 S. 60th St., Omaha, NE 68106
14158	AVX, Filters, 10080 Willow Creek Rd., San Diego, CA 92131
14298	American Components Inc., Conshohocken, PA 19428
14433	ITT Semiconductor Div., West Palm Beach, FL 33401
14455	Quality Hardware Mfg. Co., 12605 Daphine, Hawthorn, CA 90250
14655	Cornell Dubilier, Dept. 150, Ave. L, Newark, NJ 07101
18324	Signetics Corp., Sunnyvale, CA 94086
23880	Stanford Applied Engineering Inc., Santa Clara, CA 95050
23036	Pamotor Inc., Burlingame, CA 94010
24546	Corning Glass Works, Bradford, PA 16701
26654	Varadyne Ind., Santa Monica, CA 90404
27014	National Semiconductor Corp., Santa Clara, CA 95051
28480	Hewlett-Packard Co., Palo Alto, CA 94304
29990	ATC Div., Phase Ind., Huntington Station, NY 11746
34257	EIP Microwave Inc., Santa Clara, CA 95134
34649	Intel Corp., 3585 SW 198th Ave., Aloha, OR 97005
51406	Murata Corp. of America, 1148 Franklin Rd., Marietta, GA 30068
56289	Sprague Electric Co., North Adams, MA 01247
59660	Tusonix Inc., 2155 Forbes Bldg., Tucson, AZ 85705
70903	Belden Corp., Chicago, IL 60644
71590	Centralab Div., Globe-Union Inc., Milwaukee, WI 53201
72136	Electro Motive Corp., Sub. of Int. Elect. Corp., Florence, Santa Clara, CA 95050
72259	Nytronics Inc., Pelham Manor, NY 10803
72982	Erie Technological Products Inc., Erie, PA 16512
73445	Amperex Electronic Corp., Hicksville, NY 11802
80031	Mepco/Electra Inc., Morristown, NJ 07960
80740	Beckman Instruments Inc., Fullerton, CA 92634
81349	Military Specification
86797	Rogan Bros. Inc., Skokie, IL 60076
91637	Dale Electronics Inc., Columbus, NE 68601
95275	Vitramon Inc., Bridgeport, CT 06601
98291	Sealectro, Mamaroneck, NY 10544
99800	Delavan Div. American Precision Industries, East Aurora, NY 14052