Models 545/548
Microwave Frequency Counters

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List of Effective Pages

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PRELIMINARY ..... May 1979
FIRST EDITION ..... *March 1980*

Certification

EIP Microwave certifies that this instrument was thoroughly inspected and tested, and found to be in conformance with the specifications noted herein at time of shipment from factory.

Warranty

EIP Microwave warrants this counter to be free from defects in material and workmanship for one year from the date of delivery. Damage due to accident, abuse, or improper signal level, is not covered by the warranty. Removal, defacement, or alteration, of any serial or inspection label, marking, or seal, may void the warranty. EIP Microwave will repair or replace at its option, any components of this counter which prove to be defective during the warranty period, provided the entire counter is returned PREPAID to EIP or an authorized service facility. In-warranty counters will be returned freight prepaid; out-of-warranty units will be returned freight COLLECT. No other warranty other than the above warranty is expressed or implied.

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Section 1
General Information

DESCRIPTION

The 54X series is a microprocessor-based heterodyne device. The standard 545 and 548 cover the frequency range from 10 Hz to 18 GHz and 10 Hz to 26.5 GHz, respectively. The model 548, when equipped with frequency extension capability (option 06), is used in conjunction with a remote sensor (model 591) to cover the range from 26.5 to 40 GHz. Additional remote sensors extend measurement capability into higher narrowband mm ranges (e.g. 90-96 GHz).

Utilizing keyboard control, the 54X series counters provide frequency offsets and frequency selectivity. Options include power measurement, full systems capability via GPIB or BCD/Remote Programming and D/A Converter output.

Full frequency range is covered in three bands. Band 1 is a high (1 M ohms/20 pF) impedance input, and covers a 10 Hz to 100 MHz range, with a sensitivity of 25 mV RMS. Band 2 has an input impedance of 50 ohms, a 10 MHz to 1 GHz range, with a sensitivity of -20 dBm. Band 3 has an input impedance of 50 ohms nominal over its microwave range of 1 GHz to 18 or 26.5 GHz, and a sensitivity to -30 dBm. For frequencies above 26.5 GHz, a remote sensor, with an appropriate waveguide input, is designated as Band 4.

Measurements are presented on a 12 digit, LED display that is sectionalized to read GHz, MHz, KHz, and Hz. When the optional power measurement function is activated, the digits on the far right display power in dBm to 0.1 dB and frequency resolution is limited to 100 kHz.

SPECIFICATIONS

BAND 1	
RANGE	10 Hz to 100 MHz
SENSITIVITY	25 mV rms
IMPEDANCE	1 MΩ/20 pF
CONNECTOR	BNC (female)
MAX. INPUT LEVEL	120 V rms *
DAMAGE LEVEL	150 V rms *
	* (Above 1 KHz max. input will decrease at 6 dB/octive down to 3.0 V rms.)

BAND 2	
RANGE	10 MHz to 1 GHz
SENSITIVITY	-20 dBm
DYNAMIC RANGE	30 dB
IMPEDANCE	50Ω Nominal
CONNECTOR	BNC (female)
MAX. INPUT LEVEL	+10 dBm
DAMAGE LEVEL	+27 dBm
ACQUISITION TIME	< 50 msec

BAND 3	
RANGE	1 GHz to 18 GHz (26.5 GHz for model 548)
SENSITIVITY	-30 dBm = 1 GHz to 12.4 GHz -25 dBm = 12.4 GHz to 18 GHz -20 dBm = 18 GHz to 26.5 GHz
DYNAMIC RANGE	1 GHz to 12.4 GHz, 37 dB 12.4 GHz to 18 GHz, 32 dB 18 GHz to 26.5 GHz, 27 dB
IMPEDANCE	50Ω Nominal
CONNECTOR	Model 545 - Precision type N, (female) Model 548 - SMA (female)
MAX. INPUT LEVEL	+7 dBm
DAMAGE LEVEL	5 Watts (+37 dBm)
ACQUISITION TIME	~ 250 msec Independent of frequency
AUTO AMPLITUDE DISCRIMINATION	(Automatic amplitude discrimination of two frequencies) 10 dB
FM MODULATION	20 MHz P-P up to 10 MHz rate
VSWR	< 2.5:1 typical
FREQUENCY LIMIT	Keyboard control of desired limits (standard). Counter will measure largest signal within programmed limits. Signal outside operating band must be separated by at least 100 MHz from either limit. For signals more than 10 dB above desired signal, separation is typically 200 MHz

TIME BASE	
FREQUENCY	10 MHz TCXO
AGING RATE	$< \lvert 3 \times 10^{-7} \rvert$ per month
SHORT TERM	$< \lvert 1 \times 10^{-9} \rvert$ rms for one second averaging time.
TEMPERATURE	$< \lvert 2 \times 10^{-6} \rvert$ 0° to + 50°C
LINE VARIATION	$< \lvert 1 \times 10^{-7} \rvert \pm 10\%$ change.
WARM UP TIME	NONE
OUTPUT FREQUENCY	10 MHz, square-wave, 1 V p-p minimum into 50 ohms.
EXT. TIME BASE	Requires 10 MHz, 1 V p-p minimim into 300 ohms.

SPECIFICATIONS, continued

GENERAL	
RESOLUTION	Front panel keyboard input select 1 Hz to 1 GHz
MEASUREMENT TIME	1 msec for 1 KHz resolution 1 sec for 1 Hz resolution
DISPLAY	12 digit LED sectionalized
ACCURACY	±1 count ± time BASE ERROR
TEST	Front panel selected diagnostics
SAMPLE RATE	Controls time between measurements variable from 100 msec typ. to 10 sec. Switchable Hold position holds display indefinitely.
RESET	Resets display to zero and initiates new reading
OFFSETS	Keyboard control of frequency offsets (standard) and power offsets (standard with power measurement Option 02). Displayed frequency (power) is offset by entering value to 1 Hz resolution (0.1 dB power).
OPERATION TEMP.	0°C to 50°C
POWER	100/120/220/240/VAC ± 10% (selectable) 50 to 60 Hz, 60 VA typical
WEIGHT, NET	~20 lbs. (9.07 kg)
WEIGHT, SHIPPING	~25 lbs. (11.34 kg)
DIMENTIONS (HWD)	3.5" x 16.75" x 14.0" (89 mm X 425 mm X 356 mm)
ACCESSORIES FURNISHED	Power Cord and Manual

REMOTE SENSOR 591	
RANGE	26.5 GHz to 40 GHz
SENSITIVITY	-20 dBm
CONNECTOR	UG599/U Waveguide Flange (WR 28 Waveguide)
MAXIMUM INPUT LEVEL	+ 5 dBm
DAMAGE LEVEL	+ 10 dBm

OPTIONS **See Section 10 for detailed information.**

01 D TO A CONVERTER
DAC will convert any three consecutively displayed digits into an analog voltage output on rear panel.

02 POWER METER
1 to 18/26.5 GHz will measure sine wave amplitude to 0.1 dBm resolution and display simultaneously with frequency.
Power offset to 0.1 dB resolution, selectable from front panel.
Option will not degrade the basic performance of the counter.

TIME BASE OSCILLATOR OPTIONS:

	03	04	05
AGING RATE/24 HOURS (After 72 hour warm-up)	$< \lvert 5 \times 10^{-9} \rvert$	$< \lvert 1 \times 10^{-9} \rvert$	$< \lvert 5 \times 10^{-10} \rvert$
SHORT TERM STABILITY (1 second average)	$< 1 \times 10^{-10}$ rms	$< 1 \times 10^{-10}$ rms	$< 1 \times 10^{-10}$ rms
0° to +50°C TEMPERATURE STABILITY	$< \lvert 6 \times 10^{-8} \rvert$	$< \lvert 3 \times 10^{-8} \rvert$	$< \lvert 3 \times 10^{-8} \rvert$
± 10% LINE VOLTAGE CHANGE	$< \lvert 5 \times 10^{-10} \rvert$	$< \lvert 2 \times 10^{-10} \rvert$	$< \lvert 2 \times 10^{-10} \rvert$

SPECIFICATIONS, continued

OPTIONS, cont.
06 EXTENDED FREQUENCY CAPABILITY – 548 Use in conjunction with models 59X series Remote Sensors.
07 REMOTE PROGRAMMING/BCD OUTPUT
08 GPIB – Provides programming and output capability per IEEE 488-1975.
09 REAR INPUT
10 CHASSIS SLIDES

Section 2
Installation

INSTALLATION

There are no special installation instructions. The counter is a self-contained bench or rack mounted unit, and only requires connection to a standard, single-phase, 100/120/220/240. volt 50-60 Hz power line for operation.

CAUTION

Check current rating of counter fuse and setting of rear panel VAC selector switch before applying power to counter.

COUNTER IDENTIFICATION

This counter is identified by two sets of numbers. The model number 545 or 548, and a serial number that is located on a label that is affixed to the rear panel. Both numbers must be mentioned in any correspondence regarding your counter.

SHIPPING AND STORAGE

Wrap the counter in heavy plastic or kraft paper, and repack in original shipping carton. If the original container is no longer available, use a heavy (275 lb test) double-walled carton with approximately four inches of packing material between the counter and the inner carton. Seal carton with strong filament tape or strapping.

Mark the carton to indicate that it contains a fragile electronic instrument. Ship to EIP at address on the title page of this manual.

PERFORMANCE CHECKOUT PROCEDURE

The following procedure may be conducted without special tools or equipment.

1. Turn counter POWER switch off. Check fuse rating and setting of AC POWER switch on rear panel.

2. Connect power cord to 100/120 or 220/240 volt, 50-60 Hz single-phase power source. The ground terminal on the power cord plug should be grounded.

3. Turn POWER switch on. Dashes will be displayed for about one second, followed by all 0's. This indicates that the automatic self-check has been completed.

4. PRESS: TEST [0] [1] Display should read 200 000 000.

5. PRESS: TEST [0] [2] Display should read all 8's and all annunciators should be lit.

6. PRESS TEST [0] [3] Each display segment should light in turn.

7. PRESS: TEST [0] [4] Each digit should light in turn.

8. This completes the performance checkout procedure.

Section 3
Operation

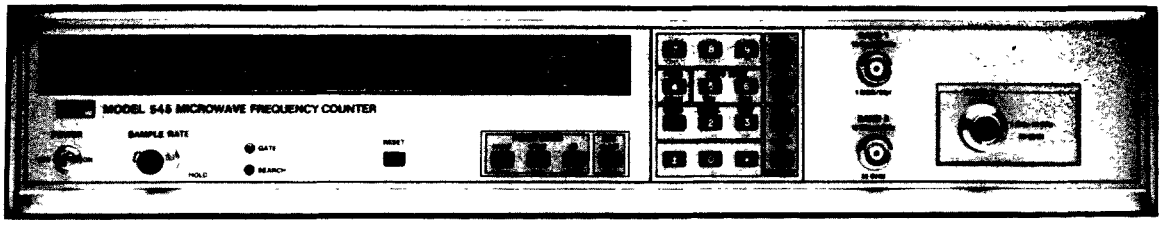


Figure 3-1. Front Panel, Model 545

FRONT PANEL CONTROLS AND INDICATORS

DISPLAY

- The 12 digit LED display provides a direct numerical readout of a measurement or of an input frequency. The frequency readout is displayed in a fixed position format that is sectionalized in GHz, MHz, kHz and Hz. Power information is displayed in dBm to 0.1 dB resolution, on the three right-most digits. When both power and frequency are displayed, frequency resolution is limited to 100 kHz.

- POWER switch turns counter on.

- SAMPLE RATE/HOLD varies time between measurements from 0.1 to 10 seconds (nominal) per reading. (Gate time is added to sample time, thus the minimum reading for 1 Hz resolution is 1.1 seconds.) The last reading is retained indefinitely in HOLD.

- GATE lights when the signal gate is open and a measurement is being made.

- SEARCH lights when the counter is not locked to an input signal.

- RESET manually over-rides all controls, resets the counter and converter, and initiates a new reading.

OPERATING STATUS

The operating status of the counter is indicated by a series of LEDs. When the counter is displaying input data, instead of a measurement, the appropriate LED status indicator will flash.

- REMOTE lights to indicate that front panel controls are disabled, and that the counter is being controlled by the GPIB option (08), or by the BCD/Remote Programming option (07).
- EXT REF lights to indicate the counter is set to an external time base reference.

CAUTION

When EXT REF lights it does NOT indicate that correct signal level has been applied.

- PWR dBm lights to indicate that the Power Meter option (02) is active.
- FRQ LMT, LOW/HIGH lights when frequency limits for counter operation have been selected.
- OFFSET, PWR/FRQ lights when power and/or frequency readings are offset from their actual value.
- BAND 1, 2, 3, 4 lights to indicate which operating range has been selected. When Band 4 is lit it indicates that the Extended Frequency Capability option (06) has been selected.
- DAC OPT lights to indicate that the Digital-to-Analog Converter option (01) is active.

POWER METER/DAC OPTION KEYBOARD

Four keys control the operation of these options.

- ON/OFF push button activates/deactivates power meter .
- OFFSET push button activates the power offset function.
- dB pushbutton acts as a terminator for the input of power offsets.
- DAC pushbutton, followed by two digits (00-12), activates the DAC option. The number keyed in will select the most significant digit (00 = OFF, 01 = 1 Hz, 12 = 10 GHz).

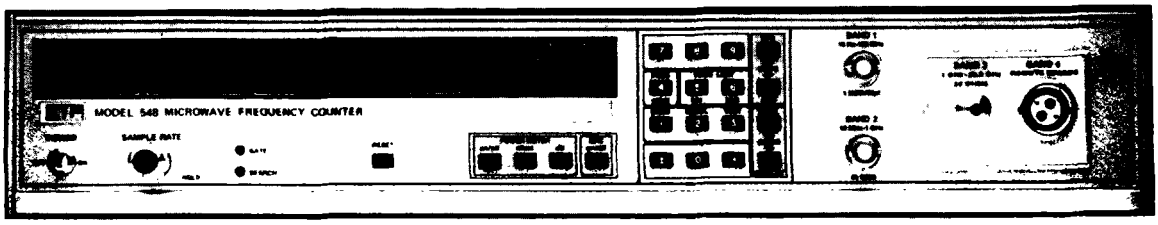


Figure 3-2. Front Panel, Model 548

SIGNAL INPUT

- BAND 1 input connector (BNC female) has a nominal input impedance of 1 Meg ohms, shunted by 20 pF. It is used for measurements in the range of 10 Hz to 100 MHz.

- BAND 2 input connector (BNC female) has a nominal input impedance of 50 ohm . It is used for measurements in the range of 10 MHz to 1 GHz.

- BAND 3 input connector on the model 545 is a precision type N female. It is used for counter operation in the range of 1 GHz to 18 GHz. Model 548 has a precision type SMA female connector that is used for operation in the range of 1 GHz to 26.5 GHz.

- BAND 4 is used in conjunction with the Extended Frequency capability option (06). It provides the interface between the Remote Sensor assembly and the 548 counter.

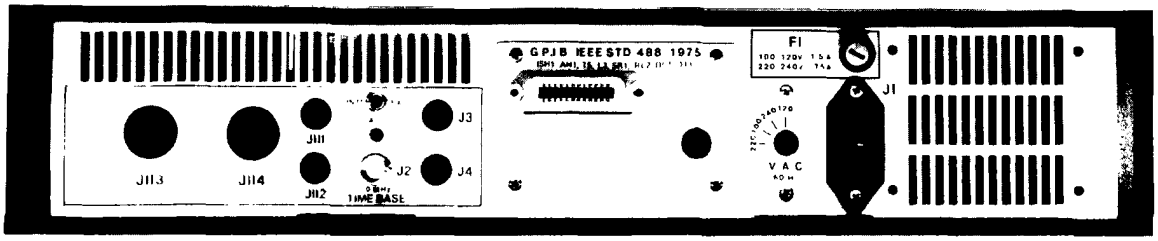


Figure 3-3. Rear Panel

REAR PANEL CONTROLS AND CONNECTORS

- AC POWER connector accepts the power cord supplied with the counter.
- FUSE provides overload protection. Use only a 0.75A slow-blow MDL type fuse for 100/120V operation. Use a 0.40A slow-blow FST type fuse for 220/240V operation.
- VAC SWITCH sets the operating voltage of the counter to match power line. There are 4 settings: 100, 120, 220, and 240 VAC. Counter will operate at voltages within ± 10% of selected line voltage, at frequencies of 50 to 60 Hz.

CAUTION
Switch setting and fuse rating must match power line voltage.

- GPIB connector is used with the IEEE 488-1975 General Purpose Interface Bus option (08).
- BCD OUTPUT and REMOTE PROGRAMMING connectors (not shown) replace the GPIB connector when the counter is equipped with the BCD OUTPUT/REMOTE PROGRAMMING option (07).
- TIME BASE ADJUST control is used with options 03, 04, or 05 only. Screwdriver adjustment allows precise setting of the internal ovenized crystal oscillator.
- TIME BASE INT/EXT switch selects either the internal time base or an external 10 MHz reference.
- TIME BASE connector (BNC female) allows monitoring of internal 10 MHz time base, or input of an external 10 MHz reference.
- DAC OUTPUT connector (BNC female) provides analog output voltage for the Digital-to-Analog Converter option (01).

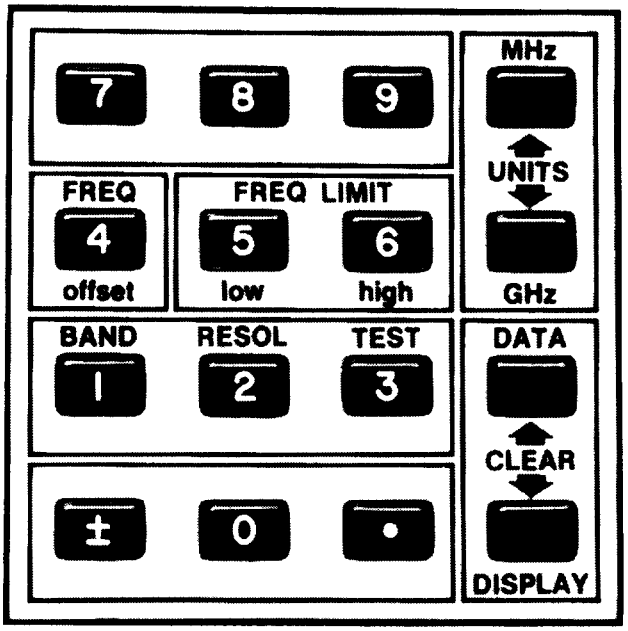


Figure 4-4. Keyboard

KEYBOARD

The keyboard consists of 16 pushbuttons that control major functions of the counter. Twelve keys are used for numerical data entry, the digits 0 through 9, the decimal point and the minus sign. Two keys (MHz and GHz) act as terminators for the input of frequency offset or frequency limits. The CLEAR DATA and CLEAR DISPLAY keys are used to clear stored or displayed data. Six of the numerical keys are also used to select the band, resolution, test function, frequency offset and frequency limits.

UNITS (MHz/GHz)

PRESS: MHz Completes Entry Sequence

PRESS: GHz Completes Entry Sequence

CLEAR (DATA/DISPLAY)

PRESS: DATA CLEAR Clears selected "STORED" data, i.e. Limits (Low/High), Offsets, and clears DAC operation.

PRESS: CLEAR DISPLAY Clears display. Does not affect stored data. Restores counter to measurement mode.

BAND SELECTION

To select one of three standard operating bands on the model 545 or 548.

PRESS: BAND [1] or BAND [2] or BAND [3]

Notice annunciator flash and selected band number will light when chosen. This feature allows multiple inputs to be connected and selected in turn.

The "BAND" KEY followed by a numeric key enables the following band selection.

PRESS: BAND [1] 10 Hz - 100 MHz Input

PRESS: BAND [2] 10 MHz - 1 GHz Input

PRESS: BAND [3] 1 GHz - 18 GHz (Model 545) 26.5 GHz (Model 548)

On the model 548, equipped with option 06 and a 59X series Remote Sensor, Band 4. is selected by:

PRESS: BAND [4] [X]

For example, with the 591 Sensor you will press BAND [4] [1]

RESOLUTION / GATE TIME SELECTION

The "RESOL" key followed by a numeric key enables following resolutions.

PRESS:	RESOL	0	1 Hz RESOLUTION
PRESS:	RESOL	1	10 Hz RESOLUTION
PRESS:	RESOL	2	100 Hz RESOLUTION
PRESS:	RESOL	3	1 KHz RESOLUTION
PRESS:	RESOL	4	10 KHz RESOLUTION
PRESS:	RESOL	5	100 KHz RESOLUTION
PRESS:	RESOL	6	1 MHz RESOLUTION
PRESS:	RESOL	7	10 MHz RESOLUTION
PRESS:	RESOL	8	100 MHz RESOLUTION
PRESS:	RESOL	9	1 GHz RESOLUTION

As the resolution is decreased from 1 Hz to 1 kHz, the gate time LED should cycle faster:

- 1 Hz resolution equals a gate time of 1 sec.
- 10 Hz = 100 msec Gate time
- 100 Hz = 10 msec Gate time
- 1 KHz to 1 GHz = 1 msec Gate time

DISPLAY AND DATA ENTRY SEQUENCE

The keyboard display and data entry sequences are segmented into four main groups. All keyboard operations must be started by choosing the function first.

DATA ENTRY - enter offsets or limits

Sequence : 1. FUNCTION , SIGN (plus sign not required) , NUMBER , DECIMAL , NUMBER , UNITS (decimal and second number is optional)

2. FUNCTION , NUMBER

Example : 1. FREQ OFFSET [±] [1] [•] [2] GHz

2. BAND [2]

DISPLAY DATA - display previously entered data

Sequence : FUNCTION , CLEAR DISPLAY

Example : FREQ OFFSET CLEAR DISPLAY

CLEAR DATA - clear entered data

Sequence : 1. FUNCTION , CLEAR DATA

2. FUNCTION , [0] , UNITS

3. FUNCTION , UNITS

Example : 1. OFFSET DATA CLEAR

2. OFFSET [0] dB

3. dB OFFSET

CLEAR ENTRY - clear display before completing data entry

Sequence : FUNCTION , STRING , CLEAR DISPLAY

Example : FREQ OFFSET [1] [•] [2] CLEAR DISPLAY

FREQUENCY LIMITS

Frequency limits can be entered to 10 MHz resolution .

PRESS: FREQ LIMIT / low · Notice flashing annunciator.

PRESS: # Number keys corresponding to desired frequency low limit to 10 MHz resolution.

PRESS: MHz or GHz To terminate input sequence. Notice FRQ LMT LOW annunciators solidly lit.

PRESS: FREQ LIMIT / high Notice flashing annunciator

PRESS: # Key numbers corresponding to desired freq. Hi limit. High and low limits should be separated by at least 100 MHz.

PRESS: MHz or GHz To terminate input sequence. Notice Hi annunciator solidly lit.

To recall stored limits.

PRESS: FREQ LIMIT / low and CLEAR / DISPLAY then FREQ LIMIT / high and CLEAR / DISPLAY

To clear data memory and remove frequency limits.

PRESS: FREQ LIMIT / low and DATA / CLEAR then FREQ LIMIT / high and DATA / CLEAR Vary Source. Notice selected limit (s) are erased. Also notice "FREQ LMT LOW HI" annunicators are out.

TEST SELECTION

The following tests will verify proper operation of most functional areas of the counter. At the initial turn on the counter performs a RAM and PROM check. During this check dashes are displayed until the check has been completed.

RAM and PROM

The processor writes a sequential bit pattern to each RAM location, then independently reads that pattern. Thus each bit in each location is checked. If the RAM check fails the display will show all "E's". This indicates that the RAM or the RAM decoding is faulty.

The PROM check verifies the PROM bit pattern. If the PROM check fails an error message will be displayed. This indicates that the PROM decoding is faulty. See Section 6.

If both RAM and PROM check are good the counter will begin normal operation about one second after turn on. The counter will now display all 0's.

200 MHz SELF TEST

PRESS: TEST [ ] [0] [1]

Notice display is 200 MHz. This verifies operation of the time base reference and it's associated circuits, the signal selection, the count chain, and the local oscillator.

LED TEST

PRESS: TEST [ ] [0] [2]

Notice all LED segments and yellow annunciators are lit. This verifies operation of all visual indicators

LED SEGMENT TEST

PRESS: TEST [ ] [0] [3]

Notice each segment of each display digit is lit in turn. The sample rate pot will change the rate, and may be adjusted. This checks the segment drivers.

DISPLAY DIGIT TEST

PRESS: TEST [ ] [0] [4]

Notice all segments of each digit are lit in turn to verify that each digit operates independently.
The sample rate pot will change the rate, and may be adjusted.

KEYBOARD TEST

PRESS: TEST [ ] [0] [5]

Notice display is 05. Press any key and display will indicate a two digit number showing the position of that key within the matrix thus checking keyboard operations.

TO EXIT TESTS

PRESS: CLEAR DISPLAY [ ] to exit a test and return to normal operation.

To exit tests 1 through 4, 6 and 7 you can press any function key. This will exit the test and enter the function selected.

Tests 6 through 10 are used for calibration and troubleshooting. See section 6 and 7.

SET-UP FOR BASIC FREQUENCY MEASUREMENT

Choose the input band by pressing BAND and a number key corresponding to the band. Choose resolution by pressing RESOL and a number key corresponding to required resolution. The signal coupled to the selected input Band Connector will be automatically displayed to the resolution chosen.

NOTE: When pressing the RESOL key the display will go blank for approximately 1/4 second.

FREQUENCY OFFSETS

Frequency OFFSETS can be added or subtracted from the measured value. These OFFSETS can be entered via the front panel keyboard to 1 Hz resolution:

PRESS: FREQ / OFFSET — Notice the flashing annunciator.

PRESS: Number keys corresponding to desired frequency OFFSETS. If OFFSET is to be subtracted press ± and notice polarity sign indicator at far left of display.

PRESS: MHz or GHz to integrate Programmed OFFSET into actual frequency measurement. Notice solidly lit annunciator indicating instrument memory is loaded.

PRESS: FREQ / OFFSET — Recalls OFFSET to display, FRQ and OFFSET annunciators flashing.

PRESS: CLEAR / DISPLAY — Notice frequency displayed includes OFFSET; annunciators are lit continuously.

PRESS: FREQ / OFFSET — Recalls OFFSET to display; FRQ and OFFSET annunciators flashing.

PRESS: CLEAR / DATA — Clears data memory and clears offset.
FRQ and OFFSET annunciators are out.
Display is actual frequency without offset.

DISPLAY ERROR MESSAGES

When an error occurs the error number will be displayed. The probable cause of each error is listed below.

01	Illegal Key Sequence.			
02	A Resolution Number Was Not Entered; Or The Number Entered Was Too Small.			
03	A Band Number Was Not Entered; Or The Number Entered Was Too Large.			
04	No Power Reading In Current Band.			
05	Frequency Limit High > 18.5 GHz (545), 27 GHz (548).			
06	(Freq. Limit Hi) – (Freq. Limit Lo) < Min. (100 MHz) Difference.			
07	Frequency Limit Low < .95GHz (545, 548).			
08				
09	Illegal Test Mode Key Sequence.			
10	Illegal DAC operation.			
31	Check sum Error	PROM 1	(C800 - CFFF)	A105, U20
32	Check sum error	PROM 2	(D000- D7FF)	A105, U8
33	Check sum error	PROM 3	(D800 -DFFF)	A105, U7
34	Check sum error	PROM 4	(E000 -E7FF)	A105,U6
35	Check sum error	PROM 5	(E800 - EFFF)	A105,U13
36	Check sum error	PROM 6	(F000-F7FF)	A105, U12
37	Check sum error	PROM 7	(F800 -FFFF)	A105, U11
38	Check sum error	PROM 8	(4000 - 47FF)	(Power Meter PROM)

Section 4
Theory of Operation

GENERAL

The 545 and 548 counters automatically measure and display the frequency of an input signal within the range of 10 Hz to 18 GHz for the 545, and 10 Hz to 26.5 GHz for the 548. In both models the frequency range is divided into three bands.

BAND 1 operates from 10 Hz to 100 MHz. An impedance converter provides an input impedance of 1 M ohm, shunted by 20 pF.

BAND 2 operates from 10 MHz to 1 GHz, using a hetrodyne down converter which converts the input signal into an output signal with a range of 10 MHz to 190 MHz.

BAND 3 operates in the microwave range of 1 to 18 GHz (or 26.5 GHz) and uses a YIG tuned hetrodyne converter to translate the input frequency downward to an intermediate frequency (IF) of 125 MHz.

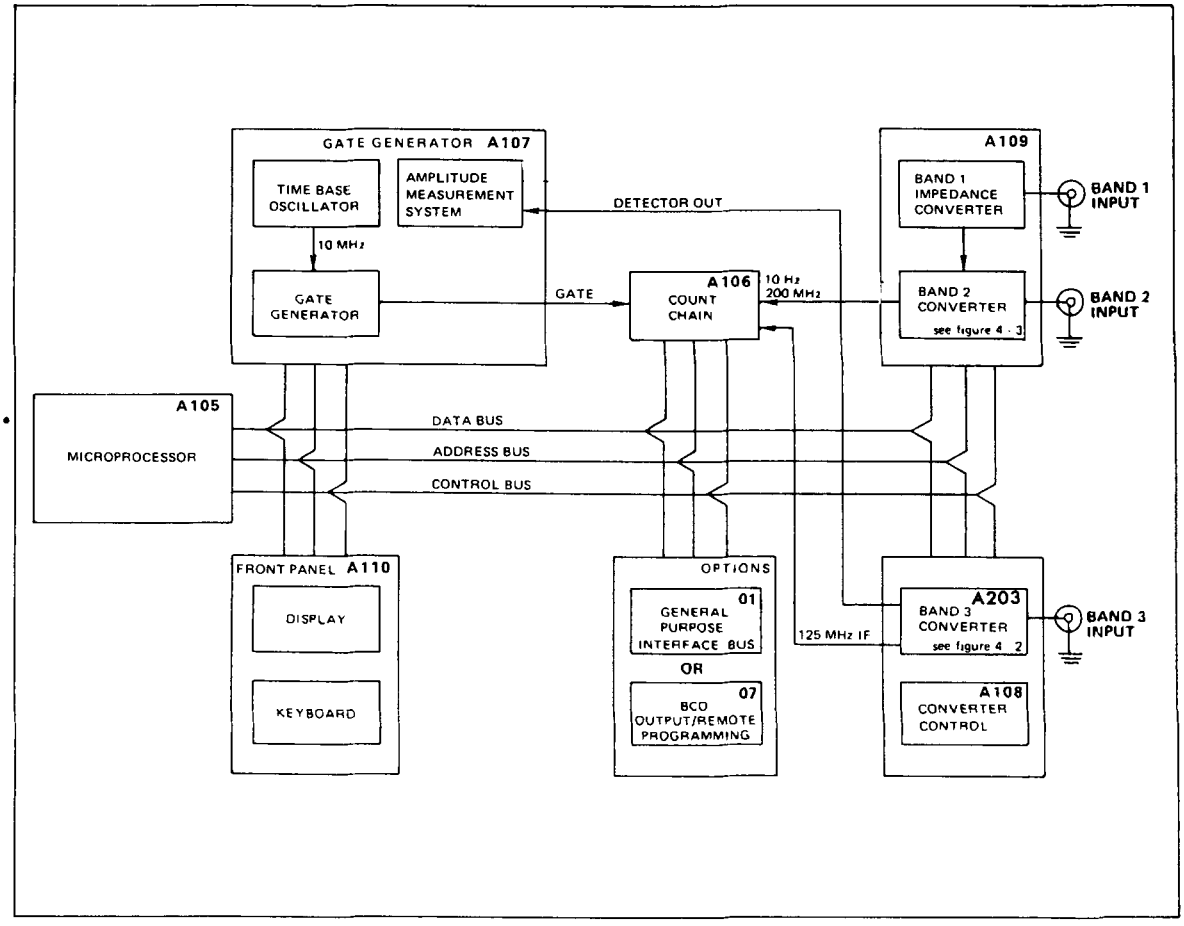


Figure 4-1. Counter Block Diagram, Simplified

BASIC COUNTER

Overall operation is controlled by the Microprocessor Assembly A105. This assembly contains an eight bit microprocessor, its control logic, and the system memory. It communicates with all other assemblies in the instrument by means of a triple bus system: the data, address, and control bus. On each assembly there is a Peripheral Interface Adaptor (PIA) which provides the interface between the bus system and the instrument hardware.

Frequency measurements are performed by comparing an unknown signal to a reference frequency, namely the time base. A 10 MHz crystal oscillator is used as the internal reference and is a part of the Gate Generator Assembly A107. For increased accuracy and stability, ovenized oscillator options are available, or the user may select an external 10 MHz reference.

A frequency measurement is made by generating a time interval (Gate Time) consisting of a number of cycles of the reference. This Gate Time is then used as an interval during which the input signal is counted by the Count Chain Assembly A106.

Initially, the microprocessor selects one of several available inputs to the Count Chain Assembly and the appropriate Gate Time based on user input information; band selection, resolution, etc. The microprocessor then initiates the measurement cycle by resetting the Count Chain to zero and allowing a gate to be generated. During the gate interval, the Count Chain accumulates the number of cycles of the input signal. At the end of the gate time, the microprocessor reads the stored information in the Count Chain and performs any required calculations necessary to convert the measurement into a direct reading of the unknown frequency. The front panel display is then updated with the new measurement results. Figure 4-1 shows a simplified block diagram of the counter.

BAND 2 CONVERTER

An input signal is applied to the mixer along with an appropriate local oscillator (L.O.) to generate an IF frequency in the range of 10 MHz to 190 MHz. This signal is filtered and amplified to a level suitable for direct measurement by the Count Chain.

The L.O. frequency is generated by the Voltage Controlled Oscillator (VCO) of the Band 3 Converter. This frequency is phase locked to the counter's time base and controlled by the microprocessor. A VCO multiplier serves to either pass along the signal directly or double it. It can also turn off the signal and pass only a DC bias to the mixer.

Two detectors provide outputs proportional to the amplitudes of both the applied RF signal and the resulting IF signal. These outputs are compared in the Signal Comparator, which provides a digital output when the IF amplitude exceeds the RF amplitude.

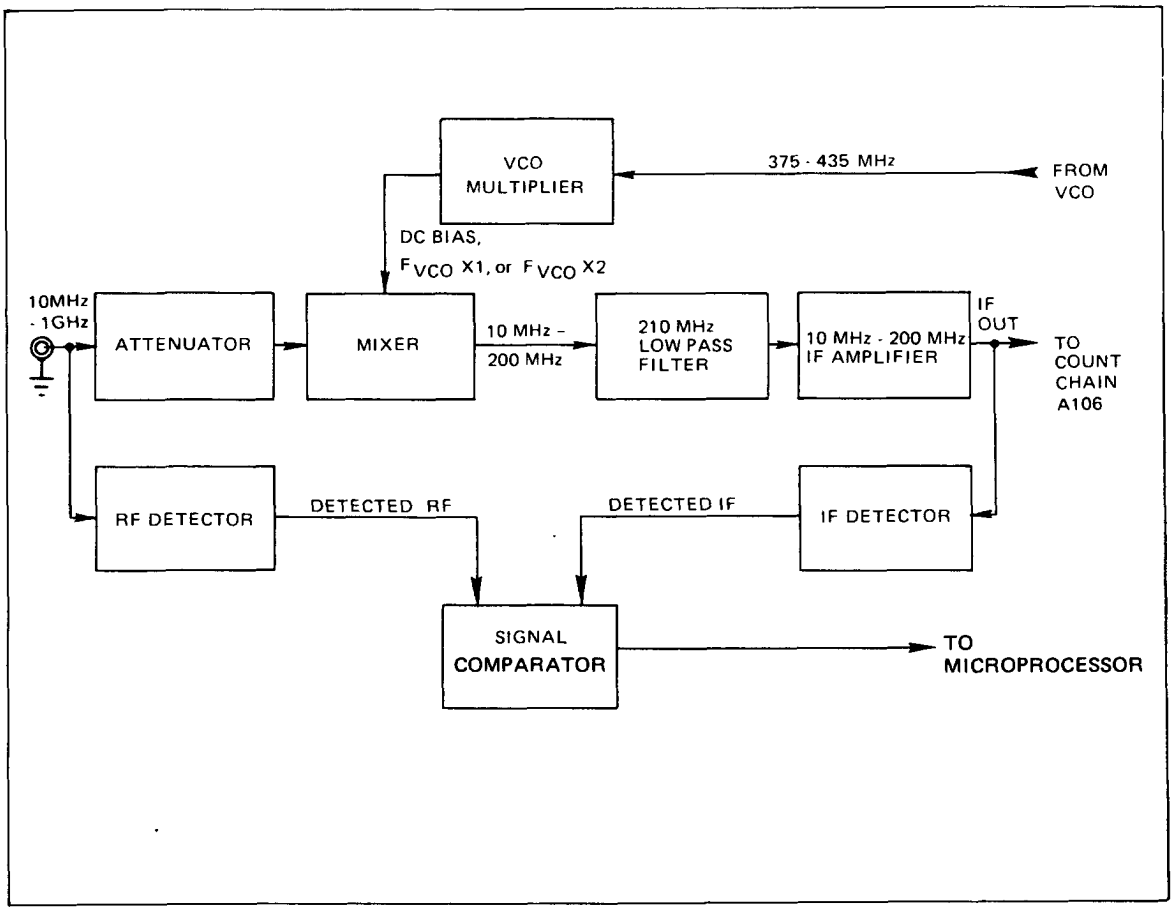


Figure 4-2 Band 2 Converter Block Diagram, Simplified

The output frequency of the system is the difference between the input signal and the L.O. applied to the mixer. Since the L.O. frequency is a harmonic (N) of the VCO frequency, the unknown input frequency can be expressed as $F_{IN}=N\ F_{VCO} \pm F_{IF}$. There are three primary functions of the software operating the converter:

- To select the appropriate harmonic number N.
- To select an appropriate VCO frequency.
- To determine whether the IF frequency is added to, or subtracted from the L.O. frequency.

These functions are accomplished by selecting N and F_{VCO} and looking for an IF signal of the appropriate amplitude and frequency. Overall system gain is such that whenever the correct L.O. frequency is applied, the IF power will exceed the RF power. This is the primary information used in determining the correct VCO frequency and harmonic number. Once an IF is obtained, the harmonic number is verified and the +/- sign in the equation is determined by shifting the VCO frequency and observing the magnitude and direction of the resulting IF shift. Converter operation is diagrammed in figure 4-3.

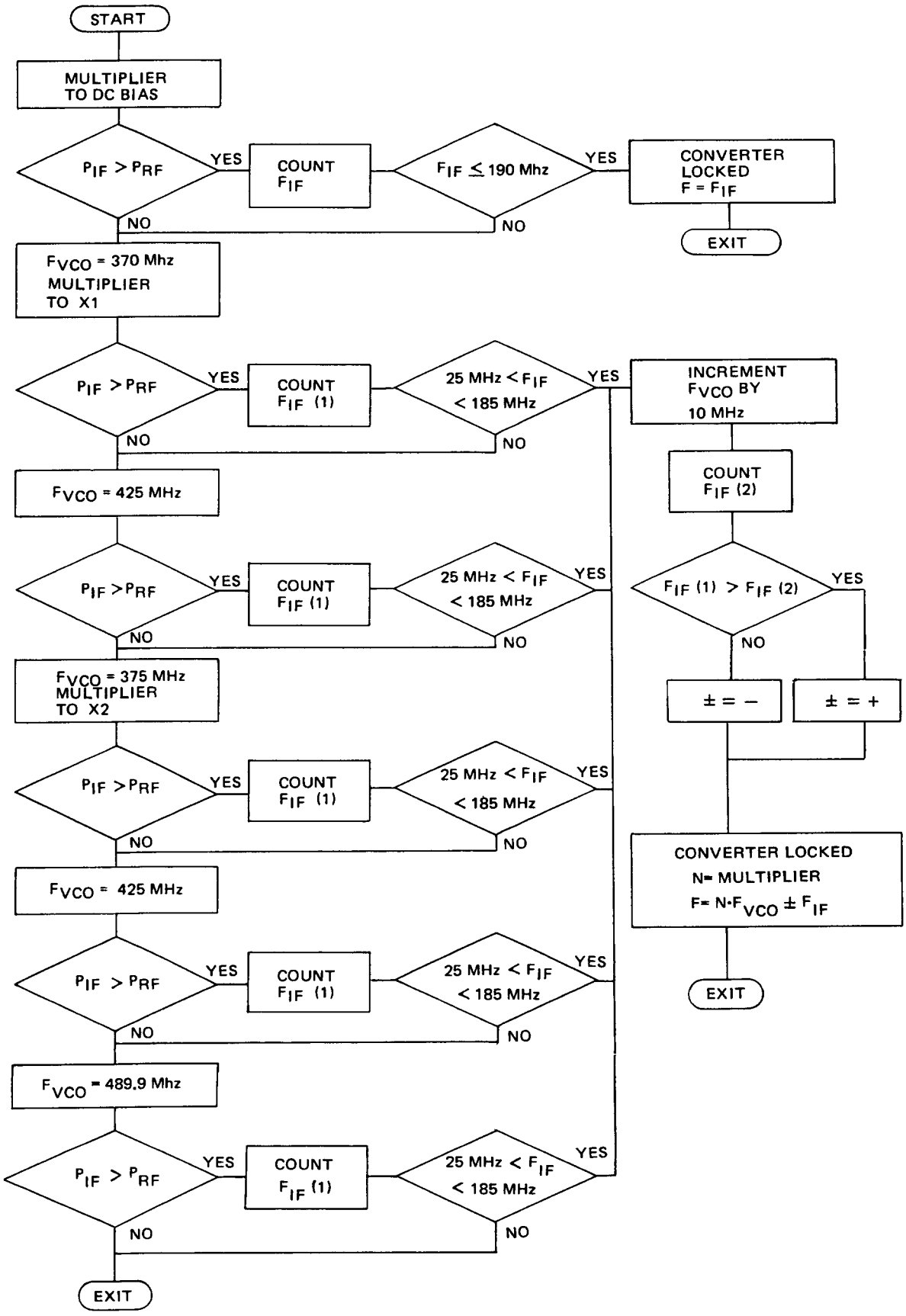


Figure 4-3. Band 2 Converter Operation

The L.O. frequencies being used, except the range of direct counting (< 190 MHz), have been selected so only IF frequencies from 25 MHz to 185 MHz are required. Since the counter can count signals less than 10 MHz, the restricted operating range provides margin for frequency modulation on the input signal, and for incrementing the VCO frequency.

Figure 4-4 shows the operating ranges for the various harmonics and VCO frequencies used.

Input Frequency Range F_{IN}(MHz)	VCO Frequency F_{VCO}(MHz)	Harmonic Number N	IF Frequency Range F_{IF}(MHz)
10 - 190	—	0	10 - 190
185 - 345	370	1	185 - 25
345 - 400	425	1	80 - 25
400 - 560	375	1	25 - 185
560 - 610	425	1	135 - 185
610 - 725	375	2	140 - 25
725 - 825	425	2	125 - 25
825 - 935	375	2	75 - 185
935 - 1035	425	2	85 - 185
1035 - 1164.8	489.9	2	55.2 - 185

Figure 4-4. Band 2 Operating Ranges

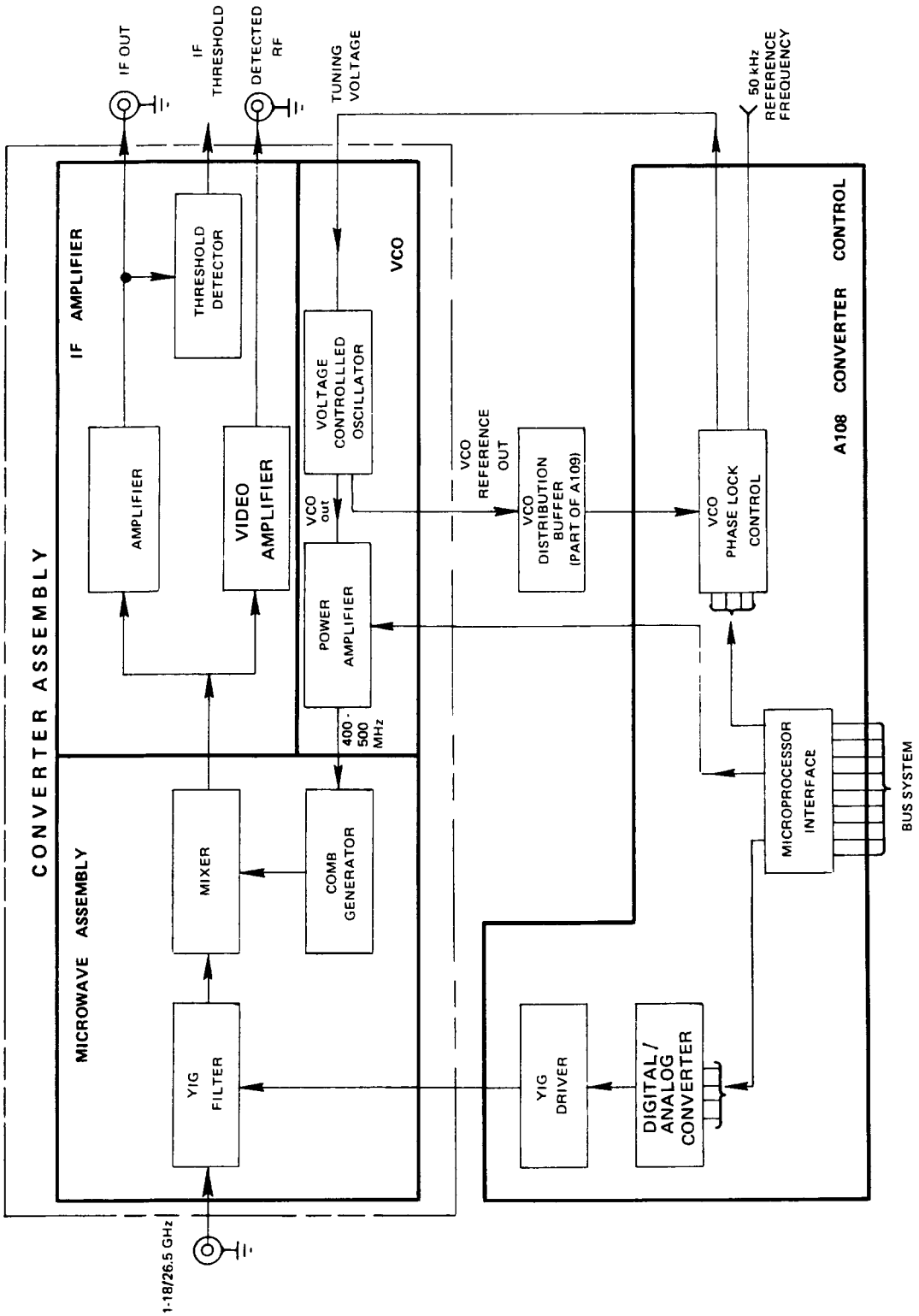


Figure 4-5 Band 3 Converter, Simplified.

BAND 3 CONVERTER

Measurement of a signal in Band 3 is accomplished by down converting from the microwave range to approximately 125 MHz. This is accomplished by mixing the input signal with a known reference frequency which is found by selecting a VCO harmonic in the range of 400 to 500 MHz. The VCO frequency can be selected in 50 KHz increments by using a microprocessor controlled phase lock system, while retaining the accuracy and stability of the counter's time base reference.

A simplified diagram of the Band 3 converter is shown in figure 4-5. There are two major assemblies. The Converter Control assembly (A108) and the Converter Assembly (A203).

CONVERTER CONTROL A108

The Converter Control assembly contains the interface between the microprocessor bus system and the Converter (A203). A digital-to-analog converter and a precision current (YIG) driver provide a 2 MHz frequency resolution for setting the YIG filter of A202.

A108 also contains the programmable VCO phase lock control system. This system lets the microprocessor interface select any VCO frequency between 400 and 500 MHz, in increments of 50 KHz.

CONVERTER A203

The Converter assembly consists of three subassemblies.

- A201A, Voltage Controlled Oscillator (VCO) Assembly
- A201B, IF Amplifier Assembly
- A202, Microwave Assembly (yig)

The A202 Microwave Assembly contains the YIG filter, mixer and comb generator.

The input signal (1 GHz - 18 GHz/26.5 GHz) passes through a YIG filter on A202. The filter is an electronically tunable bandpass filter, with an operating frequency proportional to its tuning current. This filter determines the approximate frequency of the input signal, and filters out any undesired signals, making it possible to count a signal at one frequency even if a larger signal is present at another frequency.

When tuning the YIG filter to the input signal, the mixer is used as an RF detector, and its output is amplified in the video amplifier on the IF assembly .

The output of the Video amplifier is maximum when the YIG filter is tuned to the input signal. In the case of multiple input signals, the video amplifier output determines which signal is largest.

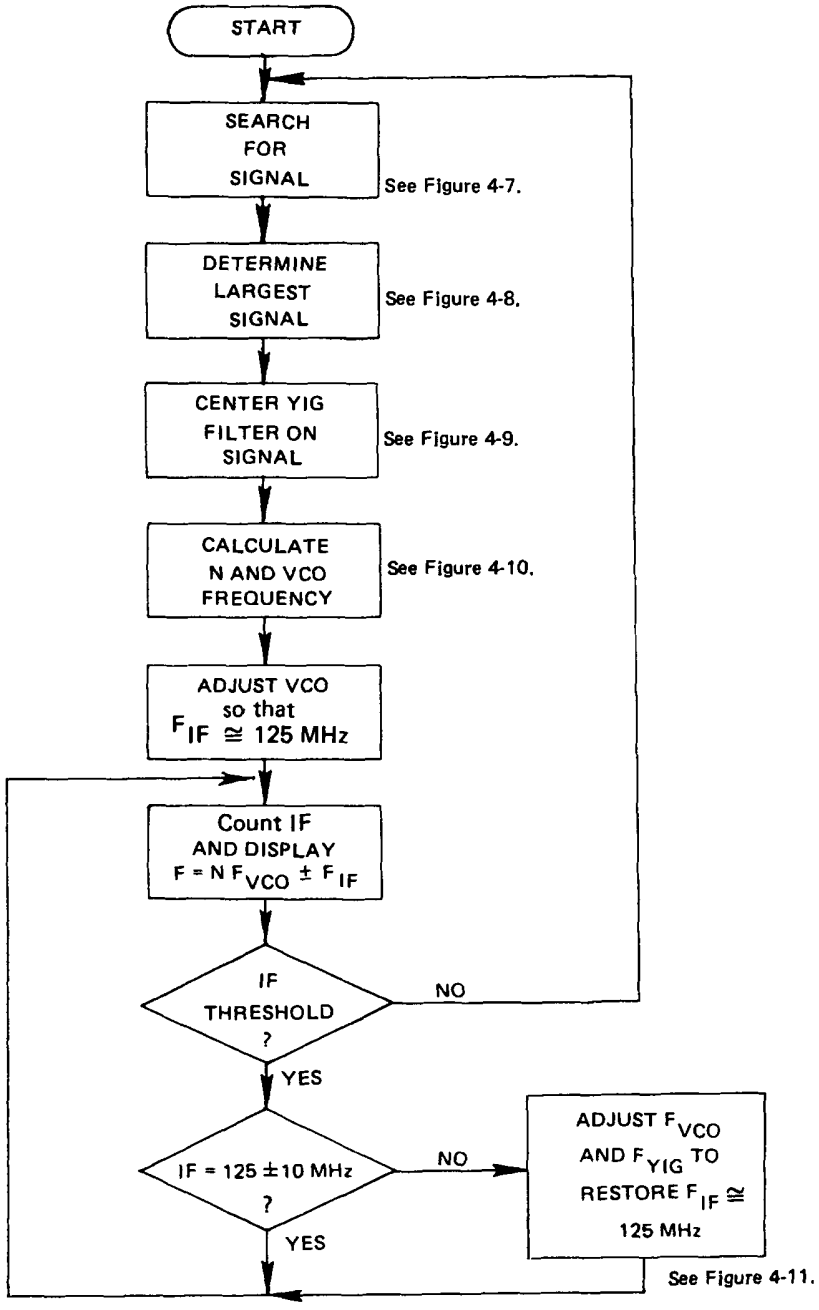


Figure 4-6. Band 3 Operation, Simplified.

On units equipped with the Power Measurement Option (02), accurate frequency correction factors are stored in the counter's memory. This allows absolute power calibration of the video amplifier output.

Once the YIG filter is tuned to the input signal, the appropriate harmonic number (N) and VCO frequency (F_{VCO}) are selected to produce an IF frequency (F_{IF}) at approximately 125 MHz. An approximation of the input signal is found by using:

$$F_{IN} = N F_{VCO} \pm F_{IF}$$

The IF frequency produced in the mixer is amplified by the high gain IF amplifier and sent to the count chain (A106). The IF threshold detector (A201B) insures sufficient IF amplitude for count accuracy.

OPERATION

First the YIG filter is stepped, (in 64 Mhz steps), from its low to high limits. During this search the RF detected output is fed, through a microprocessor controlled step attenuator to a threshold detector. After each step the threshold detector is checked. If triggered, the search mode is halted until the amplitude of the signal is determined. This is done by stepping the filter back and forth through the signal and stepping the attenuator until the signal is attenuated below the threshold. The counter then returns to the search mode to look for any larger signals. After searching the entire frequency range, it returns to the largest signal and begins to center the YIG filter precisely on the input frequency. See Figure 4-6 for a simplified diagram of Band 3 operation. For more detailed descriptions of Band 3 operation see Figures 4-7 through Figure 4-11.

The centering process consists of slowly stepping the YIG filter down (in 2 MHz increments) until a level of 3-6 dB below the peak is reached. This frequency is stored and the process is repeated from the other side by stepping the filter up in 2 MHz steps. The average of the two frequencies obtained is the center of the passband. This is the frequency which is used to determine the N and F_{VCO}.

After centering, N is determined from $N = \frac{F_{YIG} - 125}{500}$ and then rounded up to the next highest integer. From this, F_{VCO} is calculated using $F_{VCO} = \frac{F_{YIG} - 125.}{N}$. Should this yield $F_{VCO} < 400$ MHz, then F_{VCO} is recalculated using $F_{VCO} = \frac{F_{YIG} + 125.}{N}$.

Since F_{YIG} is only approximately equal to F_{IN}, the IF frequency will not be exactly 125 MHz. Therefore, the next step in operation is a VCO frequency adjustment to shift F_{IF} into the middle of the IF passband.

VCO frequency correction is achieved by counting F_{IF} and changing F_{VCO} by $\pm \frac{F_{IF} - 125.}{N}$. If the error is large enough to be outside the IF passband (IF threshold is not triggered) then a series of steps (shifting the IF in ± 20 MHz increments) are taken until the signal falls within the passband.

Once the VCO corrections have been made, the converter has acquired the signal and the counter is ready to count and display the input frequency.

After each measurement, the frequency of the IF is examined. If the input frequency has shifted more than 10 MHz, new frequencies for the YIG and VCO are calculated to restore the IF to 125 MHz. This method provides rapid tracking of a signal being tuned.

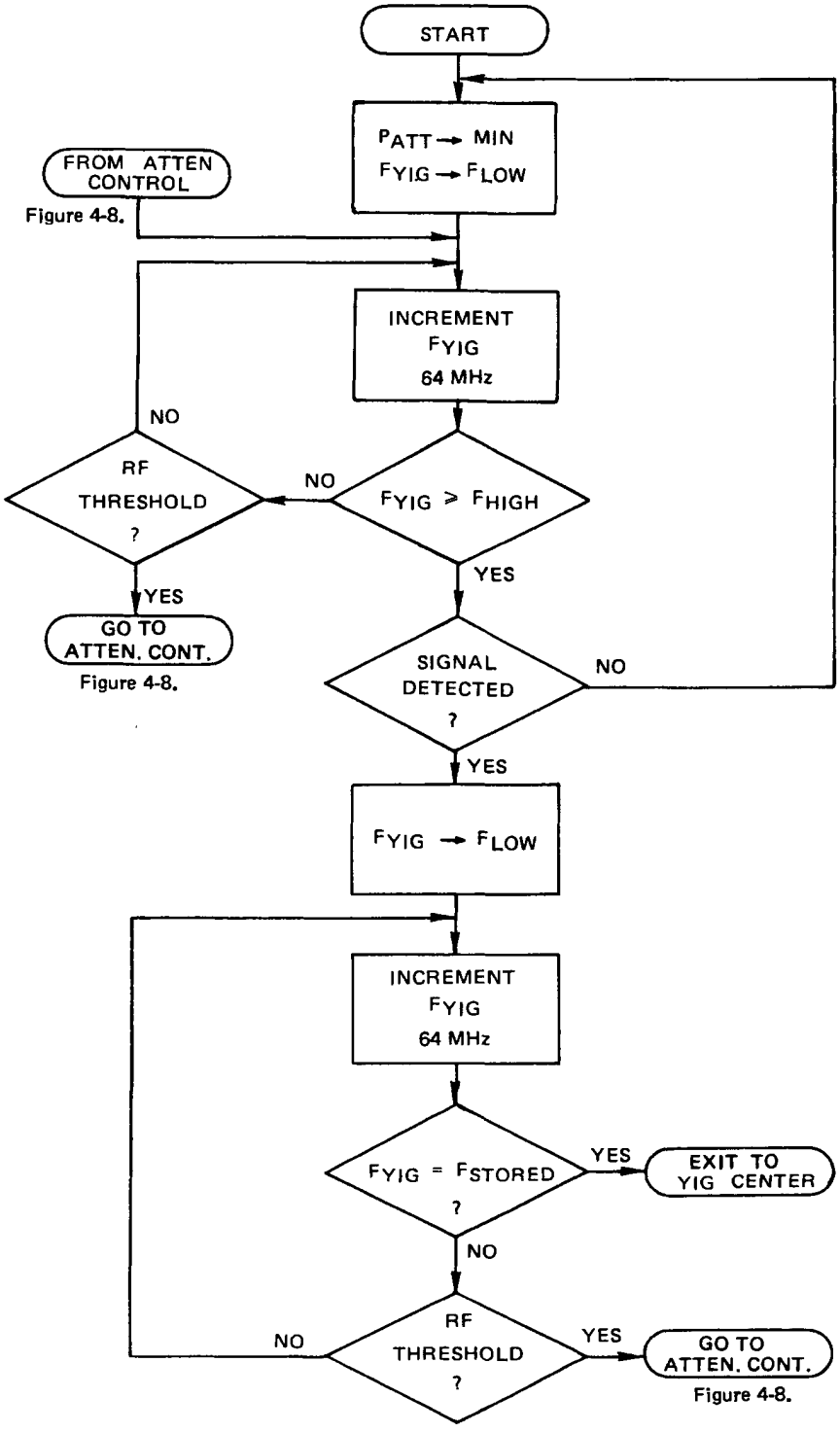


Figure 4-7. Band 3 Search For Signal

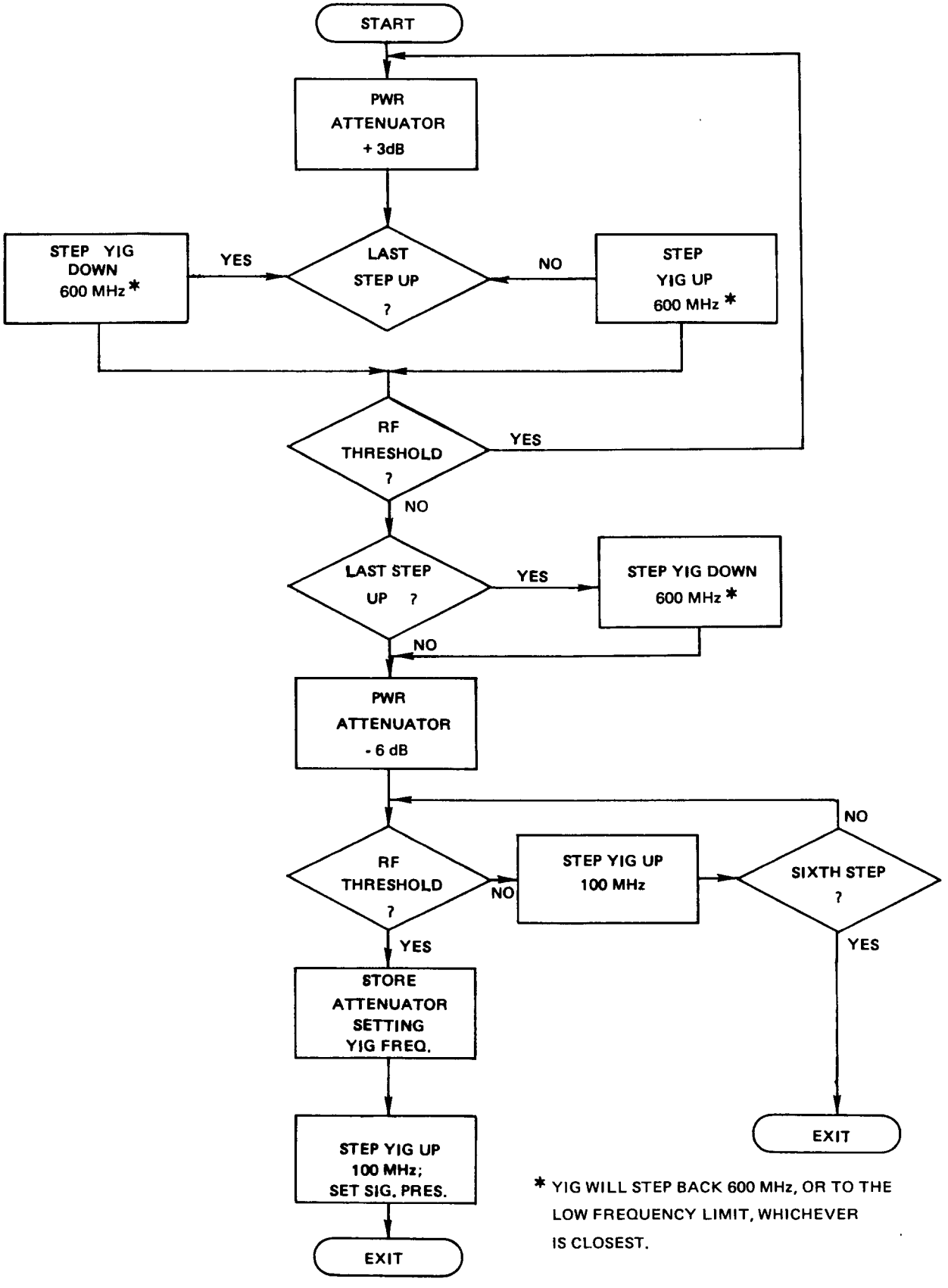


Figure 4-8. Determine Largest Signal

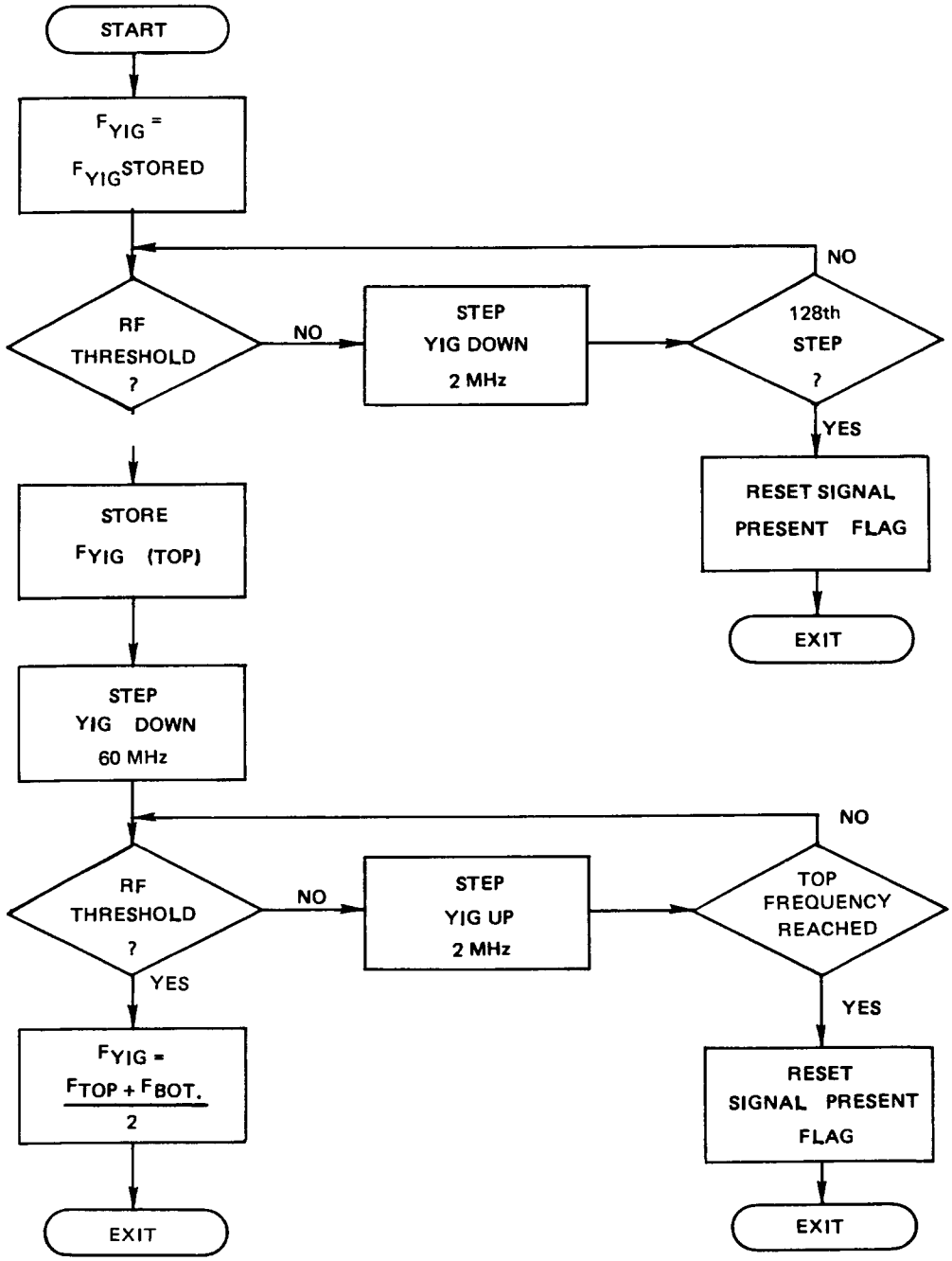


Figure 4-9. YIG Centering

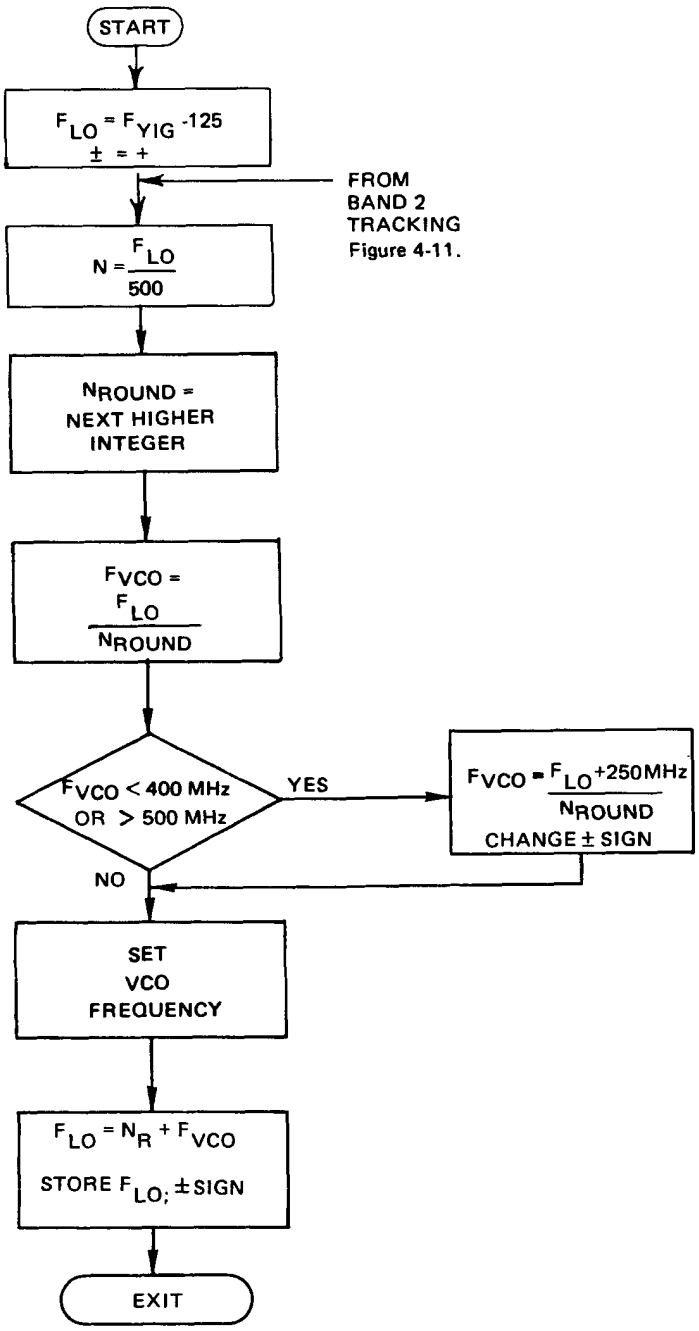


Figure 4-10. Calculate N and VCO Frequency

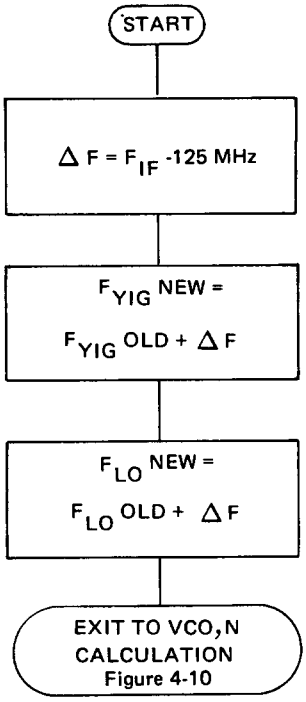


Figure 4-10

Figure 4-11. Band 3 Signal Tracking

Section 5
Maintenance and Service

This section contains instructions and information to maintain your counter.

FUSE REPLACEMENT

The counter uses one fuse. It is located on the rear panel next to the voltage select switch.

- For 100/120VAC operation use a 0.75A slow-blow MDL type fuse.
- For 220/240VAC operation use a 0.40A slow-blow FST type fuse.

The voltage select switch should be set to the proper line voltage. To change line voltage:

1. Be sure the counter is disconnected from the power line.
2. With a flat edged screwdriver, rotate the voltage select switch until the arrow points to the desired line voltage.
3. Change to a fuse with the value specified for the line voltage selected.

NOTE:
Always be sure that the fuse is the type and value specified for, and that the voltage select switch is set to correspond to the AC power input voltage, or the counter may be damaged.

AIR CIRCULATION

Air circulates through the vents in the rear panel of the counter. These vents must not be obstructed or the temperature inside the counter may increase enough to reduce the counter stability and shorten the component life.

PERIODIC MAINTENANCE

No periodic preventive maintenance is required. To maintain accuracy, it is recommended that the counter be recalibrated every six months.

CAUTION

Do not attempt repair or disassembly of the Microwave Converter or Time Base Oscillator Assemblies. Contact EIP or your sales representative.

If the following assemblies are repaired or replaced the counter may require recalibration for proper operation.

- Power Supply, A101
- Gate Generator, A107
- Converter Control, A108
- Microwave Converter, A203

Care should be taken when removing any assemblies to prevent damage to components or cables.

FACTORY

If the counter is being returned to EIP for service or repair, be sure to include the following information with the shipment.

- Name and address of owner.
- Model and complete serial number of counter.
- A COMPLETE description of problem (Under what conditions did problem occur? What was the signal level? What equipment was attached or connected to the counter? Did that equipment experience failure symptons?)
- Name and telephone number of someone familiar with the problem that may be contacted by EIP for any further information, if necessary.
- Shipping address to which the counter is to be returned. Include any special shipping instructions.
- Pack the counter for shipping (Refer to Section 2).

FIELD

EIP has an assembly exchange program. All plug in assemblies, modules, and the front panel assembly may be exchanged.

After identifying the faulty assembly, call EIP with the assembly number and shipping information. A replacement will be shipped within 24 hours. After the replacement assembly has been received, return the faulty assembly to EIP for credit.

Section 6
Troubleshooting

This section defines troubleshooting aids that are incorporated in the 545/548 counter. They are:

- Signature analysis
- Self diagnostics
- Keyboard controlled circuit tests

The procedures and tables are provided for troubleshooting to a functional circuit level.

SIGNATURE ANALYSIS

Signature analysis is a technique used to troubleshoot complex logic circuitry. It uses data compression to reduce any data pattern to a 4 character alpha-numeric word.

The start and stop inputs define the measurement window. Each time a transition within the measurement window occurs on the clock input, the probe is sampled, and the logic level is shifted into the analyzer. This information is used to generate a signature unique to that data string. That signature can then be compared to a reference signature, taken from a known good product, to determine if the data string is correct.The counter implements signature analysis in either a free running or program controlled manner.

FREE RUNNING

This mode of signature analysis is essential for troubleshooting problems that could prevent the program from running. A CLRB instruction can be forced by breaking the data bus at A105 SW1 and grounding A105 TP11, effectively "free running" the microprocessor. "Free running" means forcing a simple instruction (such as NOP or CLRB) on the data bus, which the microprocessor sees at every address location. This causes the microprocessor to continually cycle through its entire address range, accessing everything on the address bus as it does. By strategically placing the start and stop connections the entire bus system can be probed for bad signatures. Figures 6-1 through 6-7 reflect the signatures at the "L" revision. For later revision levels of the software please refer to the manual change sheet.

	START	STOP	CLOCK
CONNECTIONS	A105 TP5	A105 TP5	A105 TP2
BUTTONS	IN ↓	IN ↓	IN ↓

LINE	SIGNATURE	LINE	SIGNATURE
A0 (P1 Pin 54)	UUUU	U2 Pin 9	75HA
A1 (P1 Pin 53	FFFF	U3 Pin 12	75HA*
A2 (P1 Pin 52)	8484	U4 Pin 4	75H9
A3 (P1 Pin 51)	P763	U9 Pin 15	CA13
A4 (P1 Pin 50)	1U5P	U9 Pin 14	H75C
A5 (P1 Pin 49)	0356	U9 Pin 13	A3UU
A6 (P1 Pin 48)	U759	U9 Pin 12	AA68
A7 (P1 Pin 47)	6F9A	U9 Pin 11	A713
A8 (P1 Pin 46)	7791	U9 Pin 10	S4F7
A9 (P1 Pin 45)	6321	U9 Pin 9	6039
A10 (P1 Pin 44)	37C5	U9 Pin 7	826H
A11 (P1 Pin 43)	6U28	A15 (U4 Pin 8)	0002
A12 (P1 Pin 42)	4FCA	A14 (U4 Pin 10)	9UP2
A13 (P1 Pin 41)	4868	U3 Pin 8	755P
A14 (P1 Pin 40)	9UP1	U4 Pin 6	755H
A15 (P1 Pin 39)	0001		

+ 5V 0003 phase 0003*

* Due to the sycronous qualities of the signature analyzer , phase 2 will read the same as +5V but the logic probe will be flashing. Likewise anything gated with phase 2 may have the same signature as the ungated signal (U2 Pin 9 and U3 Pin 12).

Figure 6-1. Microprocessor Free Running Signatures

	START	STOP	CLOCK
CONNECTIONS	A105 U7 Pin 20	A105 U11 Pin 20	A105 TP2
BUTTONS	IN ↓	OUT ↑	IN ↓

NODE	SIGNATURE	NODE	SIGNATURE
A105 S1 Pin 9	32F2	A105 S1 Pin 13	50U8
A105 S1 Pin 10	07H9	A105 S1 Pin 14	4343
A105 S1 Pin 11	C5A0	A105 S1 Pin 15	8H7C
A105 S1 Pin 12	C7F2	A105 S1 Pin 16	7F7P
+ 5V CCPC			

Figure 6-2. Signatures, Basic PROM Set

	START	STOP	CLOCK
CONNECTIONS	A105 U7 Pin 20	A105 U7 Pin 20	A105 TP2
BUTTONS	IN ↓	OUT ↑	IN ↓

NODE	SIGNATURE	NODE	SIGNATURE
A105 S1 Pin 9	A88A	A105 S1 Pin 13	C068
A105 S1 Pin 10	A544	A105 S1 Pin 14	C7UP
A015 S1 Pin 11	3C26	A105 S1 Pin 15	F0H7
A105 S1 Pin 12	9F38	A105 S1 Pin 16	P2FA
+ 5V 826P			

Figure 6-3. Signature, U7 PROM 3

	START	STOP	CLOCK
CONNECTIONS	A105 U6 Pin 20	A105 U6 Pin 20	A105 TP2
BUTTONS	IN ↓	OUT ↑	IN ↓

NODE	SIGNATURE	NODE	SIGNATURE
A105 S1 Pin 9	H81A	A105 S1 Pin 13	2367
A105 S1 Pin 10	4352	A105 S1 Pin 14	240U
A105 S1 Pin 11	57UH	A105 S1 Pin 15	P892
A105 S1 Pin 12	256A	A105 S1 Pin 16	94AF
+ 5V 826P			

Figure 6-4. Signatures, U6 PROM 4

	START	STOP	CLOCK
CONNECTIONS	A105 U13 Pin 20	A105 U13 Pin 20	A105 TP2
BUTTONS	IN ↓	OUT ↑	IN ↓

NODE	SIGNATURE	NODE	SIGNATURE
A105 S1 Pin 9	3818	A105 S1 Pin 13	4UCH
A105 S1 Pin 10	3626	A105 S1 Pin 14	5376
A105 S1 Pin 11	UA26	A105 S1 Pin 15	6U31
A105 S1 Pin 12	6A22	A105 S1 Pin 16	4C0F
+ 5V 826P			

Figure 6-5. Signatures, U13 PROM 5

	START	STOP	CLOCK
CONNECTIONS	A105 U12 Pin 20	A105 U12 Pin 20	A105 TP2
BUTTONS	IN ↓	OUT ↑	IN ↓

NODE	SIGNATURE	NODE	SIGNATURE
A105 S1 Pin 9	F459	A105 S1 Pin 13	4P95
A105 S1 Pin 10	07F5	A105 S1 Pin 14	C462
A105 S1 Pin 11	485U	A105 S1 Pin 15	C0HP
A105 S1 Pin 12	3AU8	A105 S1 Pin 16	C99A
+ 5V 826P			

Figure 6-6. Signatures, U12 PROM 6

	START	STOP	CLOCK
CONNECTIONS	A105 U11 Pin 20	A105 U11 Pin 20	A105 TP2
BUTTONS	IN ↓	OUT ↑	IN ↓

NODE	SIGNATURE	NODE	SIGNATURE
A105 S1 Pin 9	9UA5	A105 S1 Pin 13	P8C4
A105 S1 Pin 10	6C99	A105 S1 Pin 14	P17F
A105 S1 Pin 11	4H5U	A105 S1 Pin 15	8822
A105 S1 Pin 12	201A	A105 S1 Pin 16	14F9
+ 5V 826P			

Figure 6-7. Signatures, U11 PROM 7

PROGRAM CONTROLLED

If the counter is working sufficiently to access the test functions, program controlled signature analysis can be used. In program controlled signature analysis the start and stop (and therefore the signature) are controlled by software. This allows the signature anlayzer to be used, in many cases, to troubleshoot the hardware outside the bus system.

SELF DIAGNOSTICS

At turn on the counter performs several internal diagnostic checks, checking ram, prom, and the associated decoding circuitry. The displays shows dashes during these checks. If the counter passes the tests it then enters the normal operating mode. If it fails ram check the display will show all E's and a unique signature will be generated. If the counter fails any of the prom checks an error message will be displayed, and a signature will be generated. Please refer to figure 6-8.

	STOP	START	CLOCK	PROBE
CONNECTION	A106 TP5	A106 TP5	A105 TP2	A105 TP12 (+ 5V)
BUTTONS	OUT ↑	IN ↓	IN ↓	

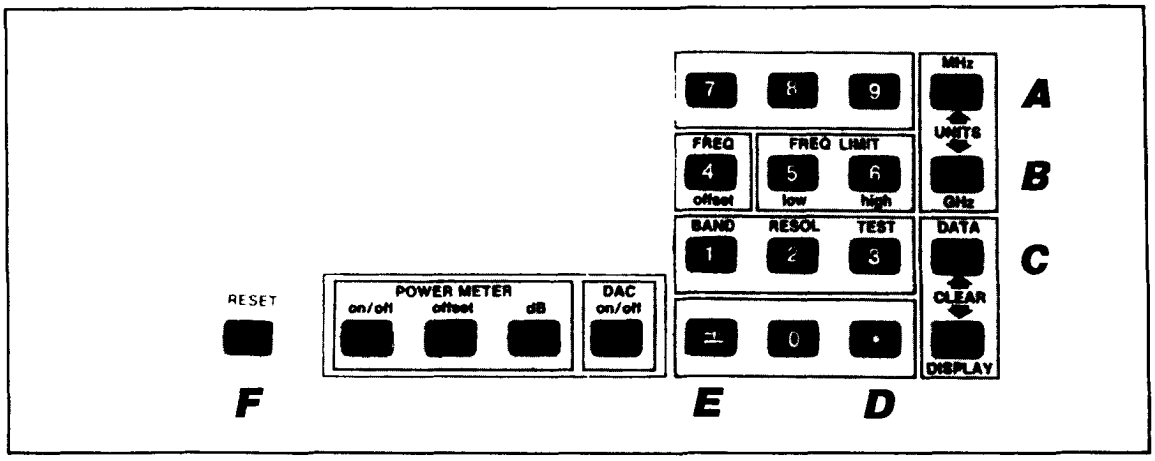
PROBLEM	ERROR SIGNATURE	
Ram Bad	All E's	007U
Prom 1 (A105 U20) Bad	31	1UFP
Prom 2 (A105 U8) Bad	32	P390
Prom 3 (A105 U7) Bad	33	P673
Prom 4 (A105 U6) Bad	34	PFP8
Prom 5 (A105 U13) Bad	35	6A6U
Prom 6 (A105 U12) Bad	36	8AF9
Prom 7 (A105 U11) Bad	37	P340
* Prom 8 (A107 U2) Bad	38	825P

*Error 38 can only occur if the counter is configured for the power meter option, 02.

Figure 6-8. Self Diagnostic Error Indications

KEYBOARD CONTROLLED CIRCUIT TESTS

There are ten keyboard controlled circuit tests (01 thru 10). All tests are accessed by pressing TEST and then the two digit test number. Tests which do not require keyboard inputs to function (tests 01, 02, 03, 04, 05, 06, 07) can be exited by pressing any key. The counter will exit the test and enter the functions selected. Tests which use the keyboard in their operation (tests 05, 08, 09, 10) can be exited by pressing any key not used by the test. All tests can be exited by pressing CLEAR DISPLAY. The counter will return to normal operation. Some tests require hexidecimal coded keyboard inputs (tests 08, 09, 10). For those tests the keyboard is defined in figure 6-3.



KEY	HEX EQUIV.	KEY	HEX EQUIV.
0	0	9	9
1	1	MHz	A
2	2	GHz	B
3	3	CLR DATA	C
4	4		
5	5	•	D
6	6	+/–	E
7	7	RESET	F
8	8	CLR DISPLAY	EXITS TEST

Figure 6-3. Keyboard Configuration For Tests Requiring Hexidecimal Inputs.

	START	STOP	CLOCK	PROBE
CONNECTION	OUT ↑	IN ↓	IN ↓	
BUTTONS	A106 TP5	A106 TP5	A105 TP2	A105 TP12 (+ 5V)

BUTTON	COORDINATES	SIGNATURE
Reset	47	U68C
Power ON/OFF	46	U7HA
Power Offset	36	20P6
dB	16	U2F9
DAC	26	811P
7	41	A19C
8	42	66PU
9	43	CCH7
MHz	44	U5PU
4	31	PUPH
5	32	UC70
6	33	HF3A
GHz	34	UPA2
1	21	APH1
2	22	C45H
3	23	1766
CLR DATA	24	H9C8
+/–	11	375U
0	12	H7PC
•	13	UAHH
CLR DISPLAY	EXIT TEST	C75U

Figure 6-10. Keyboard Test Signatures.

TESTS

01 **200 MHz Self Test** This test sets the VCO to 400 MHz, divides it by two, and counts the 200 MHz output from the divider. It checks the count chain, VCO and VCO phase lock circuitry, and the gate generator.

02 **8's Test** This will light all LED's, annunicators, and decimal points. It checks that everything on the display is lit, the intensity of the display, and the alignment of the LED's and annunciators.

03 **Display Segment Test** This lights one segment of each digit, and one annunciator at a time, cycling through all segments. The cycle rate can be adjusted with the sample rate pot. It verifies that each segment of the display, segment drivers and display multiplexer, operate properly and independently.

04 **Display Digit Test** This lights one entire digit, and its decimal point, at a time. It cycles through all digits and annunciators. The cycle rate is determined by the sample rate pot. It checks each digit and digit driver independently, and verifies operation of the display multiplexer.

05 **Keyboard Test** This will display the coordinates of each key as it is pressed. It also generates a unique signature for each key, so the keyboard can be checked without the display. Test 05 may be entered by keyboard or by momentarily tying A108 TP1 to A105 TP2 (or to A108, U5, pin 25). This makes it possible to enter the keyboard test for troubleshooting even if the keyboard is not operating well enough to enter the test in a normal manner. Test 05 checks the keyboard, keyboard interrupt, and keyboard decode circuitry. The coordinates and signatures for each key are shown in figure 6-10.

06 **Converter Ramp Test** Test 06 continuously ramps the Band 3 Converter DAC from 0 to 27 GHz, in 2 MHz (LSB). It also generates a signature for each of the inputs to the DAC. (See figure 6-11). It can be used to test the yig DAC, yig drivers, yig, and Band 3 RF level circuits.

	START	STOP	CLOCK	PROBE
CONNECTIONS	A106 TP5	A106 TP5	A105 TP2	A105 TP12 (+5V)
BUTTONS	OUT ↑	IN ↓	IN ↓	

NODE	SIGNATURE	NODE	SIGNATURE
A108 U5 Pin 2	2694	A108 U5 Pin 9	077F
A108 U5 Pin 3	8792	A108 U5 Pin 10	A3H5
A108 U5 Pin 4	5287	A108 U5 Pin 11	28PU
A108 U5 Pin 5	P082	A108 U5 Pin 12	7180
A108 U5 Pin 6	P588	A108 U5 Pin 13	U577
A108 U5 Pin 7	2HU2	A108 U5 Pin 14	F979
A108 U5 Pin 8	UPFO	A108 U5 Pin 15	7823
+ 5V	8142		

Figure 6-11. Converter Ramp Test Signatures

07 **GPIB Address Test** This test will display the decimal address of the GPIB option. If a GPIB option does not exist, test 07 will display a non valid address.

08 **Power Meter Offset Test** This makes it possible to set the power meter zero DAC to any setting. The setting is entered as a four digit hexidecimal number (figure 6-9). The first two digits are used to program the course offset DAC, and the last two digits program the fine offset DAC. Test 08 enables the power meter zero DAC to be tested, and can provide a DC level signal to aid in testing the power meter circuit.

09 **Power Meter Gain Test** This makes it possible to set the power meter sensing circuit to any number. The number is entered as a five digit hexidecimal number (figure 6-9) in the following format.

1st digit	A107 U10 bits 4-7
2nd digit	A107 U10 bits 0-3
3rd digit	A107 U12 bits 4-7 (Power Meter Option only)
4th digit	A107 U12 bits 0-3 (Power Meter Option only)
5th digit bit 0	Sets Amp marked "15 dB Gain" to high gain
5th digit bit 1	Sets Amp marked "30 dB Gain" to high gain

Digit 5 is a 2 bit number, so any number entered for digit 5 will be justified to a number from 0-3. Test 09 checks the RF level and power meter circuits.

10 **Information Read/Alter Routine** Test 10 can read any microprocessor address and, if that address is RAM or I/O, change its contents. The desired address is entered as a 4 digit hexidecimal number (see figure 6-9). When the 4th digit is entered the counter will display the contents of the desired address. The contents are then changed by entering a two digit hexidecimal number.

NOTE

Test 10 can change any temporary storage in the counter, including locations that are essential to the operation of the counter. Changing the wrong location will not damage the counter permanently, but it can cause improper operation. To return the counter to proper operation turn the counter off then back on.

SIGNIFICANT ADDRESSES, I/O PORTS

If an I/O bit is configured as an output, the number read by test 10 will be the same number that is programmed. If an I/O bit is configured as an input, the number read by test 10 will be the input signal level on the I/O line. Therefore, if an I/O port is programmed, and then read, the number displayed may not correspond to the number programmed because some bits of the I/O port may be configured as inputs.

DESCRIPTION	ADDRESS OF PA PORTS	ADDRESS OF PB PORTS
PIA on Count Chain (A106)	AC00	AC02
PIA on Gate Generator (A107)	9900	9902
Frequency Control PIA on Converter Control A108	9840	9842
Programmable Counter PIA on Converter Control (A108)	9820	9822
PIA on Band 2 Converter (A109)	9880	9882
PIA on Front Panel Logic (A111)	9808	980A
PIA on BCD/Remote (A102)	9A00	9A02
PIA on DAC Board (A103)	A820	A822

DESCRIPTION	ADDRESS
GPIB Address Switch	9C04

Figure 6-12. I/O Addresses.

Two important I/O port locations are the yig frequency control (address 9840, 9842) and the VCO frequency control (address 9820, 9822).

To convert from the desired yig frequency to the PIA program number :

1. Round the desired frequency to a multiple of 2 MHz (The yig DAC resolution is 2 MHz).
2. Divide the desired frequency in MHz by 2 (F/2).
3. Convert F/2 from decimal to hexidecimal.
4. The two most significant digits are programmed to address 9842, and the two least significant digits are programmed to address 9840.

To convert from the desired VCO frequency to the PIA program number :

EXAMPLE (420. 75 MHz)

1. Round the desired frequency to a multiple of 50 KHz (The resolution of the VCO frequency is 50 KHz).
2. Multiply the desired frequency (in MHz) by 5.....420. 75 X 5 = 2103. 75
3. If the result contains no fractional part, go to step 8.
4. Multiply only the fractional part by 16.....75 X 16 = 12
5. Add the result to the most significant digit from step 2.....MSD of 2103. 75 = 2 - 2 + 12 = 14
6. Convert the result to hexidecimal.....$14_{10} = E_{16}$
7. Replace the MSD from step 2 with the result from step 6 and drop the fractional part.....2103. 75 → E103
8. The two most significant digits are programmed to address 9822, and the two least significant digits are programmed to address 9820.

SIGNIFICANT ADDRESSES, RAM

All frequency storage registers in RAM are in the following format.

ADDRESS	SIGN	100 GHz
ADDRESS + 1	10 GHz	1 GHz
ADDRESS + 2	100 MHz	10 MHz
ADDRESS + 3	1 MHz	100 KHz
ADDRESS + 4	10 KHz	1 KHz
ADDRESS + 5	100 Hz	10 Hz
ADDRESS + 6	1 Hz	

For the sign digit:
8 = minus
0 = plus

REGISTER	ADDRESS
L.O. frequency	0140
I.F. frequency	01D2
Frequency output to display	0149
Frequency limit low (local)	0218
Frequency limit low (remote)	01F5
Frequency limit high (local)	0211
Frequency limit high (remote)	01EE
Frequency offset (local)	0203
Frequency offset (remote)	01E0

Figure 6-13. RAM Frequency Storage.

All power storage registers are in the following format.

ADDRESS	SIGN	
ADDRESS + 1		
ADDRESS + 2		
ADDRESS + 3		
ADDRESS + 4		100 dB
ADDRESS + 5	10 dB	1 dB
ADDRESS + 6	.1 dB	

For the sign digit:
8 = minus
0 = plus

RESISTER	ADDRESS
Power output to display	0150
Power offset (local)	020A
Power offset (remote)	01E7

Figure 6-14. RAM Power Storage.

TROUBLESHOOTING TREES

Troubleshooting trees are intended only as a guide, and do not describe every possible failure situation. Turn power off before removing or installing any P.C. boards or connectors. If the following assemblies are repaired or replaced, recalibration of the counter will be necessary.

- A101 Power Supply
- A107 Gate Generator
- A108 Converter Control
- A203 Converter Assembly

CAUTION

Do not attempt to repair or disassemble
the A203 hybrid assembly.

MANUFACTURER	MODEL	DESCRIPTION	CRITICAL PARAMETERS
Tektronix	475	Oscilloscope	100 MHz min. Bandwidth
Fluke	8050A	D.V.M.	4½ digit resolution
H.P.	182C, 8559A	Spectrum Analyzer	125 MHz
H.P.	5004A	Signature Analyzer	
H.P.	651B	Signal Generator	10 Hz - 10 MHz
Wavetek	2002	Sweeper	10 MHz - 2 GHz
Wiltron	610D, 6237D	Microwave Sweeper	2 GHz - 18 GHz
H.P.	8690A, 8696A	Microwave Sweeper	18 GHz - 26. 5 GHz

Figure 6-15. Troubleshooting Test Equipment Required

To use the troubleshooting trees:

1. Refer to the main troubleshooting tree.

2. Step through the main troubleshooting tree, performing all necessary checks, until the failure mode is noted.

3. Refer to the appropriate troubleshooting tree for that failure mode.

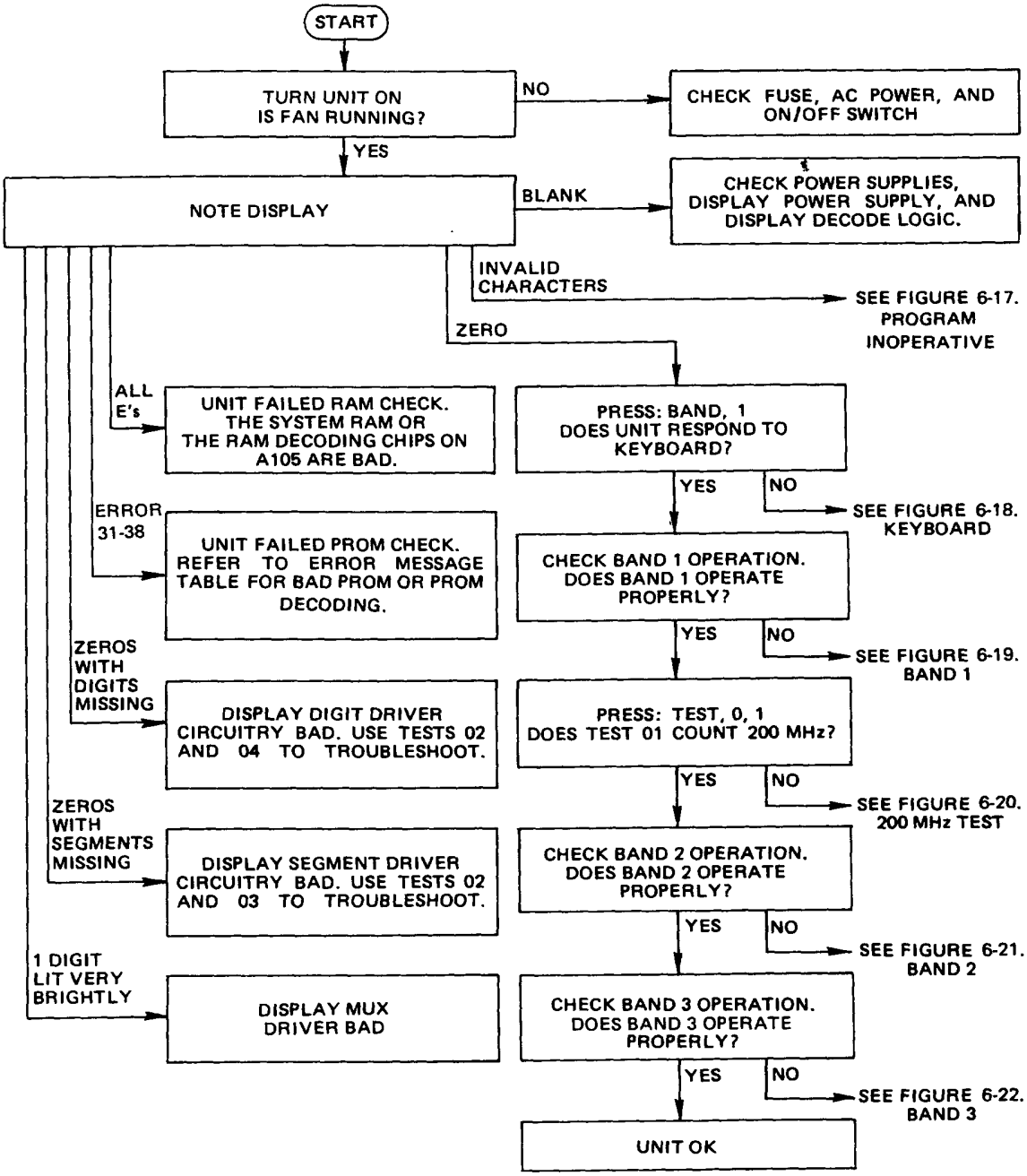


Figure 6-16. Main Troubleshooting Tree

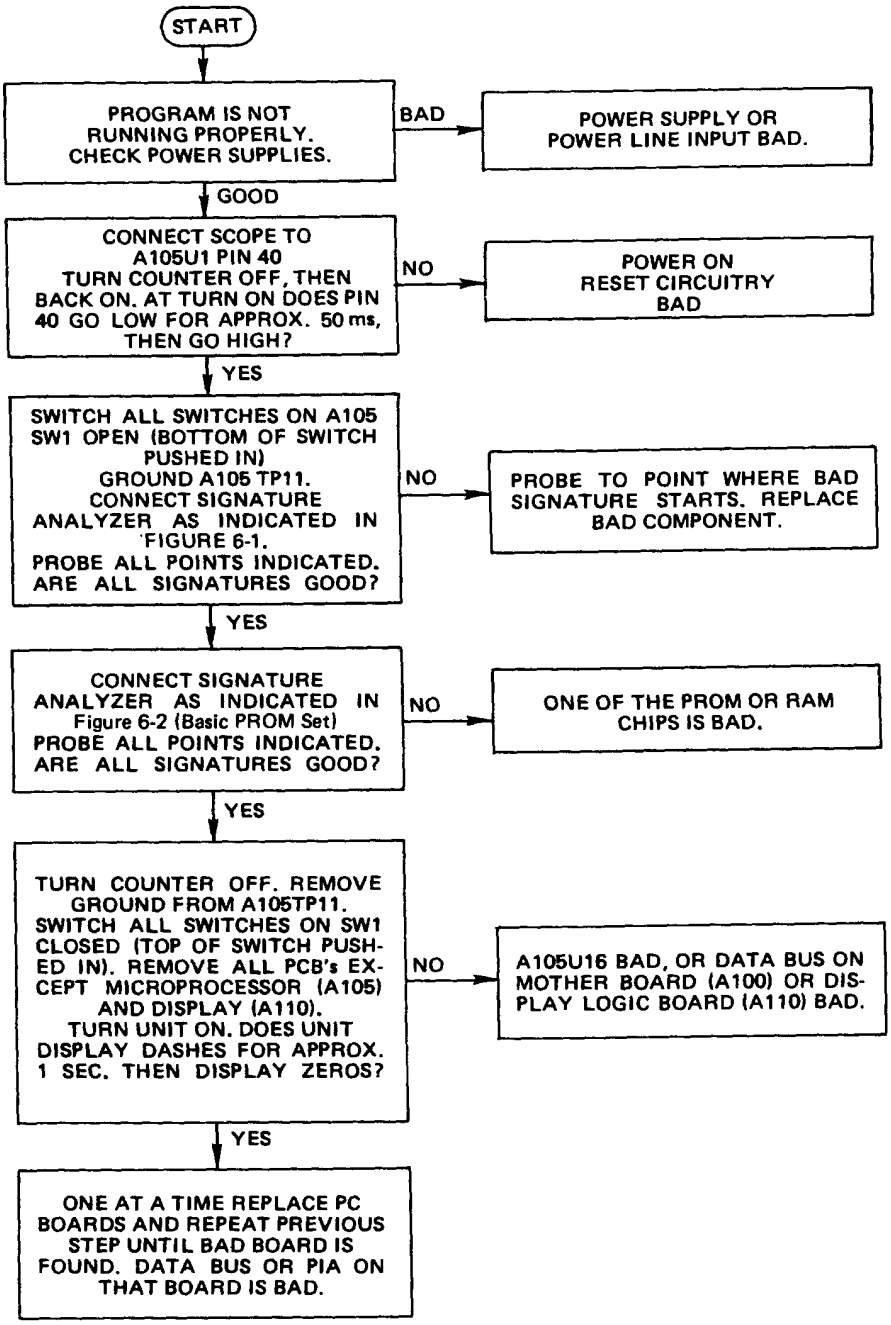


Figure 6-17. Program Inoperative

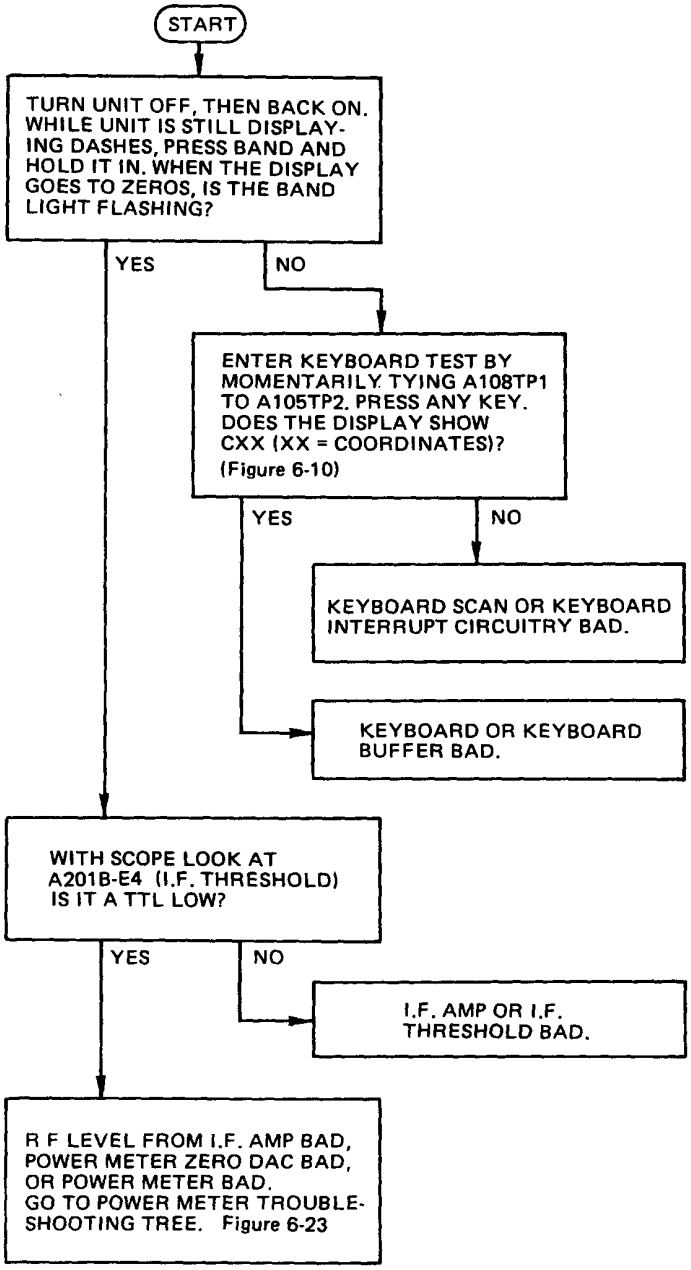


Figure 6-18. Keyboard

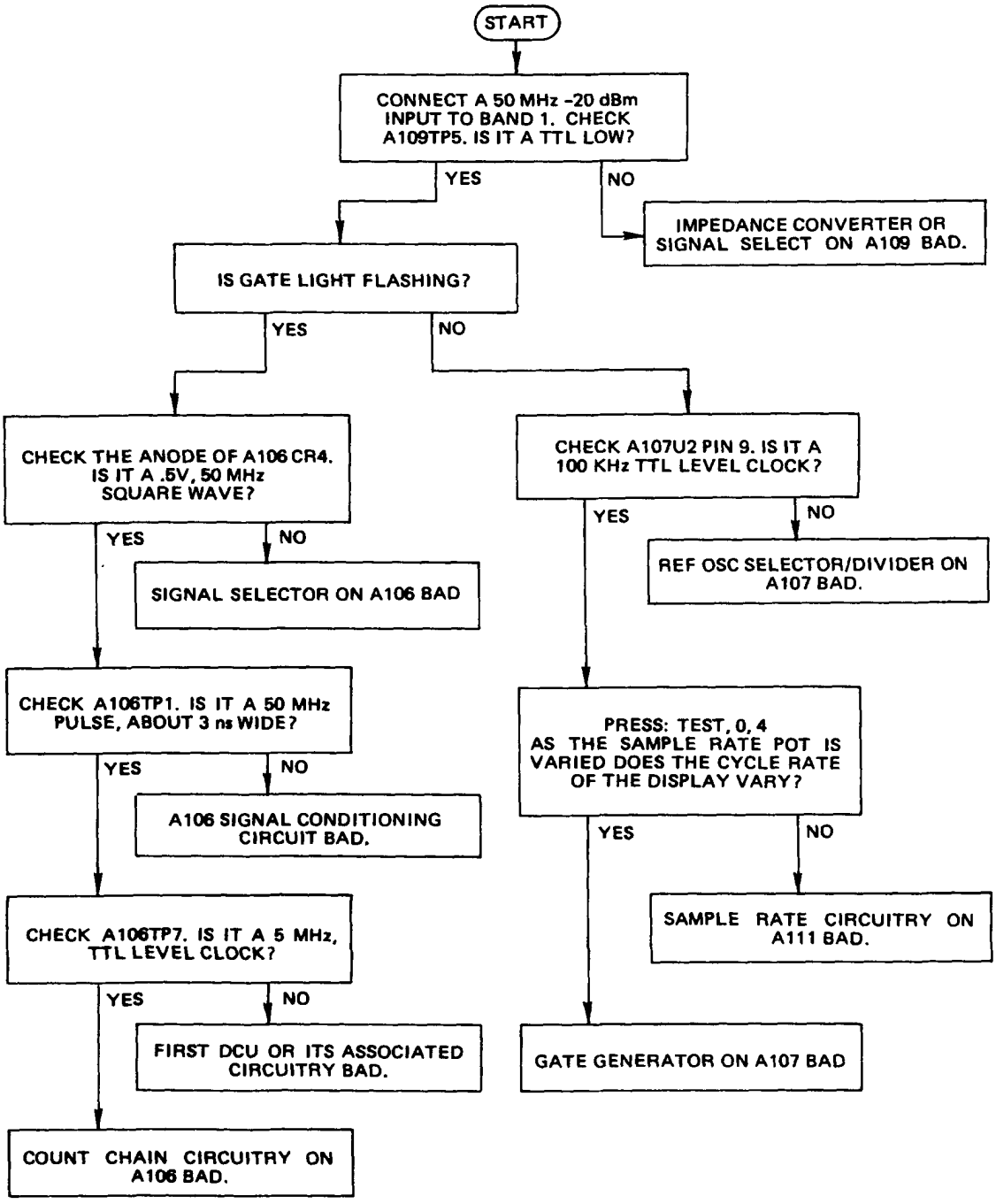


Figure 6-19. Band 1

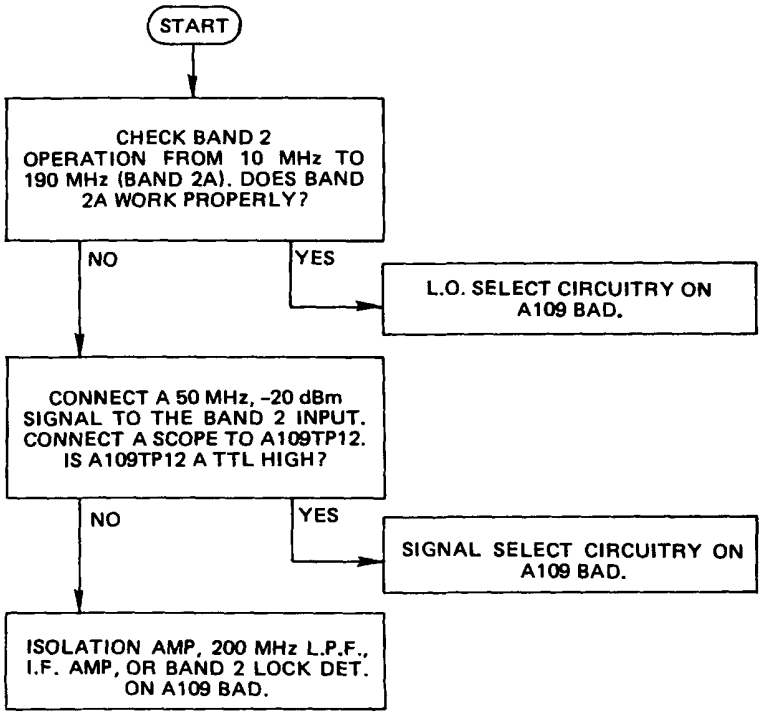


Figure 6-20. 200 MHz Test

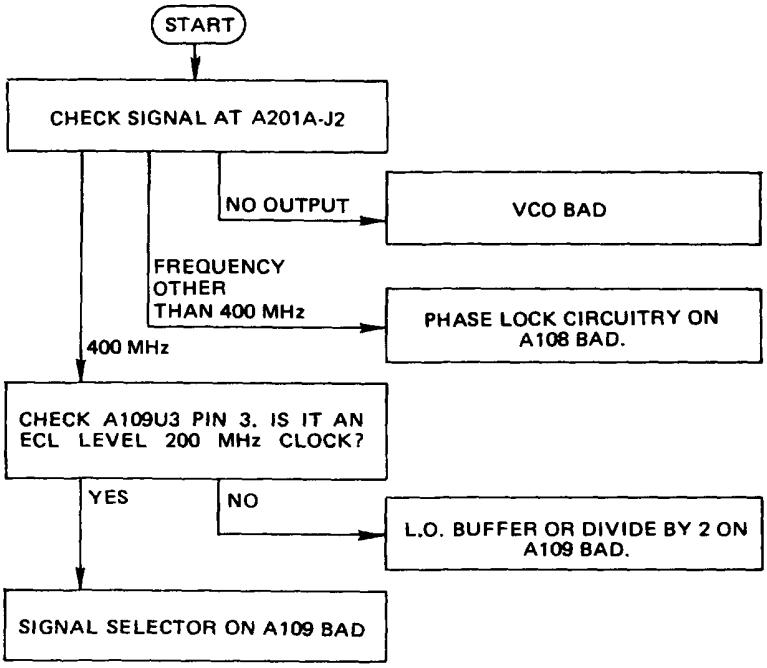


Figure 6-21. Band 2

START

WHAT IS SYMPTOM OF BAND 3 PROBLEM?

UNIT COUNTS WRONG NUMBER

VCO IS GENERATING WRONG FREQUENCY. CONNECT CONVERTER TO A109J2. (VCO REF.) IS FREQUENCY BETWEEN 400 MHz AND 500 MHz? AND STABLE?

YES

Ø LOCK CIRCUITRY ON A108 BAD.

NO

VCO NOT Ø LOCKED. CONNECT A POWER SUPPLY TO A201J3. VARY VOLTAGE FROM -2 TO +9V. DOES THE VCO FREQUENCY VARY FROM APPROX. 370 MHz TO APPROX. 510 MHz?

YES

Ø LOCK CIRCUITRY ON A108 BAD.

NO

VCO BAD

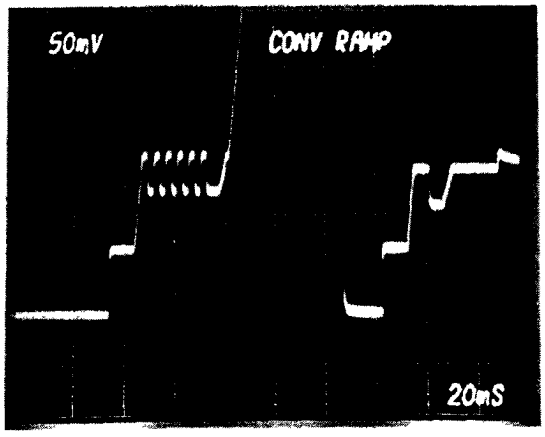


PHOTO A.

UNIT COUNTS AFTER SIGNAL IS REMOVED

I.F. THRESHOLD BAD

UNIT DOES NOT COUNT

WITH NO SIGNAL INTO THE COUNTER, CONNECT A SCOPE TO A100J7 PIN 2. DOES IT CONTAIN A 60 ms RAMP?

YES

NO

B

CONNECT A SIGNAL WITHIN THE OPERATING RANGE OF BAND 3 TO THE BAND 3 INPUT. WITH A SCOPE LOOK AT A100J7 PIN 2. IT SHOULD CONTAIN A COMPLEX WAVEFORM. DOES A PORTION OF THE WAVEFORM LOOK LIKE PHOTO A

NO

YES

A

POWER METER OR POWER METER ZERO CIRCUITS ON A107 BAD.

SEE FIGURE 6-16. POWER METER

Figure 6-15. Band 3

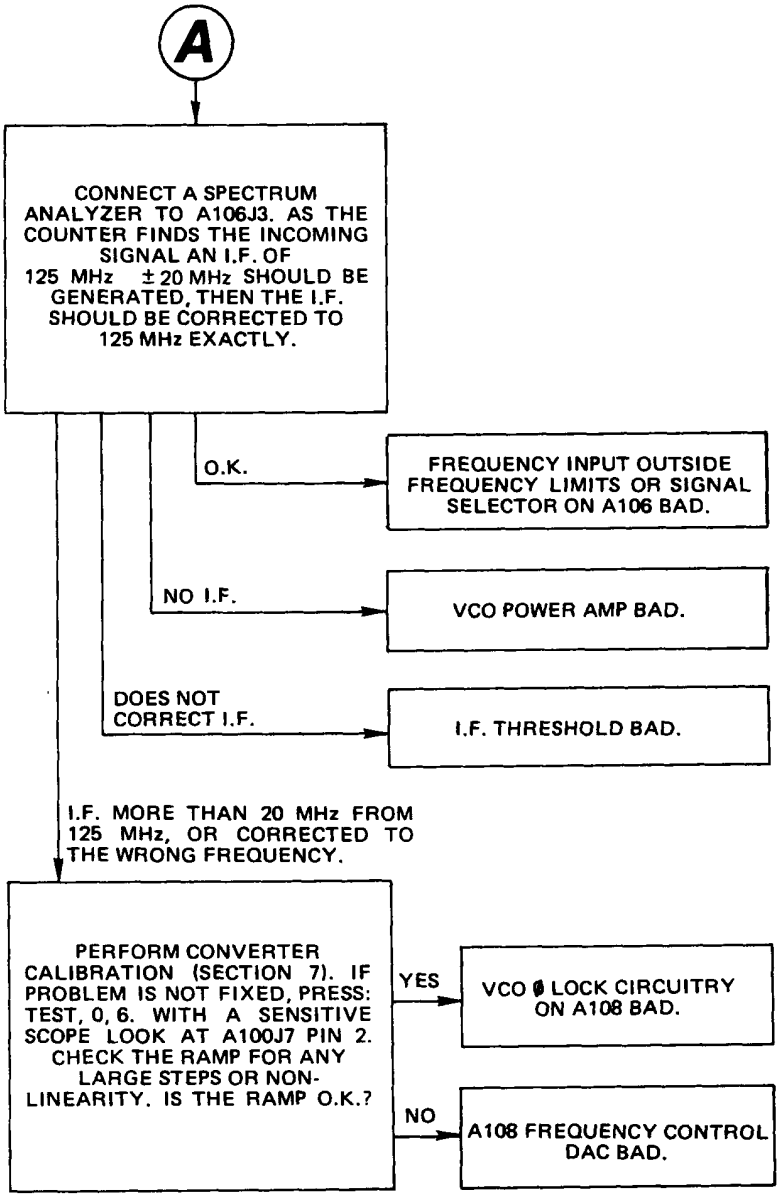


Figure 6-22. Band 3, continued

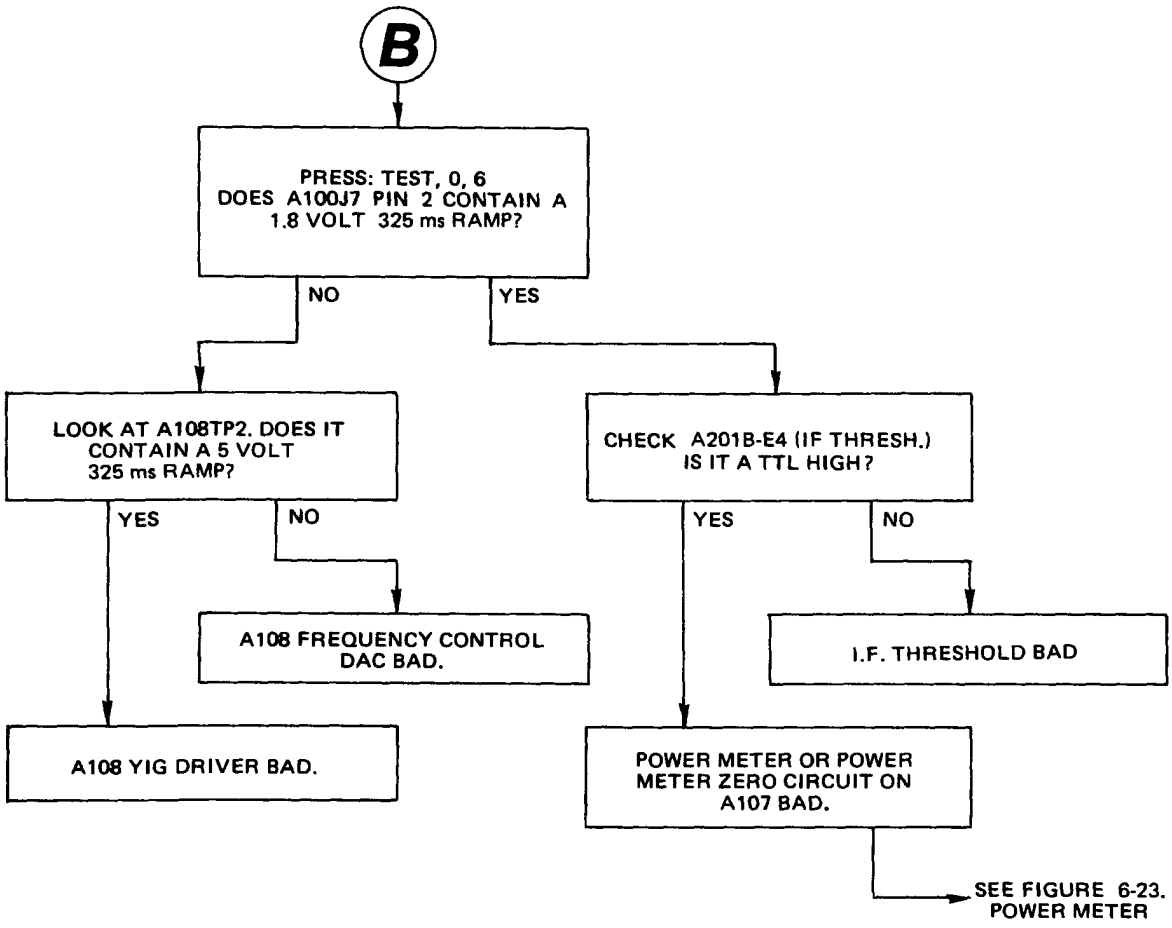


Figure 6-22. Band 3, continued

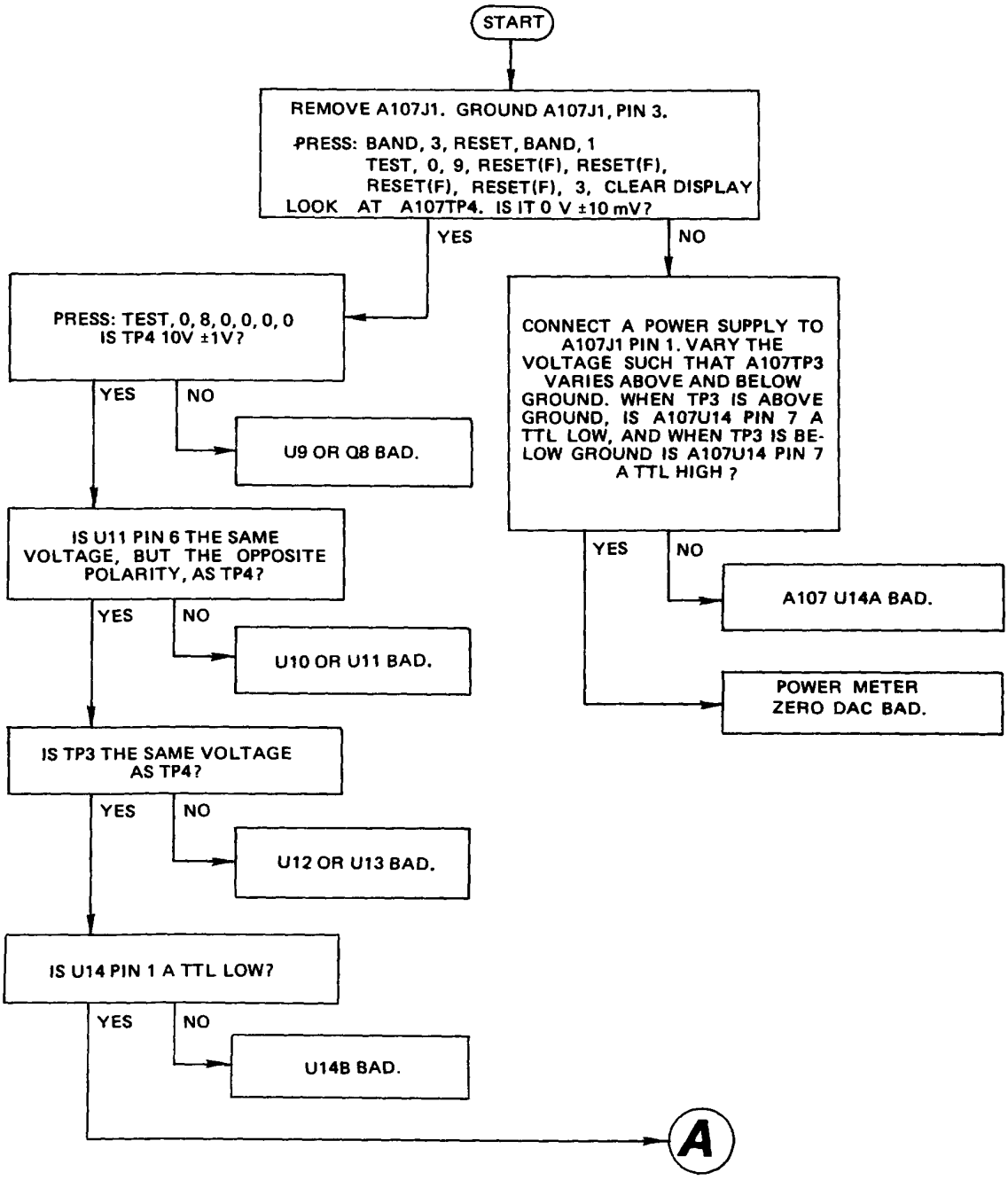


Figure 6-23. Power Meter and Power Meter Zero DAC

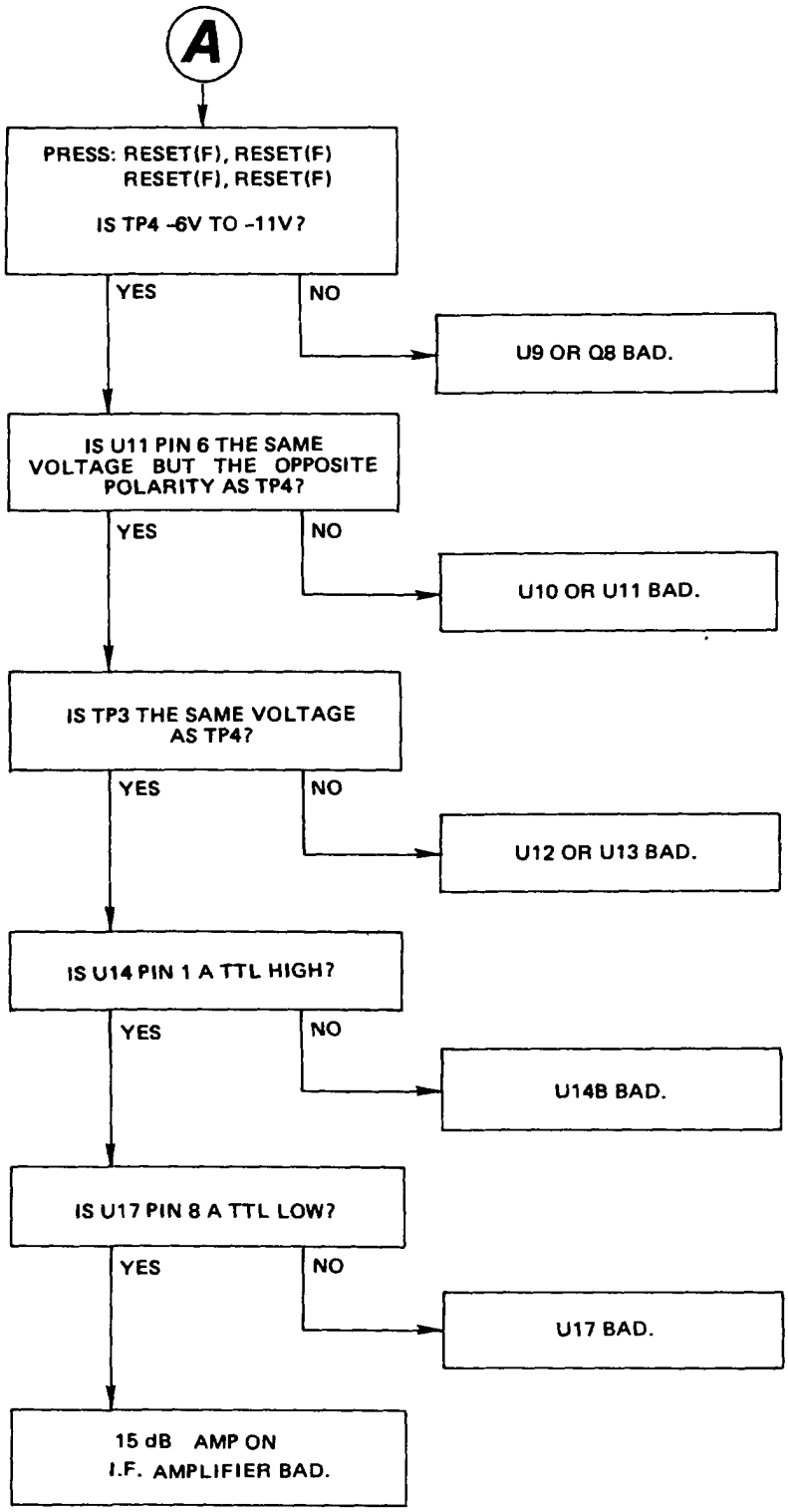


Figure 6-23. Power Meter and Power Meter Zero DAC, continued

Section 7
Adjustments and Calibrations

GENERAL

To correctly adjust the 545 or 548 counter use the following procedures. Adjustments should only be made if the counter does not operate as specified, or following the replacement of components. If the adjustments do not result in the performance specified then refer to the troubleshooting section of this manual. The test equipment required is:

MANUFACTURER	MODEL	DESCRIPTION	CRITICAL PARAMETERS
Tektronix	475	Oscilloscope	General Purpose
Fluke	8050A	D.V.M.	4½ digit resolution
H.P.	182C, 8559A	Spectrum Analyzer	125 MHz
Wavetek	2002	Sweeper	10 MHz - 2 GHz
Wiltron	610D, 6237D	Microwave Sweeper	2 GHz - 18 GHz
H.P.	8690A, 8696A	Microwave Sweeper	18 GHz - 26.5 GHz

POWER SUPPLY ADJUSTMENTS

Prior to making any adjustments to the power supply the counter should "warm up" at least 20 minutes.

Voltages are measured on the back of the Interconnect board (A100), or on the back of the Power Supply board (A101).

1. Connect the Digital Volt Meter (DVM) between ground and +12V.
2. Adjust A101 R5 until the voltage measures +12.000 VDC ± .010 VDC.
3. Connect the DVM between ground and -12 V.
4. Adjust A101 R17 until the voltage measures -12.000 VDC ± .010 VDC.

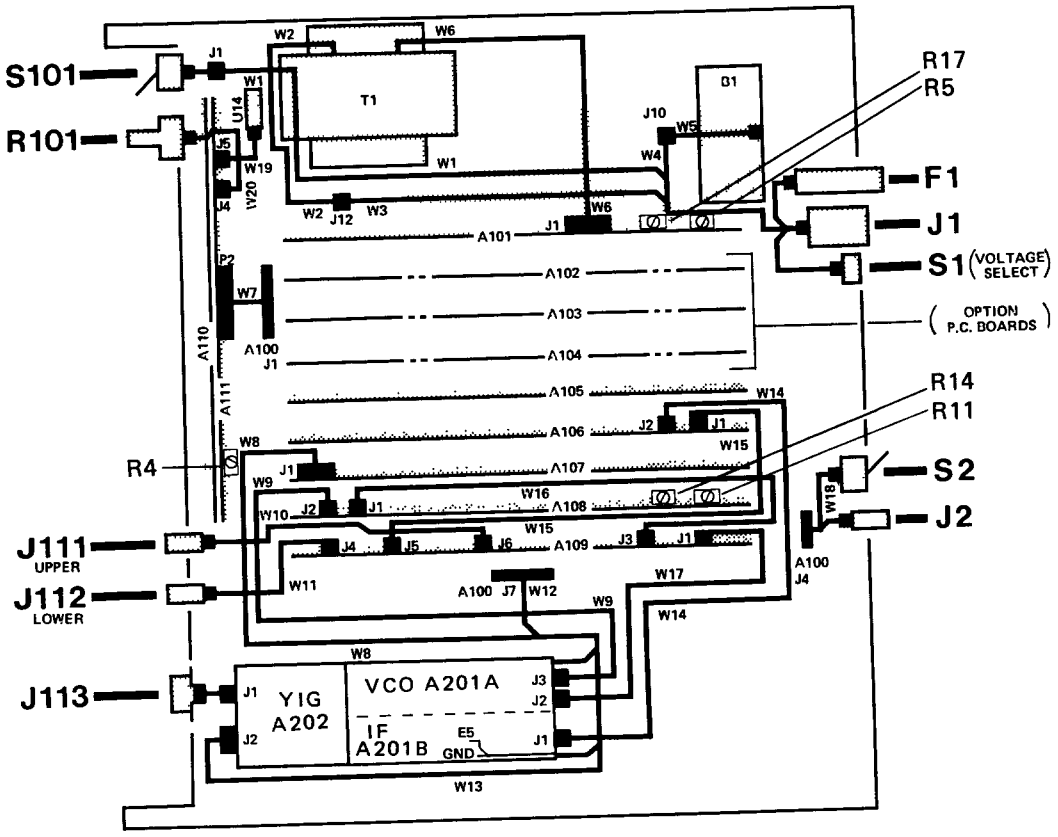


Figure 7-1. Adjustment Locations.

CONVERTER CALIBRATION

COURSE ADJUSTMENT

1. Press: [BAND] [3], [TEST] [1] [0],
   [9] [8] [4] [2] [0] [3]
   [9] [8] [4] [0] [±] (E) [8]

2. Set the microwave sweeper at 2.00 GHz ± 10 MHz, about -10 dBm.

3. Connect the sweeper output to band 3 of the counter.

4. Connect the oscilloscope to A201B-E5 (RF level).

5. Adjust A108R14 until A201B-E5 is at maximum negative voltage.

6. Set the sweeper to 15.00 GHz ± 10 MHz.

7. On the counter press: [9] [8] [4] [2] [1] [•] (D)
   [9] [8] [4] [0] [4] [CLEAR DATA] (C)

8. Adjust A108R11 until A201B-E5 is at maximum negative voltage.

9. Set the sweeper to 2.00 GHz ± 10 MHz.

10. On the counter press: [9] [8] [4] [2] [0] [3]
    [9] [8] [4] [0] [±] (E) [8]

11. Adjust A108R14 until A201B-E5 is at maximum negative voltage.

12. On the counter press: [CLEAR DISPLAY]

FINE ADJUSTMENT

1. Set the sweeper to 1.0 GHz ± 10 MHz.

2. Connect the spectrum analyzer to A109J2 (IF output).

3. The counter should be counting the incoming signal. The spectrum analyzer should be displaying the IF (125 MHz).

4. On the counter press RESET. When the converter finds the incoming signal an IF is generated which is near 125 MHz at first, then shifts to exactly 125 MHz (see figure 7-2). If the first IF is more than 5 MHz from 125 MHz, adjust A108R14 until the first IF (at an input frequency of 1 GHz) is 125 MHz ± 5 MHz.

5. Slowly tune the microwave sweeper from 1 to 26.5 GHz (to 18 GHz for 545), while pressing RESET on the counter.

6. Every time the converter finds the incoming signal the first IF should be 125 MHz ± 20 MHz. If not, adjust A108R11 until the first IF is always 125 MHz ± 20MHz.

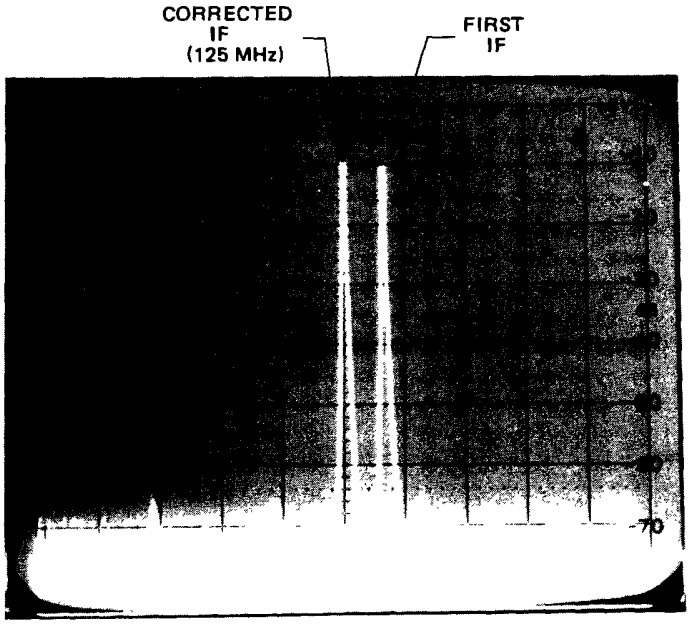


Figure 7-2. If Signal.

TIME BASE CALIBRATION

It is important to note that the precision of the time base calibration directly affects overall counter accuracy. Reasons for recalibration, and the procedures to be used, should be thoroughly understood before attempting any readjustment.

The fractional error in the frequency indicated by the counter, is equal to the negative of the fractional frequency error of the Time Base Oscillator with respect to its true value. That is:

$$\frac{\Delta f_s}{f_s} = \frac{\Delta f_t}{f_t}$$

where f_s is the true frequency of the measured signal, and f_t is the true frequency of the Time Base Oscillator. Thus, the inaccuracy associated with a frequency measurement is directly related to the quality of the Time Base Oscillator, and a measure of the precision with which it was originally adjusted.

TEMPERATURE COMPENSATED CRYSTAL OSCILLATOR (TCXO)

The standard Time Base Oscillator used in the counter is a TCXO (A116). The range of the actual measured frequencies of this oscillator will differ by no more than 2 parts in 10^6 if the temperature is slowly varied from 0 to +50 degrees C.

With a stable input frequency, the measurement indicated by the counter will fluctuate proportionally to the TCXO drift. To center this fluctuation on the true value of the measured signal, each TCXO has imprinted on its side the frequency setting required at +25 degrees C.

At approximate room temperature (+25 degrees C.), the slope of the frequency vs. temperature curve is normally no worse than $\pm 1 \times 10^{-7}$ parts per degree C. When the counter is used in an ordinary laboratory environment, the TCXO may be set as close to 10,000,000 Hz as desired. In this environment, a peak-to-peak temperature variation of 5° C. will result in a measured signal error of no more than $\pm 2.5 \times 10^{-7}$ parts. This signal error is due to the temperature characteristics of the Time Base Oscillator.

The natural aging characteristics of the crystal in the Time Base Oscillator can also cause inaccurate signal measurements. Aging refers to the long term, irreversible change in frequency (generally in the positive direction) which all quartz oscillators experience. The magnitude of this frequency fluctuation in the TCXO is less than 3×10^{-7} parts per month as specified. This may improve to at least 1×10^{-6} parts per year when in continuous operation.

Error due to aging adds directly to error due to temperature. The number of times the counter requires recalibration depends on the environment in which the counter operates, and upon the level of accuracy required.

For example, if the counter is subjected to the full operating temperature range one month after proper initial adjustments, the inaccuracy could vary from $+1.3 \times 10^{-6}$ parts to -0.7×10^{-6} parts.

TCXO CALIBRATION PROCEDURES

METHOD 1 (with accurate frequency counter)

1. Remove top cover of counter. Connect counter to reliable power source. Note ambient temperature.

2. Measure the frequency of the TCXO (at the rear panel 10 MHz connector) with a second counter of known calibration accuracy.

3. Adjust the TCXO by turning the calibration screw on the TCXO case until the measured frequency equals that shown on the TCXO calibration label.

METHOD 2 (with accurate frequency source)

1. Apply a 10 000 000 Hz signal from a frequency standard (or other oscillator of suitable accuracy and stability) to the Band 1 input of the counter.

2. Press RESOL [ ] [1] (1 Hz resolution)

3. Adjust the TCXO until the reading on the counter is offset from 10 000 000 Hz by the negative of the frequency shown on the TCXO. For example, if the TCXO calibration label shows a frequency of 10 000 003 Hz, adjust the TCXO until the counter displays 9 999 997 Hz.

DISPLAY INTENSITY

On the front panel logic assembly (A111) R4 may be adjusted to provide the most comfortable display intensity.

Section 8
Performance Tests

GENERAL

These tests are for the basic counter. Peformance tests for options are in section 10. These tests will enable the user to verify that the counter is operating within specifications.

VARIABLE LINE VOLTAGE

During the performance tests the counter should be connected to the power source, through a variable voltage device, so that line voltage may be varied ±10% from nominal. This will assure proper operating of the counter under various supply conditions.

REQUIRED TEST EQUIPMENT
(or equivalent)

MANUFACTURER	MODEL	DESCRIPTION	CRITICAL PARAMETERS
H.P.	651B	Signal Generator	10 Hz - 10 MHz
Wavetek	2002	Sweeper	10 MHz - 2 GHz
Wiltron	610D, 6237D	Microwave Sweeper	2 GHz - 18 GHz
H.P.	8690A, 8696A	Microwave Sweeper	18 GHz - 26.5 GHz

BAND 1
(10 Hz - 100 MHz)

1. Set the counter to band 1.
2. Connect the signal source output, through a 50 ohm shunt feedthrough resistor, to the band 1 input on the counter.
3. Set the signal level to 25 mv RMS (-19 dBm into 50 ohms).
4. Vary the signal from 10 Hz to 100 MHz (changing signal source as required).

The counter should display the correct input frequency.

BAND 2
(10 MHz - 1 GHz)

1. Set the counter to band 2.
2. Connect the signal source output to the band 2 input of the counter.
3. Set the signal level to -20 dBm (22 mv RMS).
4. Vary the signal input from 10 MHz to 1 GHz.

The counter should display the correct input frequency.

BAND 3
(548: 1 GHz - 26.5 GHz)
(545: 1 GHz - 18 GHz)

1. Set the counter to band 3.
2. Connect the signal source output to the band 3 input of the counter.
3. Vary the signal frequency from 1 GHz to 18/26.5 GHz (changing the signal source as required) at the following levels.

1 GHz – 12.4 GHz	-30 dBm (7 mv RMS)
12.4 GHz – 18 GHz	-25 dBm (12 mv RMS)
18 GHz – 22 GHz	-20 dBm (22 mv RMS)
22 GHz –26.5 GHz	-15 dBm (38 mv RMS)

The counter should display the correct input frequency.

Section 9
Functional Description and Illustrated Parts Breakdown

This section contains a functional description, a parts list, an illustration and a schematic diagram for each printed circuit board used in this counter.

The parts list is broken down by types of components, listed in alphanumeric sequence. The components that have a different reference designator (REF DES), but have the same EIP part number, are described for the first such component listed. Subsequent descriptions of that component will refer to the first entry. The total number of like components used on the same assembly will be listed with the first entry in the column identified as UNITS PER ASSY.

The last two columns of the parts list wil supply the name of the manufacturer and their Federal Supply Code for manufacturers (FSCM) number. A list of manufacturers names, addresses and their Federal Supply Code for Manufacturers (FSCM) number are given in Appendix A. The FSCM number is used in the parts list as a guide to the manufacturer or supplier of a part.

Pages 9-3 through 9-5 contain the top assembly of the counter and other basic information. After page 9-5 you will note that the page numbers have a three digit first number followed by a dashed number. The three digit number reflects the number of the assembly being described on those pages. The dashed number is the page sequence for the description of that assembly. For example, pages 105-1 through 105-5 all relate to the A105 printed circuit board. This page numbering system facilitates simple, modular page replacement when an assembly revision makes a manual update necessary.

REFERENCE DESIGNATORS

A	Assembly
B	Battery or Fan
C	Capacitor
CR	Diode
DS	Indicator (display)
F	Fuse
J	Jack or Connector
K	Relay
L	Inductor
P	Plug or PCB contacts
Q	Transistor
R	Resistor
S	Switch
T	Transformer
TP	Test Point
U	Integrated Circuit
X	Socket or Holder
Q1-3	Q1 *through* Q3
Q1/2	Q1 *and* Q2 (matched pair)

ABBREVIATIONS

CBN	Carbon
CER	Ceramic
CMT	Cermet
CNTR	Counter
CONV	Converter
COMP	Composition
CONN	Connector
ELEC	Electrolytic
FDTH	Feedthrough
FLM	Film
FML	Female
GP	General Purpose
IC	Integrated Circuit
K	Kilo (x 1,000)
LED	Light-emitting-diode
M	Meg (x 1,000,000)
MET OX	Metal Oxide
mF	Metal Film
mH	Millihenry
ML	Male
MTCH PR	Matched Pair
PC	Printed Circuit
PCB	PC Board Assembly
pF	Picofarad
PREC	Precision
RSTR	Resistor
RT AN	Right Angle
S.A.T.	Value or type selected during factory test. Part may not be used.
SW	Switch
TANT	Tantalum
TRIM	Trimmer
uF	Microfarad
uH	Microhenry
VAR	Variable
WPRF	Waterproof
WW	Wirewound
XSTR	Transistor

545/548 MICROWAVE COUNTER

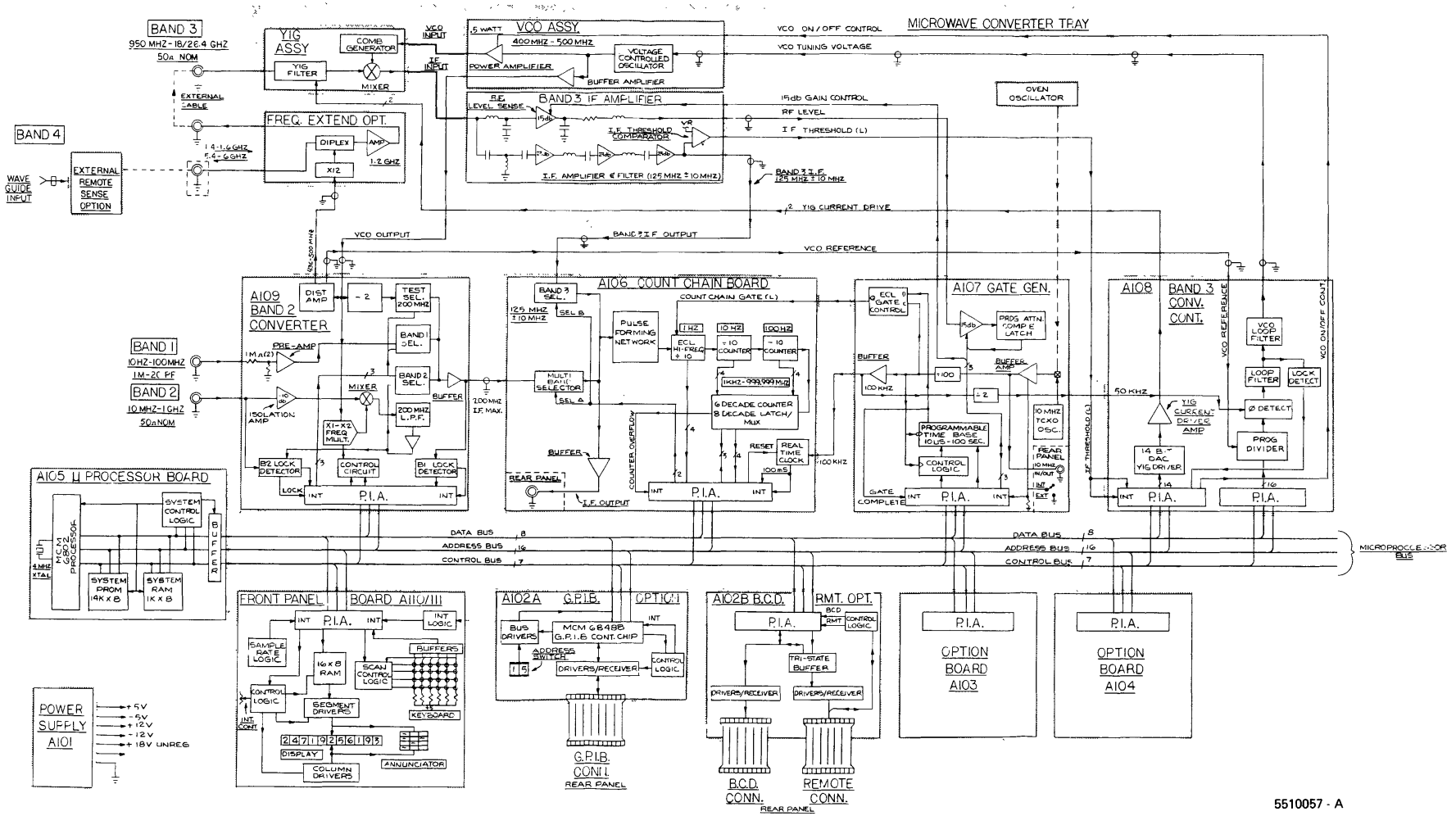
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
	COUNTER, MODEL 545			EIP	
-1	FRONT PANEL ASSY	2010133	1		
	Knob	5210223	1	5000160	31013
	Button set, 12 + 5	5210220	1	5230005 - 02	
	Panel	5210184	1		
	Sample Rate Control Assy	2010134	1		
	Alignment Pin	5210190	2		
	Retainer Key	5210191	1		
	Switch, toggle, PWR	2010187	1		
-2	REAR PANEL ASSY	2010135	1		
	Panel	5210192	1		
	Conn, Filter	2650005	1	3EF1	05245
	Switch, toggle, SPDT, 120V, 5A	4510001	1	7101H	09353
	Fuse holder	5000170	1	031.1653/1666/1663	
	Fuse, .75A, SB	5000079	1	MDL - 3/4A	71400
	Fuse, 0.4 A, S.B.	5000168	1	FST3X20mm	71400
	Conn, BNC	2610024	1	KC - 79 - 35	91836
	Voltage Select Switch Assy	2010159	1		
-3	FAN ASSY	2010136	1		
	Fan	5000151	1	760/126LF/182/1115	
	Conn, Plug, 3 pin	2620110	1	03 - 06 - 2032	0000A
	Contact, Male	2620038	2	02 - 06 - 2103	0000A
	Spacer	5210016	2		
-4	FRAME KIT	2010151	1		
	Panel, Side, Enclosure	5210210	2		
	Trim, Front Post	5220004	2		
	Trim, Handle	5220025	2		
	Frame	5210248	2		
	Corner Post, Front	5250001	2		
	Corner Post, Rear	5250002	2		
	Handle, Enclosures	5250011	2		
-5	TRANSFORMER,ASSY, A1T1	2010155	1		
	Transformer, Power	4900005	1		
	Conn, Plug, 9 pin	2620112	1	03 - 06 - 2092	0000A
	Conn, Housing, 6 pin	2620129	Ref	640427 - 6	AMP
	Contact, Male	2620038	7	02 - 06 - 2103	0000A
	Contact, Female	2620036		02 - 06 - 1103	0000A
-6	FRONT CARD GUIDE ASSY	2010156	1	5210199	
-7	REAR CARD GUIDE ASSY	2010157	1	5210200	
-8	TOP COVER ASSY	2010212	1		
-9	BOTTOM COVER	5210209	1		
-10	TILT BAIL	5000055	1		

545/548 MICROWAVE COUNTER, continued

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
-11	Foot, Plastic Enclosure	5220003	4		
-12	Line Cord Set - Domestic	5440002	1		
	Line Cord Set - Export	5440017	1		
	PCB ASSEMBLIES			See Page No.	
A100	Counter Interconnect	2020180	1	100 - 1	
A101	Power Supply	2020131	1	101 - 1	
A105	Microprocessor	2020135	1	105 - 1	
A106	Count Chain	2020136	1	106 - 1	
A107	Gate Generator	2020137	1	107 - 1	
A108	Converter Control (Band 3)	2020138	1	108 - 1	
A109	Band 2 Converter	2020139	1	109 - 1	
A110	Display and Keyboard	2020140	1	110 - 1	
A111	Driver Logic	2020141	1	111 - 1	
A203	Microwave Converter	2010142	1	200 - 1	
A201A	Voltage Control Oscillator	2020142	1	201 - 1	
A201B	IF Amplifier	2020143	1	202 - 1	
A202	Microwave (YIG) not shown				
	CABLES:				
	Front Panel, Flat Ribbon	2040169	1		
	Front Panel, Harness	2040168	1		
	Rear Panel, Harness	2040167	1		
	(J111 - A109J8) Band 1, Coax	2040165	1		
	(A112-A109J4) Band 2, Coax	2040166	1		
	(A108J1-N09J3), Coax	2040208	1		
	(A106J2-A109J7), Coax	2040210	1		
	VCO/IF, Harness	2040170	1		
	(A201J3-A106J1), Coax	2040172	1		
	(A201J4-A107J1), Coax	2040173	1		
	(A201J5-A108J2), Coax	2040174	1		
	(A201J6-A109J1), Coax	2040175	1		
	PROMS:				
A105 —	BASIC PROM SET				
U7		6400001-03			
U6		6400001-04			
U13		6400001-05			
U12		6400001-06			
U17		6400001-07			
A105 —	GPIB/ BAND 4 OPTION				
U20		6400001-01			
U8		6400001-02			
A107 —	POWER METER OPTION				
U20		6400001-08			
A103 —	DAC OPTION				
U9		6400001-09			
A105 —	BCD REMOTE PROGRAMMING OPTION				
U20		6400002-01			
U8		6400002-02			
A105	BAND 4 ONLY (548)				
U20		6400001-01			

FOR REFERENCE ONLY

SEE PARTS LIST OF EACH ASSEMBLY OR OPTION FOR PROM DESCRIPTION



5510057 - A

Figure 9-1. 545/548 Block Diagram

A100
COUNTER INTERCONNECT
(2020130)

FUNCTIONAL
DESCRIPTION
NOT REQUIRED

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A100 COUNTER INTERCONNECT ASSY

2020180 - B

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A100	Counter Interconnect Assy	2020180	1		
J1	Header, Str, 26 pin	2620078	1	3429 - 2302	76381
J2	Header, Str, 50 pin	2620081	2	3433 - 2302	76381
J3	J2				
J4	Friction Lock, 4 pin	2620061	1	09 - 65 - 1049	0000A
J5	Friction Lock, 6 pin	2620090	1	09 - 65 - 1069	"
J6	Friction Lock, 7 pin	2620091	1	09 - 65 - 1079	"
J7	Friction Lock, 10 pin	2620092	1	09 - 65 - 1109	"
J8	Friction Lock, 4 pin	2620068	1	640456-4	AMP
XA101	Conn, 11 position	2620101	1	583533 - 9	AMP
XA102	Conn, 50 position	2620103	1	4 - 583533 - 8	"
XA103 thru XA109	Conn, 30 position	2620102	7	2 - 583533 - 8	"
	Key Plug	5000155	8	530286 - 2	"

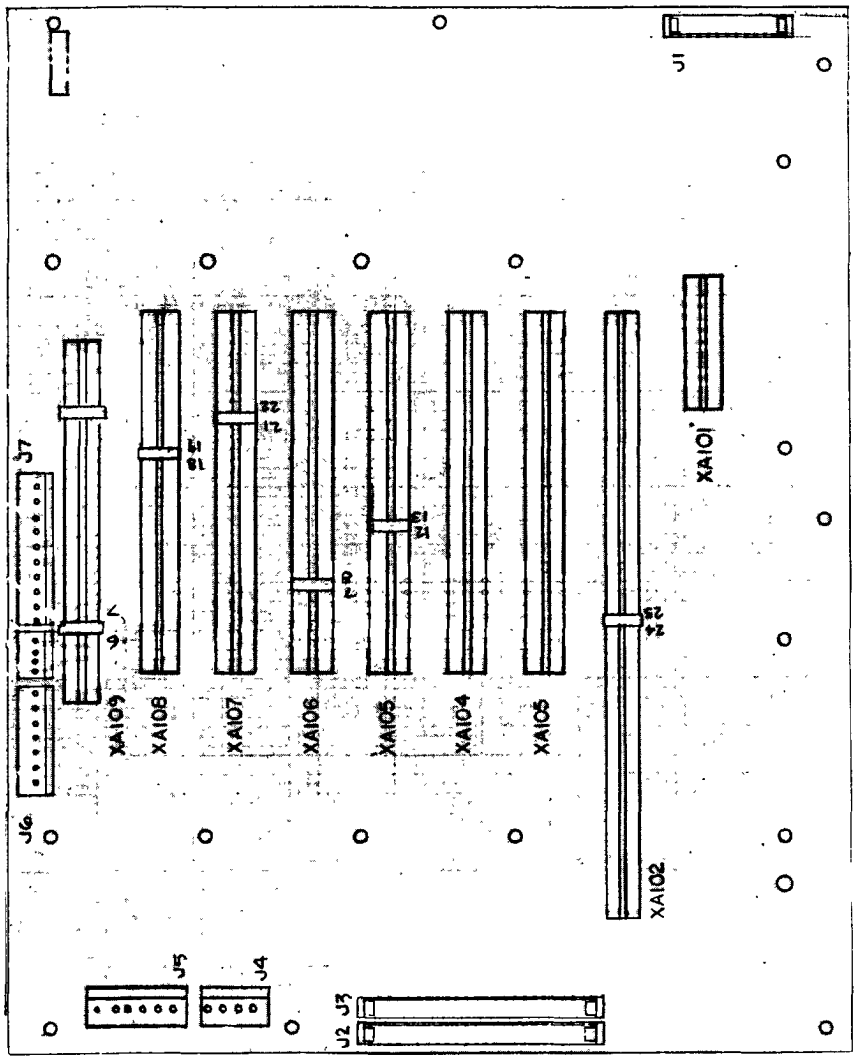
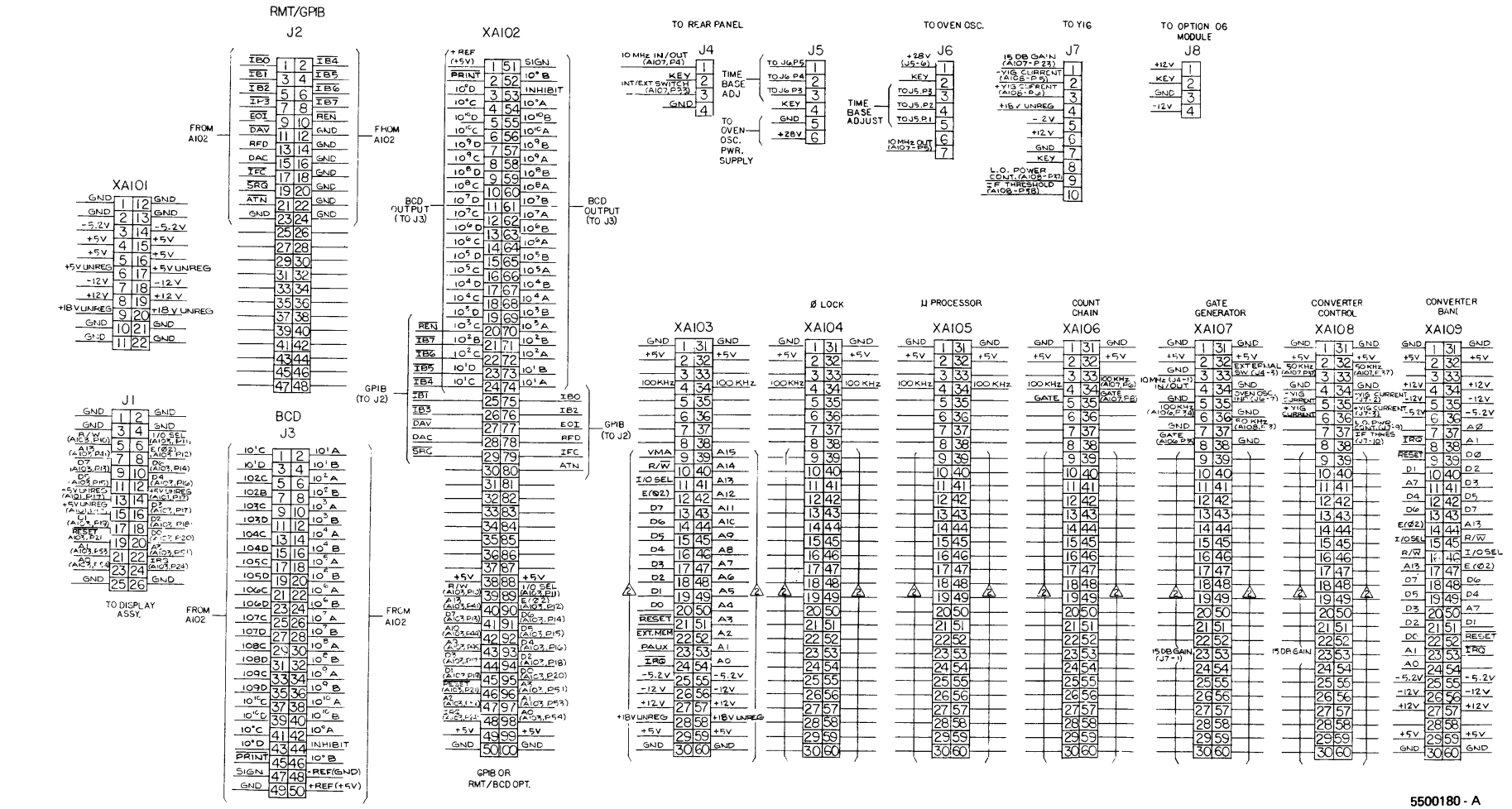


Figure 100a. Counter Interconnect Component Locator



△ XA103 THRU XA106 HAVE COMMON CONNECTIONS ON LINES SHOWN IN BRACKETS ETC.

Figure 100b. Counter Interconnect Schematic

A101
POWER SUPPLY
(2020131)

The power Supply furnishes all basic operating voltages required by the counter. The supply consists of two basic sub-assemblies.

- PC Board (A101), containing the rectifiers, filter capacitors, and regulator circuitry.
- Chassis mounted components consisting of the power transformer (T1), primary wiring, F1 fuse; (100/120V), the 220/240V power programming switch; and the on/off power switch (S101) mounted on the front panel.

The basic voltages required by the counter are unregulated +18V, regulated +5V, −5.2, +12V and −12V.

The input AC voltage is full wave rectified and filtered to produce DC voltages of +9V and 18V.

The unregulated +18V is used directly as one supply voltage. The +18V is regulated to a +12V by the action of LM305, a series pass transistor (MJE3055), and foldback current limiting circuitry. The +18V is regulated to a −12V by LM304, a series pass transistor, and foldback current limiting circuitry.

The +9V current is regulated to +5V by a three terminal regulator containing current and thermal sensing circuitry. The +9V current is also regulated to −5.2V by a three terminal regulator that contains thermal and current shutdown circuitry.

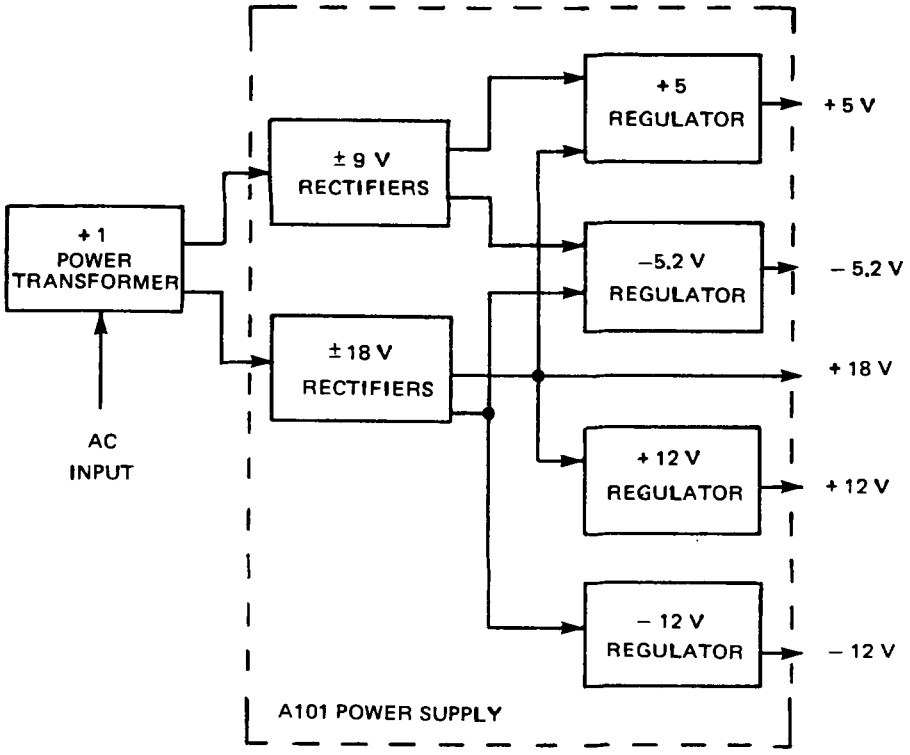


Figure 101a. Power Supply Functional Diagram

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A101 POWER SUPPLY ASSY

2020131-B

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A101	Power Supply Assy	2020131	1		
C1	Tant, 10μF, 20%, 25V	2300029	2	TAG 20 - 10/25(M)	14433
C2	Mica, 47 pF, 5%, 500V	2260004	1	DM10 - 470J	72136
C3	C1				
C4	Tant, 33μF, 20%, 20V	2300023	1	TAG 20 - 33/20 - 20	14433
C5	Cer, .001μF, 20%, 20V	2150001	1	5GA - D10	56289
C6	Tant, 1.0μF, 20% 35V	2300008	3	TAG 20 -1.0/35 - 50	14433
C7	Elec, 14,000μF, 25V	2200017	1	3110HB143U025	80031
C8	Elec, 9,500μF, 15V	2200016	1	3110HA952U025	80031
C9	Elec, 32,000μF, 15V	2200019	1	3110RB323U015	80031
C10	Elec, 4,700μF, 16V	2200020	1	3050JJ4720U16B	80031
C11	C6				
C12	C6				
CR1 thru CR4	Rectifier	2704001	4	IN4001	07263
CR5	Zener, 12V	2720963	1	IN963A	04713
CR6	Rectifier Brdg	2710029	1	MDA970 - 1	04713
CR7	Rectifier, Brdg	2710028	1	MDA990 - 1	04713
J1	Conn, 6 pin (FRCTN Lock)	2620157	1	640445-6	0000A
Q1	NPN Power	4710001	2	MJE3055	04713
Q2	PNP Power	4710002	2	MJE370	04713
Q3	Q1				
Q4	Q2				
Q5	PNP, General Purpose	4704126	1	2N4126	04713
R1	Comp, 68 ohms, 5%, 1/4 W	4010680	2	RC07GF680J	81349
R2	Met Ox, 36 ohms, 2%, 1/4 W	4130360	1	C4/2%/36	24546
R3	Wire Wound, .66 ohms, 3%, 4W	4110012	2	RS - 2	91637
R4	Prec, 14.7K ohms, 1%, 1/8 W	4061472	1	RN55D1472F	81349
R5	Var. Cer., 500 ohm	4250014	1	72XR500	73138
R6	Prec, 2.26K ohms, 1%, 1/8 W	4062261	1	RN55D2261F	81349
R7	Met Ox, 820 ohms, 2%, 1/4 W	4130821	2	C4/2%/820	24546
R8	R7				
R9	R3				
R10	R1				
R11	Comp, 100 ohms, 5%, 1/4 W	4010101	1	RC07GF101J	81349
R12	Met Ox, 910 ohms, 2%, 1/4 W	4130911	2	C4/2%/910	24546
R13	Met Ox, 12K ohms, 2%, 1/4 W	4130123	1	C4/2%/12K	24546
R14	Prec, 2.43K ohms, 1%, 1/8 W	4062431	1	RN55D2431	81349
R15	Prec, 4.7K ohms, 2%, 1/4 W	4130472	1	C4/2%/4.7	24546
R16	Met Ox, 1K ohms, 2%, 1/4 W	4130102	1	C4/2%/1K	24546
R17	Var, Cer, 2K ohms	4250016	1	72XR2K	73138
U1	Voltage Regulator	3040305	1	LM305	0000X
U2	Voltage Regulator	3040304	1	LM304	0000X
U3	+5VDC Regulator	3057805	1	UA78H05A	07263
U4	-5.2 V Regulator	3057905	1	MC7905.2 CT	04713
	Heatsink	5210196	1	EIP	

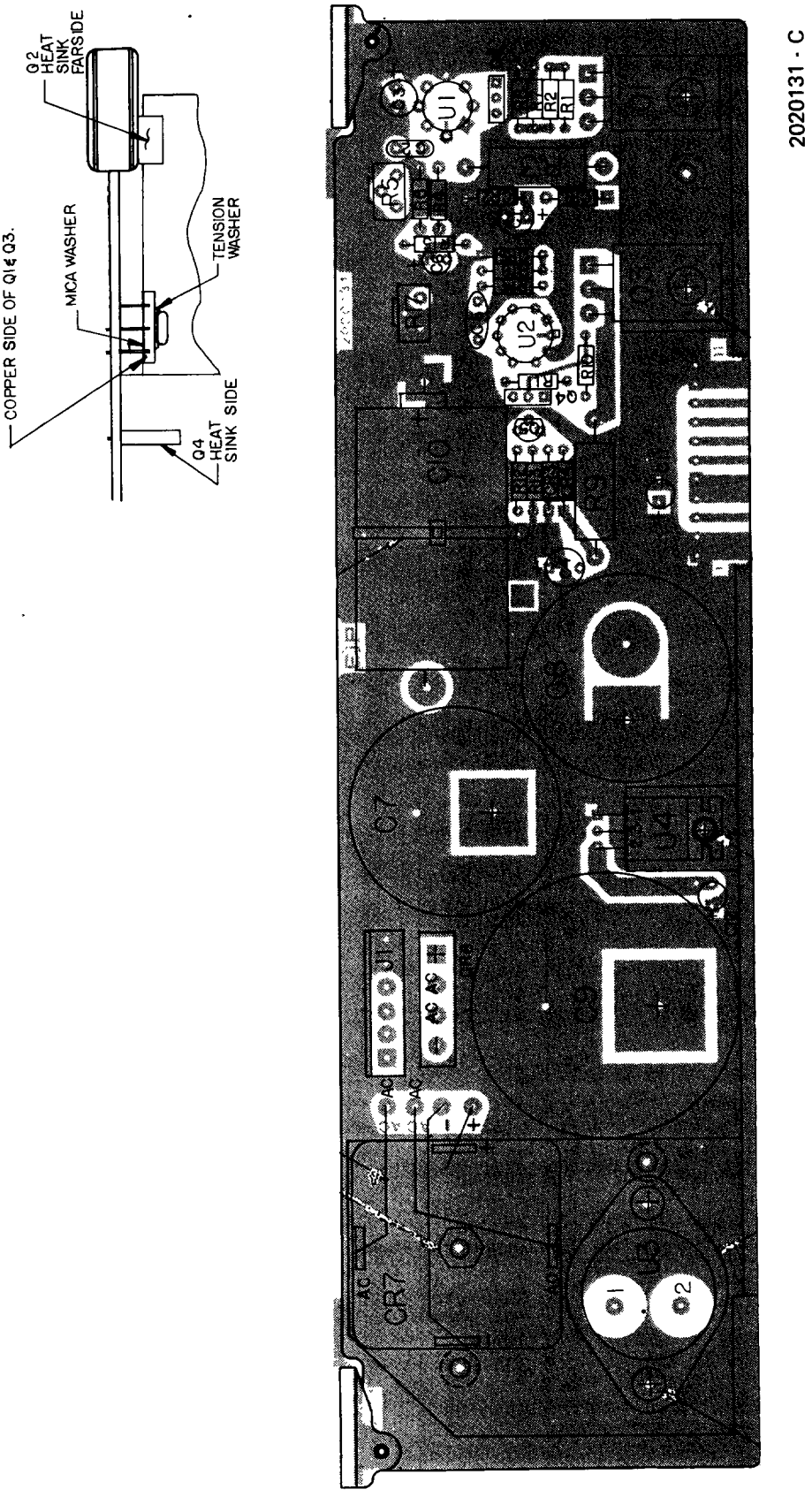
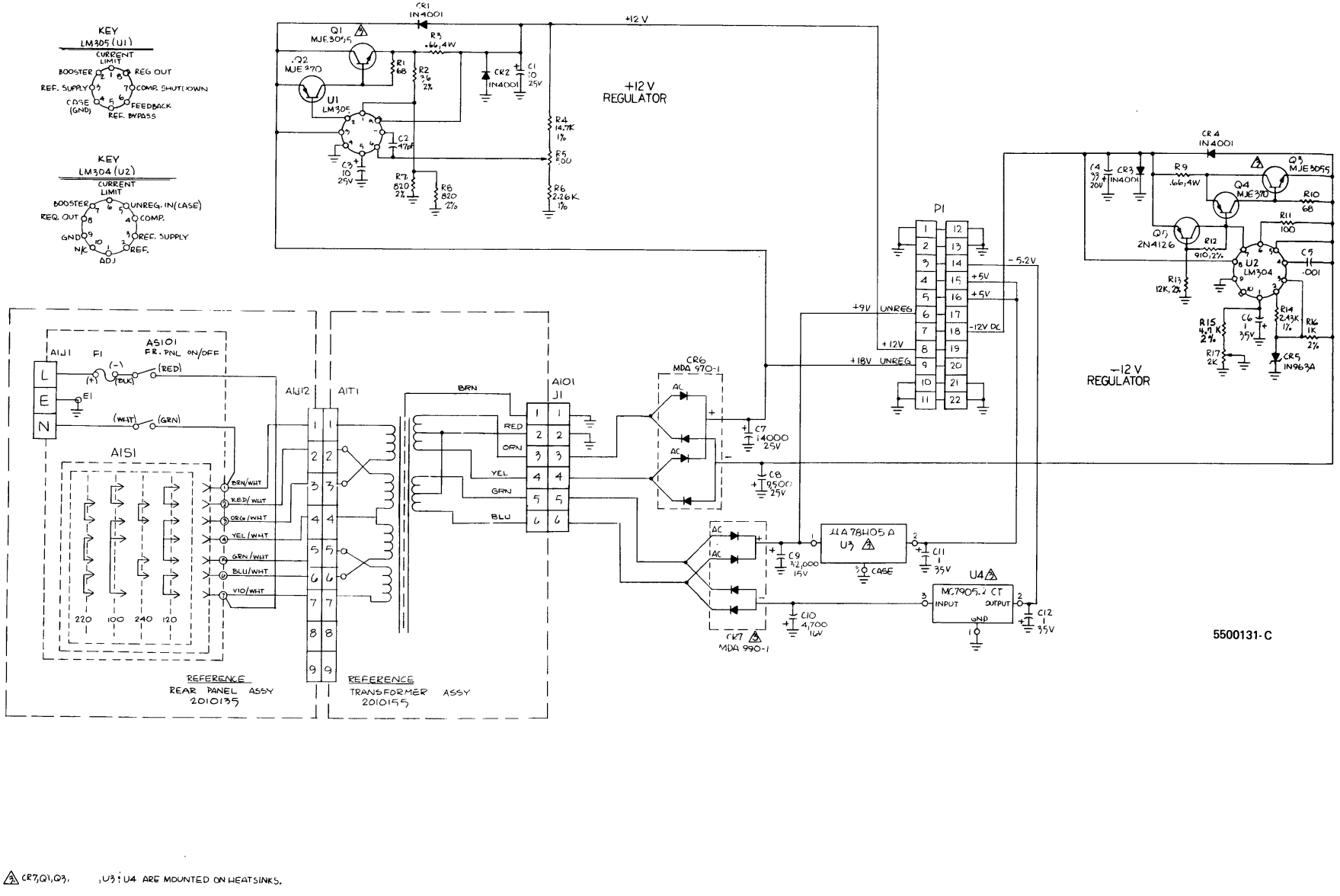


Figure 101 b. Power Supply Component Locator



⚠2 CR7, Q1, Q3, , U3 & U4 ARE MOUNTED ON HEATSINKS.

Figure 101 c. **Power Supply Schematic**

A105
MICROPROCESSOR
(2020135)

The Microprocessor assembly controls the counter operation. The microprocessor (U1) contains an internal clock oscillator and 128 bytes of RAM. U1 has both an 8 bit data bus and a 16 bit address bus.

A 4MHz crystal (Y1) is connected between pins 38 and 39 of U1 to provide a 1MHz clock signal for U1 and the rest of the counter. A divide-by-4 circuit on U1 performs the frequency division. The 1 MHz clock, E (02), can be stretched integral multiples of half periods (500ns) by putting a logic 0 on the $\overline{\text{MEMORY READY}}$ ($\overline{\text{MR}}$) input. The clock is stretched when interfacing with slow memories or I/O devices. See figure 105a.

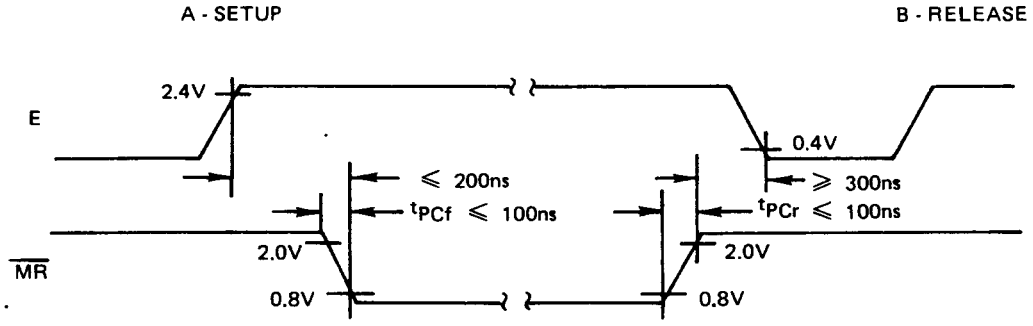


Figure 105a. Memory Ready Timing Diagram

A one-shot retriggering circuit (U14) provides the signal required to stretch the clock E(02) by 500ns (1 half period). U14 is triggered whenever an I/O operation is performed. It can also be triggered by $\overline{\text{EXT MEMORY}}$ if the trace labeled ⚠3 on the schematic is cut and jumpered to the $\overline{\text{EXT MEMORY}}$ input.

The microprocessor assembly contains seven 24-pin sockets for either seven 2KX8 or four 4KX8 PROM's (U6-U8, U11-U13, U20). The assembly is currently wired for 2KX8 PROM's. When 4KX8 PROM's are used, traces labeled ⚠4 on the schematic have to be cut and jumpers have to be added as indicated (total 10 places). When 4KX8 PROM's are used, only sockets labeled U6, U11-U13 are used. The PROM's on this assembly occupy address locations COOO-FFFF hex for 4KX8 PROM's and C800-FFFF hex for 2KX8 PROM's.

The address decoding for the PROM's is provided by U9. When the address on the address bus falls within the address range of a PROM, the chip select of that PROM will be enabled. The address range of each PROM is indicated on the shematic (for 2KX8 PROM's only).

This assembly also contains two 1KX4 RAM's. The RAM's are connected to form a 1KX8 block of random access memory. Address decoding for the RAM's is provided by a comparator (U2). For ease of address decoding, the 128 bytes of RAM in U1 are disabled. This is done by grounding the RAM ENABLE (RE) input on U1 pin 36. The 1024 bytes of RAM occupy address locations 0000 - 03FF hex.

The voltage comparator (U17) provides the $\overline{\text{RESET}}$ command during system power-up. When power is first turned on, the negative input of U17 is at ground. The reset command is at logic 0, resetting U1 and the rest of the counter. C6 will slowly charge towards +5V through the 2.2M ohm resistor (R3). When C6 is charged to more than 0.85V, the output of U17 will switch to logic 0, taking away the $\overline{\text{RESET}}$ command. The counter is now ready for normal operations.

U16, U18, and U19 are octal buss tranceivers. U18 and U19 are used for the address bus, and they are always enabled. U16 is used for the data buss. The R/$\overline{\text{W}}$ command signal from U1 determines whether U16 is in the receive or transmit state. U16 is enabled only when I/O SEL (true when active instruction is I/O) or $\overline{\text{EXT MEMORY}}$ is true.

The DIP switch SW1, diodes CR2 and CR3 are used for trouble-shooting. When trouble-shooting the A105 board with a signature analyzer, the microprocessor is put into a free-running mode by opening SW1 and grounding TP11. By doing so, the data bus of the microprocessor is disconnected from the rest of the board and a CLRB (HEX 5F) instruction is put on the data bus continuously. When the START, STOP & CLOCK inputs of the signature analyzer are properly connected, the signatures at various inputs or outputs can be obtained by using the logic probe of the signature analyzer. The signatures can then be compared with the signature chart for the microprocessor board to determine which component is faulty.

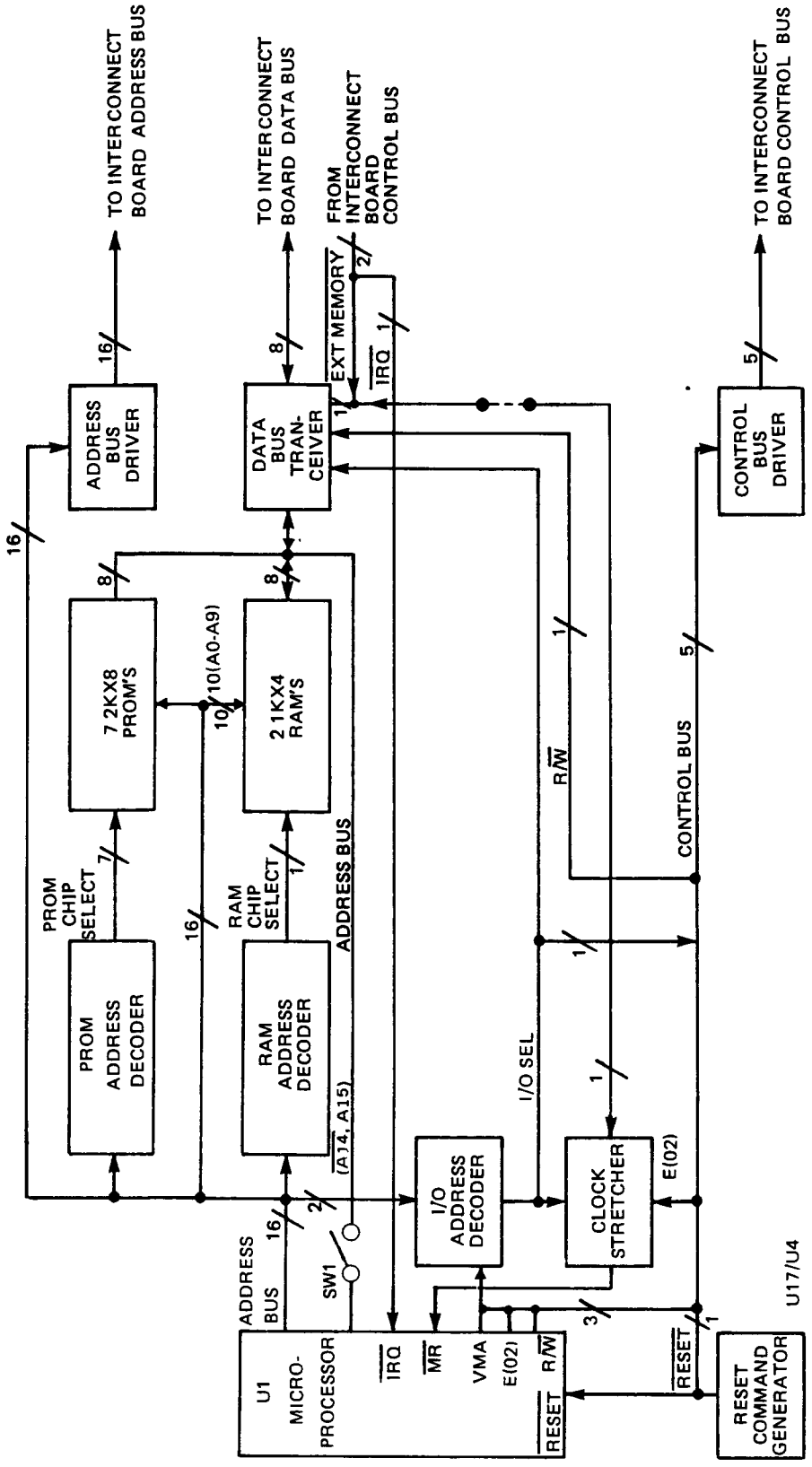


Figure 105b. Microprocessor Functional Diagram

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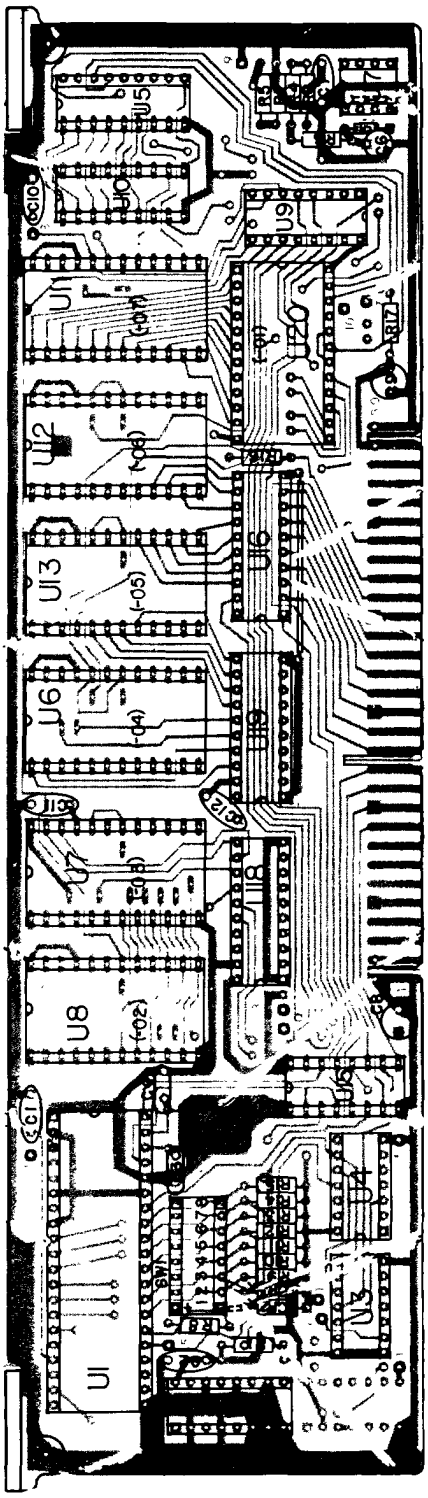
A105 MICROPROCESSOR ASSY

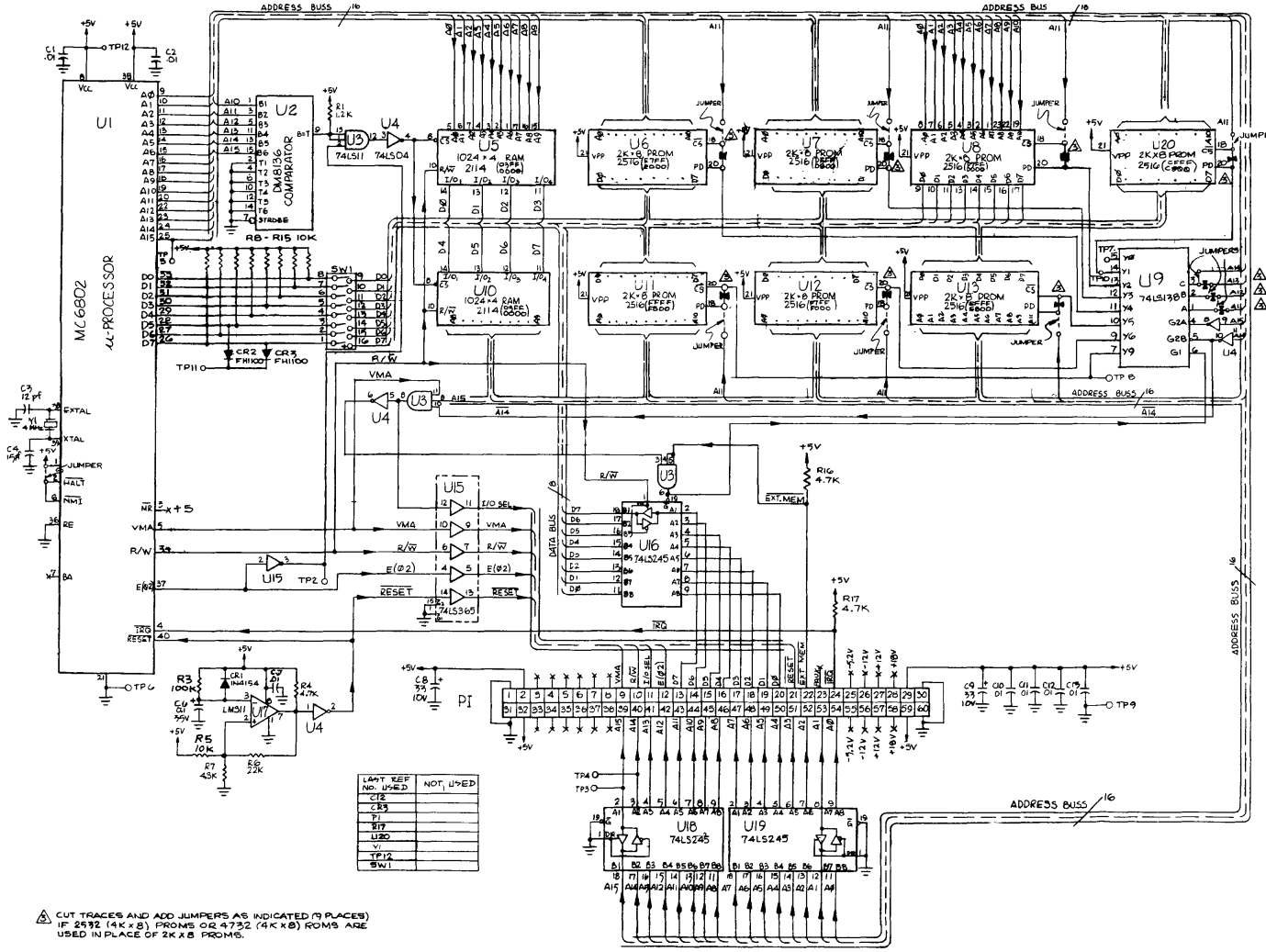
2020135 - K

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A105	Microprocessor Assy	2020135	1	EIP	
C1	Cer, .01μF, 20%, 100V	2150003	6	TG - S10	56289
C2	C1				
C3	Mica, 12pF, 5%, 500V	2260013	1	CD120J03	72136
C4	Mica, 15pF, 5%, 500V	2260014	1	CD150J03	72136
C5	Not Used				
C6	Tant, .1μF, 20%, 35V	2300020	1	TAG20 - 0.10/35	14433
C7	C1				
C8	Tant, 33μF, 20%, 10V	2300015	2	TAG20 - 33/10 - 50	14433
C9	C8				
C10 thru C12	C1				
CR1	General Purpose	2704154	1	IN4154	07263
CR2	General Purpose	2710004	2	FH1100	
CR3	CR2				
R1	Comp, 1.2K, 5%, 1/8W	4010122	1	RC07GF122J	81349
R2	Not Used				
R3	Comp, 1 M, 5%, 1/8 W	4010105	1	RC07GF105J	81349
R4	Comp, 4.7K, 5%, 1/8 W	4010472	1	RC07GF472J	81349
R5	Comp, 10 K, 5%, 1/8 W	4010103	1	RC07GF103J	81349
R6	Comp, 22K, 5%, 1/8 W	4010223	1	RC07GF223J	81349
R7	Comp, 4.3K, 5%, 1/8 W	4010432	1	RC07GF432J	81349
R8 thru R15	Comp, 10K, 5%, 1/4 W	4010103	8	RC07GF103J	81349
R16	Comp, 4.7K, 5%, 1/4 W	4010472	2	RC07GF472J	81349
R17	R16				
SW1	8 Dip	4540005	1	1008 - 692	
TP1 thru TP12	Conn, Pin, .04D, Gold	2620032	12	460-2970-02-03	71279
U1	Microprocessor/Clock/RAM	3056802	1	MC6802	04713
U2	6 Bit Comparator	3078136	1	8136	27014
U3	Tri, 31NP Cap and Gate	3087411	1	DM74LS11N	0000X
U4	Hex Converter	3087404	1	DM74LS04N	0000X
U5	1024X4 Bit RAM	3052114	2	TM2114	01295
U6	Program PROM 4	6400001-04	1	TM2516	01295
U7	Program PROM 3	6400001-03	1	TM2516	01295
U8	Program PROM 2 ——— GPIB Only	6400001-02	1	TM2516	01295
U9	Decoder 1	3084138	1	SN74LS138N	01295
U10	U5				
U11	Program PROM 7	6400001-07	1	TM2516	01295
U12	Program PROM 6	6400001-06	1	TM2516	01295
U13	Program PROM 5	6400001-05	1	TM2516	01295
U14	Not Used				
U15	Hex Buss Driver	3084365	1	SN74LS365N	01295
U16	Octal Buss Trans.	3084245	3	SN74LS24SN	01295
U17	Voltage Comparator	3050311	1	LM311N	0000X
U18	U16				
U19	U16				
U20	Program PROM 1 ——— GPIB Only	6400001-01	REF	TM2516	01295
Y1	Crystal, 4 MHz	2030015	1	MP1PR4.00	



2020135 - P

Figure 105 c. Microprocessor Component Locator

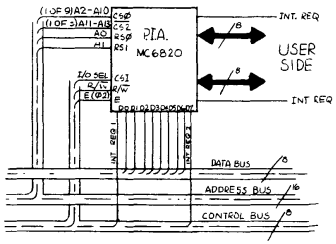


LAST REF NO. USED	NOT USED
C15	
C23	
PI	
R17	
U20	
Y1	
TP12	
SW1	

I.C. NO.	TYPE	PIN NO. GND	PIN NO. +5V
U1	MC6802	1,21	8,35
U2	DM8136	5	16
U3	74LS11	7	14
U4	74LS04	7	14
U5,U10	1024 x 4 RAM 2145	9	18
U6,U7,U8,U20 U11,U12,U13	2K x 8 PROM 2516	12	24
U9	74LS138	8	16
U15	74LS365	8	16
U16,U18,U19	74LS245	10	20
U17	LM311	4	8

NOT USED

TYPICAL P.I.A. I/O CONNECT
(REF ONLY)



5500135 - D

⚠5 CUT TRACES AND ADD JUMPERS AS INDICATED (9 PLACES) IF 2532 (4K x 8) PROMS OR 4732 (4K x 8) ROMS ARE USED IN PLACE OF 2K x 8 PROMS.

Figure 105d. Microprocessor Schematic

A106
COUNT CHAIN
(2020136)

The Count Chain Assembly receives IF signals from the Band 3 IF Amplifier (A201B) and the Band 2 Converter (A109). It also receives a gate signal and a 100 kHz reference signal from the Gate Generator (A107). The count chain assembly selects the appropriate IF signal, gates it, and counts it to produce a BCD output that represents the input frequency. It also produces one or two IF output signals to be used for options at J3 and J4.

The A106 board receives two IF input signals on J1 and J2. The appropriate input is selected by enabling one of two differential amplifiers (U1A or U1B). Enabling of the appropriate amplifier is achieved by turning on a transistor switch (Q11 or Q12). The appropriate transistor is turned on by the output of an open collector inverter (U7C or U7A) driven by a TTL signal from the PIA (U10).

The output of the input selector differentially drives a squaring circuit. The squaring circuit consists of a differentially driven current mirror (Q1) driving a tunnel diode (CR5). The voltage across the tunnel diode changes abruptly between two states (approximately 0.2V and 0.5V). The signal across the diode drives the pulse forming circuit. This circuit begins with a high speed differential amplifier (Q2 and Q3). The output of this amplifier drives Q4 which is a current switch. The square wave current, from Q4's collector, drives an inductor (L1). The voltage across the inductor is a series of pulses; a positive pulse when Q4 turns on and a negative pulse when Q4 turns off. Diode CR5 tends to remove the negative pulses and increases the damping to improve the amplitude of the positive pulses. The positive pulses from the generator drive a pulse inverter (Q6). The pulse inverter is a high-speed zero bias amplifier that is biased at cut off by diode CR6.

The output of the pulse inverter (Q6) drives the input to the first decade counter (U2). The bias for the U2 input is established by a tracking bias supply (U3, Q7). The voltage at TP2 is equal to the voltage on U2 pin 1, plus a fixed DC offset selected by R45. The BCD outputs from U2 are slew-rate limited, and can only be seen after the counting ends and comes to rest. The carry output on pin 9 is an ECL level U2 signal, and is always visible.

The ECL output of U2 drives an ECL to TTL converter (Q8, Q9 and Q10). This converter is a differential amplifier with a cascode output buffer (Q8). The response of Q8 is improved by inductive peaking provided by L2. The output of Q8 drives a decade counter (U4) which in turn drives a third decade counter (U5). The BCD outputs of U4 and U5 are connected to a 6 decade counter (U6) which derives its clock information directly from the BCD outputs of U5. When counting is finished, 8 decades of BCD data are read by the microprocessor (through the PIA U10) from U6 by a time multiplex process. The multiplexer (set to the first digit by the end of the previous reset clock) loads the multiplex latches with the $\overline{\text{Latch Load}}$ clock, and steps to the remaining 7 digits with 7 pulses on the $\overline{\text{Scan Clock}}$ line. The first decade of BCD data from U2 is read directly from the PIA.

A single reset line is used to reset all count stages to zero before the next count cycle begins.

A real-time clock (U8, U9) is also on the count chain assembly. This circuit takes the 100kHz reference signal, that is coming from the Counter Interconnect Assembly (A100), and divides it by 10,000 to give a 10Hz (100ms) clock. The output from this clock is fed to the PIA to allow the microprocessor to gather time information at a 10Hz rate for timing functions within the program.

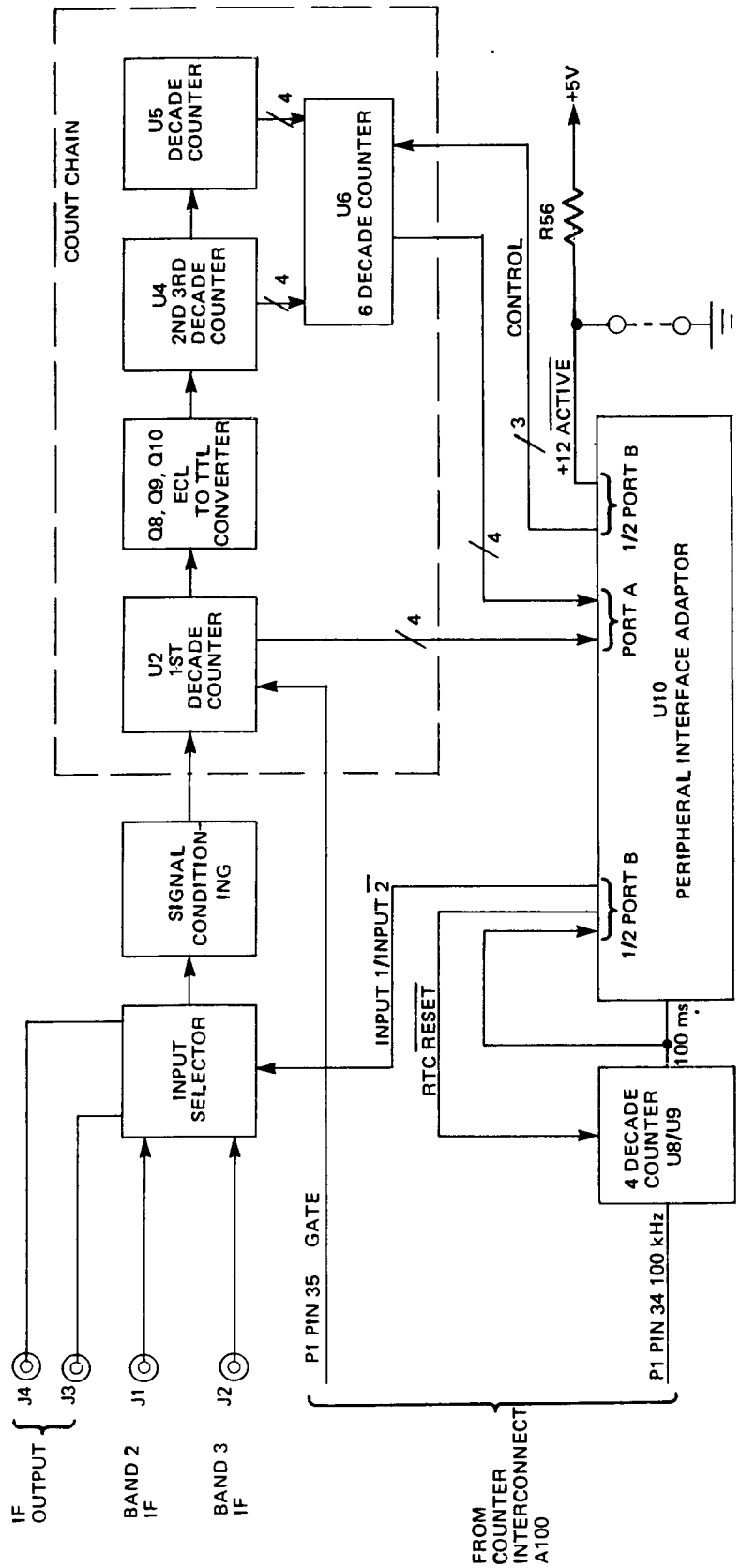


Figure 106a. Count Chain Functional Diagram

A106 COUNT CHAIN ASSY

2020136 - F

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A106	Count Chain Assy	2020136	1		
C1	Tant, 33μF, 20%, 10V	2300015	5	TAG 20 - 33/10 - 50	14433
C2	Cer., .01μF, 20%, 100V	2150003	18	TG - S10	56289
C3	C2				
C4	C1				
C5	Mica, 10pF, 5%, 500V	2260012	1	DM15CD100J03	72136
C6	Tant, 10μF, 20%, 25V	2300029	4	DF106M529	NEC
C7	C2				
C8	C2				
C9	Cer., .001μF, 20%, 1KV	2150001	3	5GA - D10	56289
C10	C2				
C11	C2				
C12	C9				
C13	C2				
C14	C6				
C15	C6				
C16	C2				
C17	C9				
C18	Not Used				
C19	Not Used				
C20	C1				
C21	C2				
C22	C1				
C23	Not Used				
C24 thru C28	C2				
C29	C1				
C30 thru C33	C2				
C34	C6				
CR1	General Purpose	2704154	3	IN4154	07263
CR2	Zener, 6.2V	2705234	1	IN5234	04713
CR3	CR1				
CR4	Tunnel, Switching	2710033	1	G00010C	20754
CR5	Hot Carrier	2710016	1	5082 - 2835	28480
CR6	CR1				
CR7	Not Used				
L1	Part of Board				
L2	Inductor, 1μH	3510003	1	DD-0.10	72259
Q1	PNP, RF	4704959	1	2N4959	04713
Q2	NPN, RF SW	4710017	3	MMT3960	04713
Q3	Q2				
Q4	PNP, RF	4710010	1	MPS - H81	04713
Q5	NPN, RF	4710024	1	BFR90	73445
Q6	NPN, RF	4710026	1	NE73432B	0000S
Q7	Q2				
Q8	NPN, RF	4705179	3	2N5179	04713
Q9	Q8				
Q10	Q8				
Q11	PNP, General Purpose	4704126	2	2N4126	04713
Q12	Q11				

A106 COUNT CHAIN ASSY, continued

2020136-F

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R1	Comp., 1.5K, 5%, 1/4 W	4010152	2	RC07GF152J	81349
R2	Comp., 6.2K, 5%, 1/4 W	4010622	2	RC07GF622J	81349
R3	Comp., 51 ohm, 2%, 1/4 W	4130510	3	C4/2%/51	24546
R4	Comp., 5.1K, 5%, 1/4 W	4010512	2	RC07GF512J	81349
R5	Comp., 2.7K, 5%, 1/4 W	4010272	2	RC07GF272J	81349
R6	Comp., 51 ohm, 5%, 1/4 W	4010510	1	RC07GF510J	81349
R7	Met Ox, 2K, 2%, 1/4 W	4130202	3	C4/2%/2K	24546
R8	Comp., 510 ohm, 5%, 1/4 W	4010511	1	RC07GF511J	81349
R9	Comp., 5.6 ohm, 5%, 1/4 W	4010569	5	RC07GF5R6J	81349
R10	R5				
R11	R9				
R12	Met Ox, 68 ohm, 2%, 1/4 W	4130680	1	C4/2%/68	24546
R13	Met Ox, 43 ohm, 2%, 1/4 W	4130430	1	C4/2%/43	24546
R14	Met Ox, 3.9K, 2%, 1/4 W	4130392	1	C4/2%/3.9K	24546
R15	R7				
R16	R4				
R17	R1				
R18	R2				
R19	Comp., 100 ohm, 5%, 1/4 W	4010101	1	RC07GF101J	81349
R20	Met Ox, 56 ohm, 2%, 1/4 W	4130560	2	C4/2%/56	24546
R21	R9				
R22	R20				
R23	Comp., 430 ohm, 5%, 1/4 W	4010431	1	RC07GF431J	81349
R24	R9				
R25	Met Ox, S.A.T. (2K, 2% Nom)	4130999	1	C4/2%/XX	24546
R26	Met Ox, 39 ohm, 2%, 1/4 W	4130390	2	C4/2%/39	24546
R27	Met Ox, 200 ohm, 2%, 1/4 W	4130201	3	C4/2%/200	24546
R28	Met Ox, 270 ohm, 2%, 1/4 W	4130271	1	C4/2%/270	24546
R29	R3				
R30	R3				
R31	Comp, 10 ohm, 5%, 1/4 W	4010100	2	RC07GF100J	81349
R32	Met Ox, 47 ohm, 2%, 1/4 W	4130470	1	C4/2%/47	24546
R33	Met Ox, 20 ohm, 2%, 1/4 W	4130200	1	C4/2%/20	24546
R34	Met Ox, 510 ohm, 2%, 1/3 W	4130511	1	C4/2%/510	24546
R35	R9				
R36	Met Ox, 1K, 2%, 1/4 W	4130102	3	C4/2%/1K	24546
R37	R26				
R38	Comp., 390 ohm, 5%, 1/4 W	4010391	1	RC07GF391J	81349
R39 thru R42	Comp, 10 K, 5%, 1/4 W	4010103	4	RC07GF103J	81349
R43	Met Ox, 20 K, 2%, 1/4 W	4130203	4	C4/2%/20K	24546
R44	R43				
R45	R36				
R46	R43				
R47	Met Ox, 18 ohm, 2%, 1/4 W (NOM) SAT	4130999	1	C4/2%/18	24546
R48	R43				
R49	Met Ox, 240 ohm, 2%, 1/4 W	4130241	1	C4/2%/240	24546
R50	R27				
R51	R27				
R52	R36				
R53	Met Ox, 430 ohm, 2%, 1/4W.	4130431	1	C4/2%/431	24546

A106 COUNT CHAIN ASSY, continued

2020136-F

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R54	R7				
R55	Comp., 1.8K, 5%, 1/4 W	4010182	1	RC07GF182J	81349
R56	Comp., 4.7K 5%, 1/4 W	4010472	1	RC07GF472J	81349
R57	R31				
TP1 thru TP10	Conn., Pin, .040D	2620032	10	460-2970-0203	71279
U1	Dual/Diff Ampl	3043049	1	CA3049T	07263
U2	UHF, BCD, Decade Counter	3010637	1	SP8637B	0000C
U3	Op Amplifier	3040741	1	LM741CN	0000X
U4	PST Decade Counter	3084196	1	SN74LS196N	01295
U5	4 Bit Decade Counter	3084160	1	SN74LS160N	01295
U6	6 Dec. Ctr/8 Dec. Latch	3057031	1	LS74031	01295
U7	Hex Inverter	3087404	1	DM74LS04N	0000X
U8	Decade Counter	3084490	2	74LS490N	01295
U9	U8				
U10	Periph. Interface Adapter	3086820	1	MC6820	04713

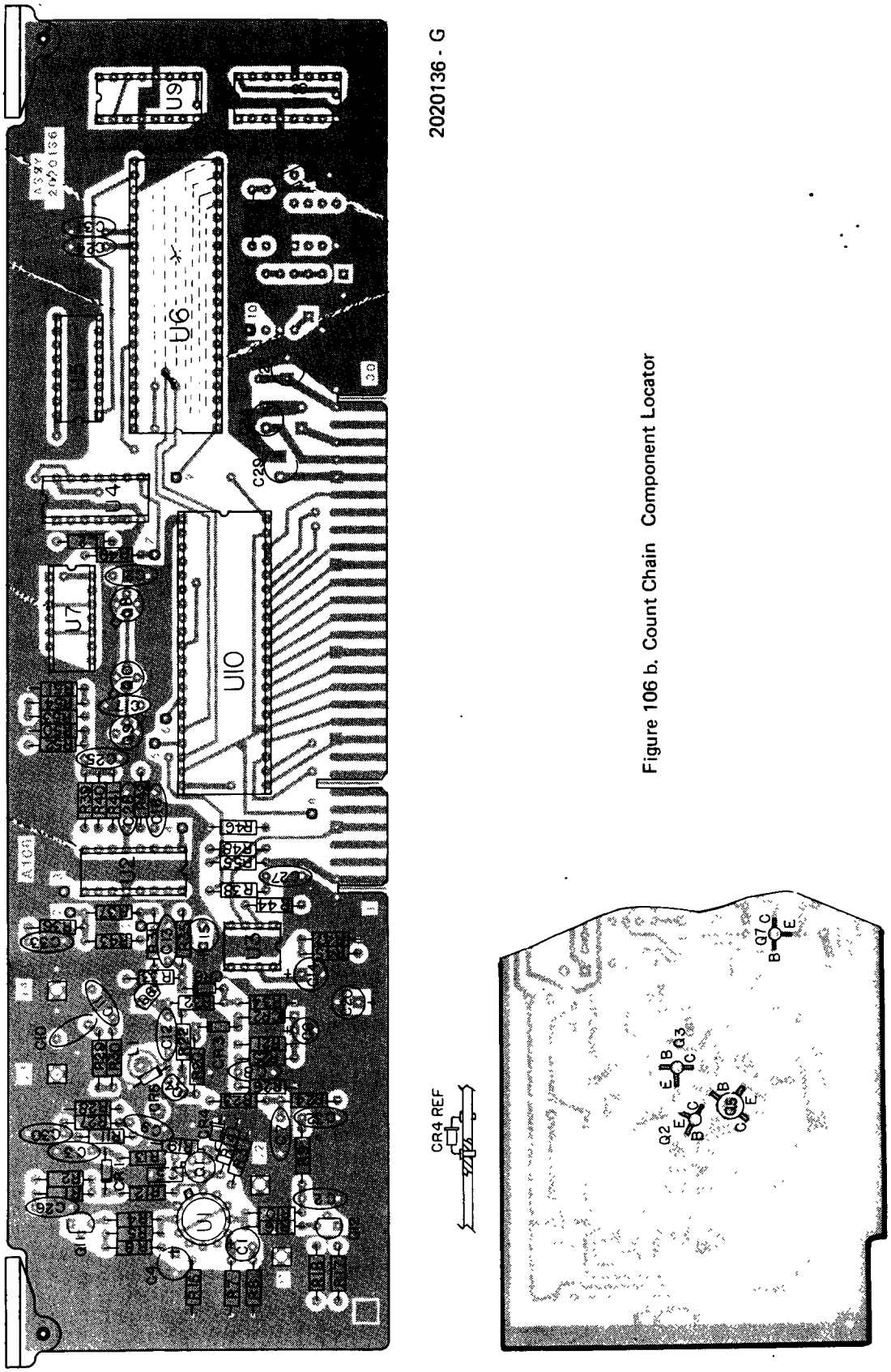
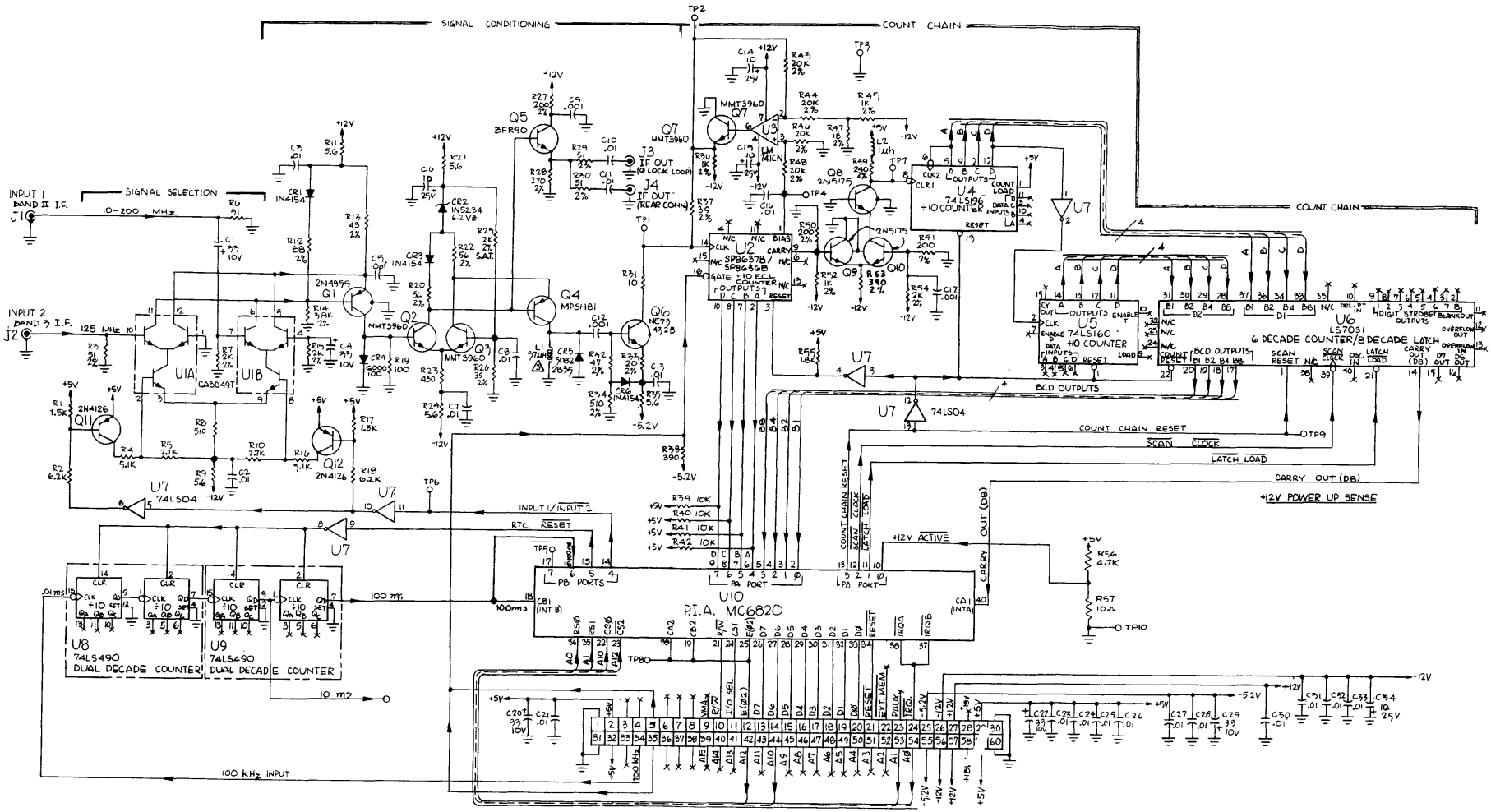


Figure 106 b. Count Chain Component Locator



I.C. NO	TYPE	PIN NO			
		GND	+5V	-5.2	-12V
U1	CA3049T				
U2	SP8637B	12		5	
U3	LM741CN				
U4	74LS196	7	14		
U5	74LS160	8	16		
U6	74LS7031	23	27		26
U7	74LS04	7	14		
U8,U9	74LS490	8	16		
U10	MC6820	1	20		

LAST REF. NO. USED	NOT USED
C34	
C66	
L2	
R87	
TP10	
Q12	
U10	
J4	

⚠ INDUCTOR PART OF P.C. BOARD.

5500136 - G

Figure 106 c. Count Chain Schematic

A107
GATE GENERATOR
(2020137)

This assembly performs the following functions.

- Reference Oscillator Control
- Gate Generation
- Band 3 Amplitude Determination
- Power Meter Control (Option 02 only)

REFERENCE OSCILLATOR CONTROL

This circuit selects, as the time base for the counter, either the internal reference oscillator or an external 10 MHz signal applied to the rear panel. This circuit provides a 100 kHz TTL level clock signal for the gate generator, a 50 kHz TTL level clock signal for the microwave converter and, in the internal oscillator mode, a 10 MHz signal (1 volt p-p into 50 ohms) to the rear panel.

The 10 MHz internal reference signal is applied to a switchable "analog to TTL" converter (Q1, Q2, Q3). When the Ref Int/Ext line is high the TTL converter is enabled. One output goes to drive Q4, giving a square wave (1V p-p into 50 ohms) on the 10 MHz Ref line. A second output goes to NAND gate U1 (also switchable for signal isolation). The output of U1 goes to the clock input of U2. U2 is a dual decade divider that divides by 100. The output of U2 is a 100 kHz TTL clock signal to the gate generator. The output of U2 also goes through inverter U7 to one half of U17 and provides a 50 kHz TTL signal for the microwave converter.

When the Reference Int/Ext line is set to external (low) the TTL converter (Q1, Q2, Q3) and driver (Q4) are disabled, TTL converter (Q5, Q6, Q7) is enabled, and U1 is set to select the external input. An external reference signal applied to the 10 MHz reference line is then converted to the input of U2.

GATE GENERATOR

The Gate Generator must provide an accurate, stable, signal gate to the Count Chain. The gate must be switchable, in decade increments, between 100 micro sec and 1 sec. The gate generator consists of a programmable divide-by-N time base (U5), a dual flip-flop (U6A, U6B), and an ECL flip flop (U8). The divide ratio of U5, which determines the gate time, is set by U5 pins 12, 13, and 14 as follows.

Pin 12	Pin 13	Pin 14	Divide Ratio	Gate Time
0	0	1	10^1	100 μsec
0	1	0	10^2	1 Msec
0	1	1	10^3	10 Msec
1	0	0	10^4	100 Msec
1	0	1	10^5	1 sec

The outputs of U5 and U6 enable ECL flip-flop U8, but U8 is clocked directly from the 100kHz clock to insure gate accuracy.

When the gate is not active, U5 is permitted to free-run by holding U6A clear (T0). The gate is initialized by setting U6A. This clears U6B and clears U5 (T1). The next clock pulse sets U8 (T2). The gate is then enabled by momentarily clearing U6A (T3). The next clock sets U6B which enables U5 and U8 (T4). At T5 the gate is opened and U5 begins counting clocks (T5). Halfway through the gate, U5 pin 1 goes high (T6). After U5 has accumulated the proper number of clocks its output, pin 1, goes low. This sets U6A, which clears U6B, and sets U8 pin 7 high (T7). The next clock closes the gate (T8). The program next clears U6A (T9), which enables the gate to free-run again (T0). See figure 107a.

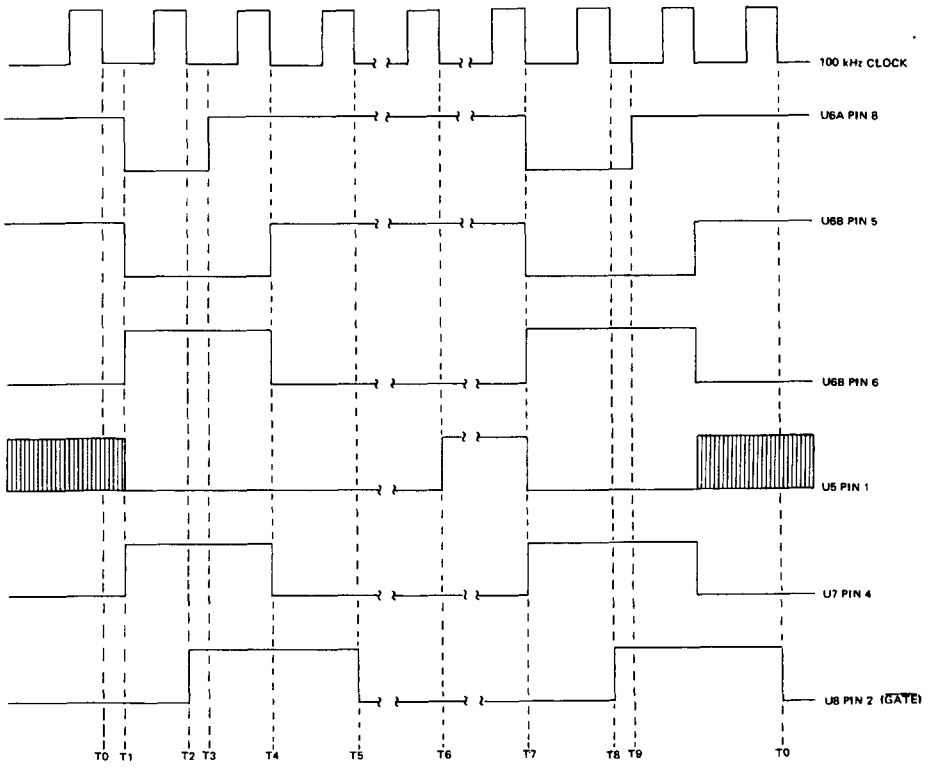


Figure 107a. Gate Generator Timing Diagram

BAND 3 AMPLITUDE DETERMINATION

This circuit consists of three main parts.

- THE POWER METER ZERO DAC is used to automatically zero offsets in the Power Meter. It consists of two 8 bit latching DACs (U3, U4), and a comparator (U14A). All the latching DACs are driven in parallel by shift register U16, with the appropriate DAC being written to by the four write lines (U15, pins 2, 4, 6, 8). The coarse DAC (U3) has a range of ± 200 micro amps, and the fine DAC (U4) has a range of ± 1.5 amps. The Power Meter Zero DAC is adjusted such that, on 1 step U14A is not set, but on the next step U14A is set. This adjusts the input to U14 to 0 volts, nulling any offsets in the power meter curcuit.

- THE POWER METER consists of a 15 dB switchable gain stage (U9), an 8 bit DAC used as a variable attenuator (U10), a 100 mV comparator (U14B), and a latch (half of U17). Two variable attenuators are used, on counters equipped with the option 02 power meter, to provide greater resolution (U10, U12).

  When the detected signal from the microwave converter enters U9 the power meter is first set for maximum gain and minimum attenuation. Next the latch (U17) is reset. If the input to the comparator (U14B) is greater than 100mV, latch U17 will be set. The signal amplitude to the comparator is then reduced, and the process is repeated until latch U17 no longer gets set. The input amplitude can then be calculated from the switch and DAC settings. On counters without the power meter option the amplitude is calculated to a 3dB resolution. On counters with the power meter option the amplitude is calculated to a resolution of 0.1dB.

- The POWER METER PROM (Option 02 only) contains a logic comparator (U21), a 2K X 8 prom (U20), and a bus driver (U19). The logic comparitor is connected to the microprocessor address bus, and is configured to decode the 2K address range from 4000 Hex to 47FF Hex. The comparator output drives the chip select of the Prom, and the bus driver. The prom contains the Power Meter program as well as the power correction factors. Bus driver U19 is used as a buffer for driving the microprocessor data bus.

PERIPHERIAL INTERFACE ADAPTER (PIA)

The Peripherial Interface Adapter (U18) is used as the microprocessor I/O port. It has an address range from 9900 Hex to 9903 Hex. Peripheral Port A is at address 9900, and Peripheral Port B is at address 9902.

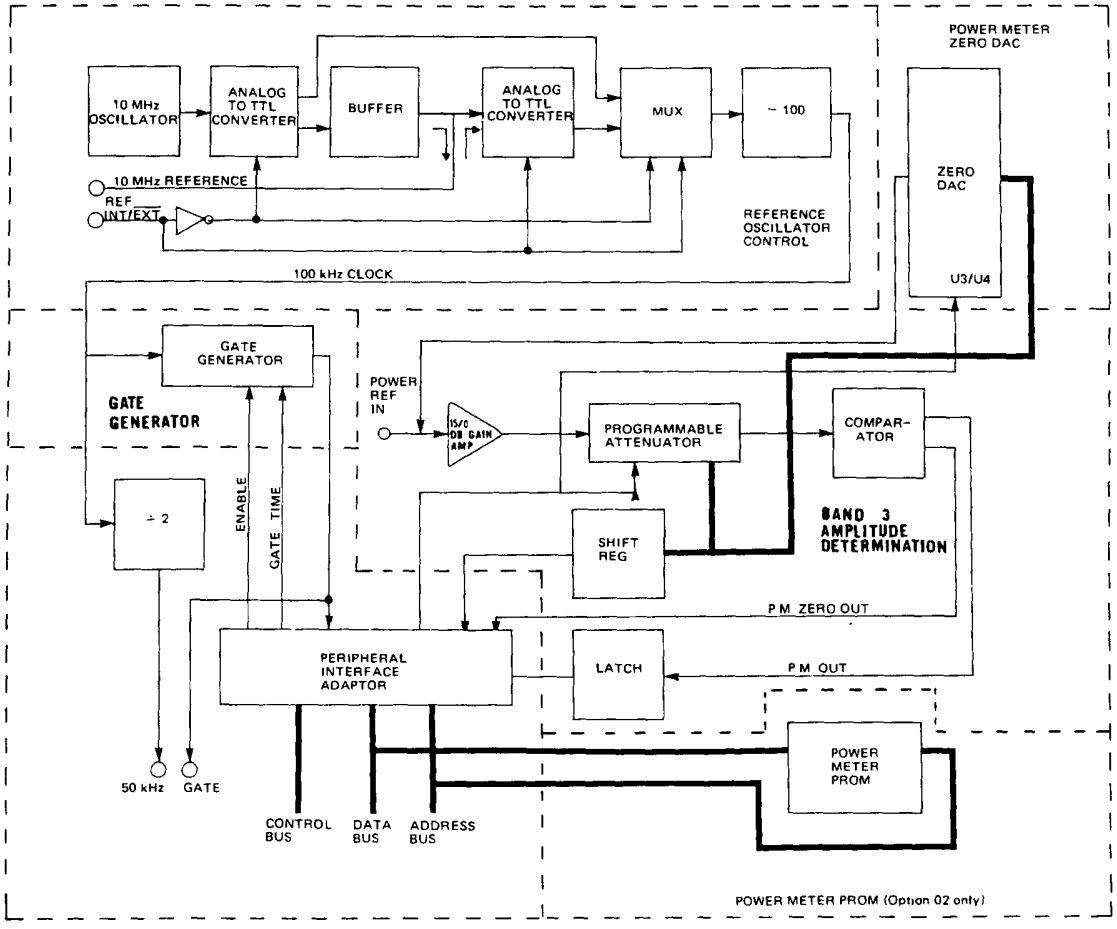


Figure 107b. Gate Generator Block Diagram

A107 GATE GENERATOR

2020137 - L

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A107	Gate Generator Assy	2020137	1	EIP	
	A112 Crystal Oscillator Assy	2030002	1	EIP	
C1	Cer, .01μF, 20%, 100V	2150003	14	TGS10	72982
C2	C1				
C3	Tant, 33μF, 20%, 10V	2300015	4	TAG20 - 33/10 - 50	14433
C4 thru C7	C1				
C8	Mica, 22pF, 5%, 500V	2260017	1	ED220J03	72136
C9	Tant, 1.0 μF, 20%, 35V	2300008	1	TAG20-1.0/35-50	14433
C10	Mica, 33pF, 5%, 500V	2260021	1	ED330J03	72136
C11	Mica, 100pF, 5%, 500V	2260034	1	ED101J03	72136
C12	C10				
C13 thru C15	C1				
C16	Tant, 10μF, 20%, 25V	2300029	2	NECDF106M25S	
C17	C1				
C18	C3				
C19	C3				
C20	C1				
C21	C1				
C22	C3				
C23	C1				
C24	C1				
C25	C16				
CR1	Hot Carrier	2710004	1	FH1100	07263
CR2	Hot Carrier	2710006	1	5082 - 2800	
CR3	Not Used (Option 02 only)				
CR4	Zener, 6.2V	2700827	1	IN827	
Q1	NPN, General Purpose	4704124	4	2N4124	
Q2	PNP, General Purpose	4704126	3	2N4126	
Q3	Q1				
Q4	Q2				
Q5	Q1				
Q6	Q2				
Q7	Q1				
Q8	D-MOS FET SW	4710031	1	2D215	
R1	Comp, 1K, 5%, 1/4 W	4010102	2	RC07GF102J	81349
R2	Comp, 200, 5%, 1/4 W	4010201	2	RC07GF201J	81349
R3	Comp, 620, 5%, 1/4 W	4010621	2	RC07GF621J	81349
R4	Comp, 2.2K, 5%, 1/4 W	4010222	2	RC07GF222J	81349
R5	Comp, 220, 5%, 1/4 W	4010221	2	RC07GF221J	81349
R6	Comp, 510, 5%, 1/4 W	4010511	2	RC07GF511J	81349
R7	R2				
R8	Comp, 27, 5%, 1/4 W	4010270	1	RC07GF270J	81349
R9	Comp, 300, 5%, 1/4 W	4010301	1	RC07GF301J	81349
R10	Comp, 4.7K, 5%, 1/4 W	4010472	6	RC07GF472J	81349
R11	R1				
R12	Comp, 390, 5%, 1/4 W	4010391	1	RC07GF391J	81349
R13	R10				
R14	R4				
R15	R5				

A107 GATE GENERATOR, continued

2020137 - L

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R16	R6				
R17	R3				
R18	Met Ox, 5.6K, 2%, 1/4 W	4130562	1	C4/2%/5.6K	24546
R19	Comp, 3.3K, 5%, 1/4 W	4010332	1	RC07GF333J	81349
R20	Met Ox, 27 ohm, 2%, 1/4 W	4130270	1	C4/2%/27	24546
R21	Comp, 2.7K, 5%, 1/4 W	4010272	1	RC07GF272J	81349
R22	R10				
R23	R10				
R24	Comp, 1.5K, 5%, 1/4 W	4010152	2	RC07GF152J	81349
R25	R24				
R26	Comp, 1.6K, 5%, 1/4 W	4010162	1	RC07GF162J	81349
R27	Met Ox, 30K, 2%, 1/4 W	4130303	1	C4/2%/30K	24546
R28	Met Ox, 39K, 2%, 1/4 W	4130393	1	C4/2%/39K	24546
R29	Prec, 1.69K, 1%, 1/10 W	4051691	1	RN55C1691F	81349
R30	Prec, 1.82K, 1%, 1/10 W	4051821	1	RN55C1821F	81349
R31	Prec, 57.6K, 1%, 1/10 W	4055762	1	RN55C5762F	81349
R32	Comp, 36K, 5%, 1/4 W	4010363	1	RC07GF363F	81349
R33	Comp, 15K, 5%, 1/4 W	4010153	1	RC07GF153F	81349
R34 thru R39	Comp, 6.2K, 5%, 1/4 W	4010622	6	RC07GF622J	81349
R40	Met Ox, 750, 2%, 1/4 W	4130751	1	C4/2%/750	24546
R41	Prec, 6.19K, 1%, 1/8 W	4056191	1	RN55C6191F	81349
R42	Prec, 100, 1%, 1/8 W	4051000	1	RN55C1000F	81349
R43	R10				
R44	R10				
R45	Met Ox, 10K, 2%, 1/4 W (Option 01 only)	4130103	2	C4/2%/10K	24546
R46	R45				
U1	Quad Schmitt NAND	3084132	1	SN4LS132	01295
U2	Dual Decade Counter	3084490	1	SN74LS490N	01295
U3	8 Bit DAC	3057524	3	AD7524JN	
U4	U3				
U5	Digital P Chan. MOS Divider	3035009	1	MK5009P	
U6	D Type Pos Flip-flop	3087474	2	SN74LS74N	01295
U7	Quad 2INP NOR Gate	3087402	1	SN74LS02N	01295
U8	Digital Dual D Flip-flop	3110131	1	MC10131L	04713
U9	Dual Low Noise Op Amp	3045532	1	NE5532	
U10	8 Bit DAC (Option 02 only)	3057525	2	AD7524LN	
U10	U3				
U11	Op Amplifier	3040308	2	LM308AN	
U12	U10 (Option 02 only)				
U13	U11				
U14	Comparator	3050393	1	LM393N	
U15	Hex Buffer/Driver	3007407	1	DM7407N	27014
U16	Dual 4 Bit Static S/R	3034015	1	MC14015B	04713
U17	U6				
U18	Periph. Interface Adaptor	3086820	1	MC6821	01295
U19	Oct. Buffer (Option 02 only (-08))	3084244	1	SN74LS244	01295
U20	Power Meter PROM (Option 02 only (-08))	6400001	1	MCM2716	04713
U21	6 Bit Comparator (Option 02 only (-08))	3078136	1	DM8136	27014

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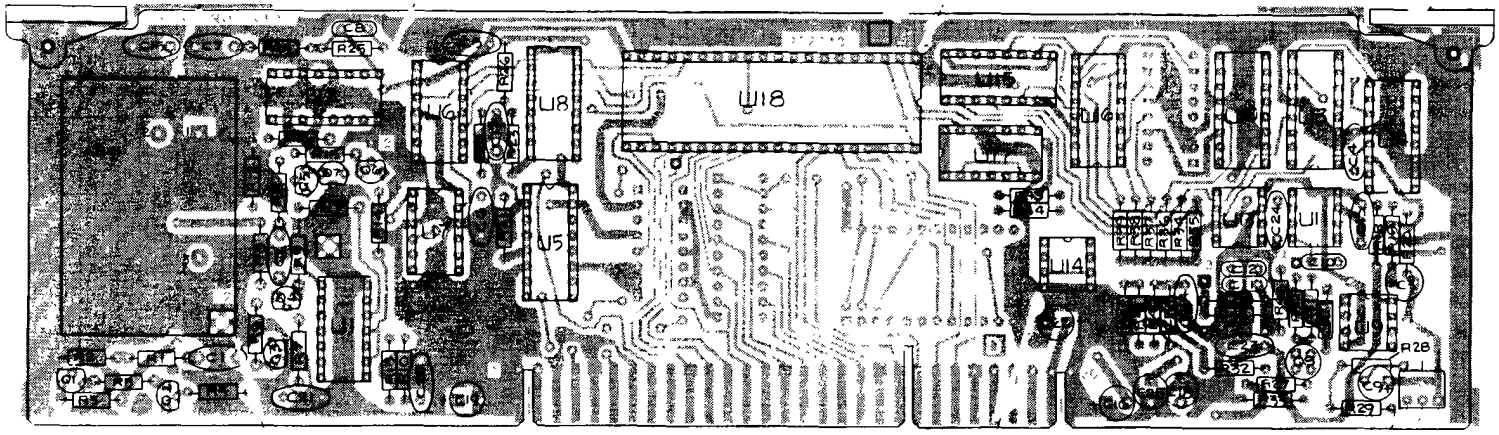
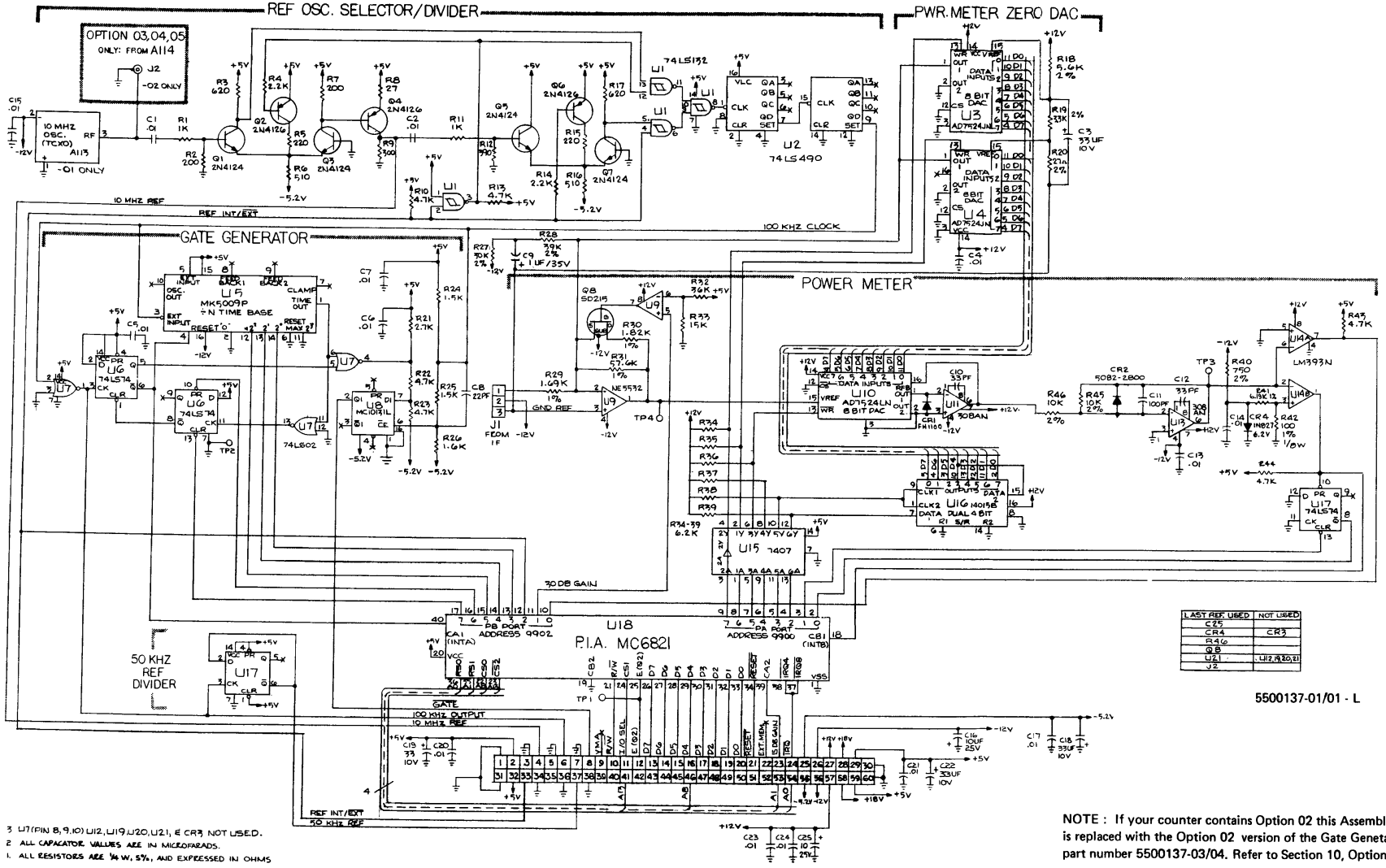


2020137-01/02 - P

Figure 107 c. Gate Generator Component Locator

NOTE : If the counter contains option 02 this board is replaced with the 2020137-03/04.
Refer to Section 10, Option 02 for the -03/04 version of the Gate Generator Assy.



LAST REF. USED	NOT USED
C25	
CR4	CR3
R46	
Q8	
U21	U12,19,20,21
J2	

3. U7 (PIN 8, 9, 10) U12, U19, U20, U21, & CR3 NOT USED.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
1. ALL RESISTORS ARE ¼ W, 5%, AND EXPRESSED IN OHMS

NOTE : If your counter contains Option 02 this Assembly is replaced with the Option 02 version of the Gate Genetator part number 5500137-03/04. Refer to Section 10, Option 02.

Figure 107 d. Gate Generator Schematic

A108
CONVERTER CONTROL
(2020138)

The Converter Control provides a precise YIG tuning current which is controlled by the microprocessor via PIA U5. It will also phase lock the VCO (A201A) in the Microwave Converter (A203) to a selected harmonic of a 50kHz reference signal so that it will provide a synthesized LO. The converter control assembly also permits the microprocessor to control the LO power amplifier and provide the microprocessor input for the IF Threshold signal.

FREQUENCY CONTROL DAC and YIG DRIVER

The yig tuning current is supplied by the yig driver (U3, Q1, Q2, & Q3) which is controlled by the DAC. The DAC is composed of a 12 bit monolithic DAC (U1), summing amplifier (U2) and resistors (R3, R4, R7, & R8) to provide a total resolution of 14 bits. R4 and R5 are pull up resistors for PA ports 0 and 1 of the PIA (U5) which directly drive the 2 least significant bits of the DAC. A change in the least significant bit of the DAC corresponds to a yig frequency change of 2MHz. A voltage analog of yig current appears across R20, and is compared to the DAC output at the summing junction of U3, with resistors R10 and R18.

The slope of yig current vs DAC voltage is adjustable using R11, and the offset is adjusted using R14.

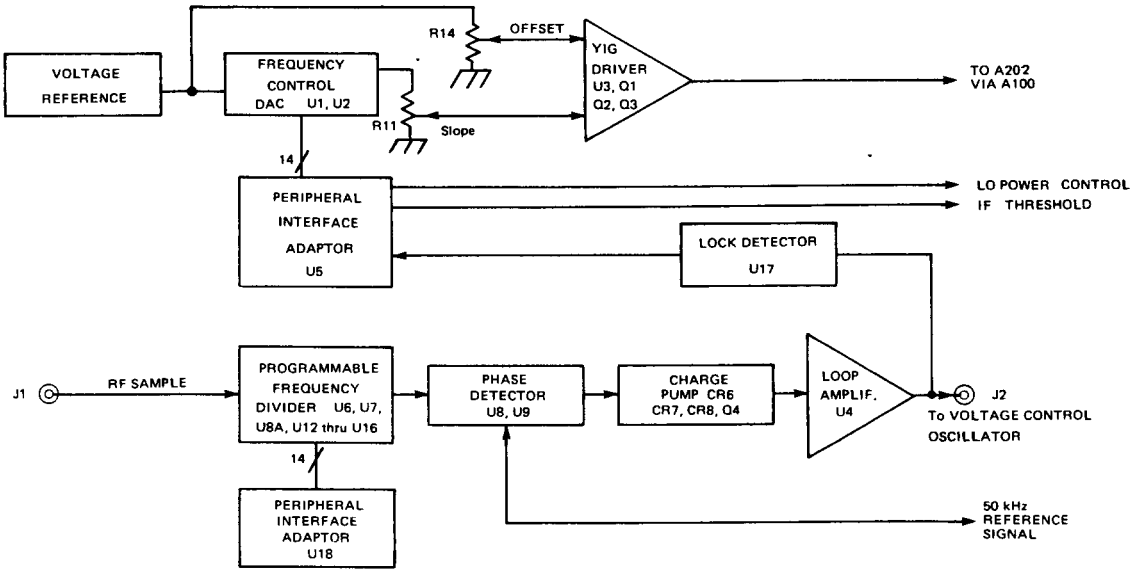


Figure 108a. Converter Control Block Diagram

VCO CONTROL

The VCO control circuitry and the VCO (A201A) from a phase lock loop frequency synthesizer. The synthesizer frequency range is 370MHz to 500MHz.

An output signal from the VCO (A201A), via a buffer amplifier on the Band 2 Converter (A109), is applied to the programmable frequency divider (U6, U7, U8A, U10 thru U16). The frequency divider is programmed by the microprocessor (A105) via PIA U18. The output of the frequency divider is compared to the 50kHz reference signal from the gate generator (A107) by the phase detector (U8, U9). A phase difference between the divided down VCO and the 50 kHz reference will result in an output from the phase detector. The phase detector has two output ports, a pump-up port and a pump-down port. Pump down is U8D pin 11. It is normally low, and goes high to reduce the VCO frequency. Pump-up is U9 pin 13. It is normally high, and goes low to increase the VCO frequency.

The outputs of the phase detector go to the charge pump, which converts them to a single tri-state output. The charge pump output is open with no pump command, sources about 2 mA with pump down, and sinks about 2 mA with pump up. The output of the charge pump is connected to the input of the loop amplifier (U4). The loop amplifier provides the proper gain and filtering to achieve the desired loop response. The output of the loop amplifier is the VCO tuning voltage. If the tuning voltage should fall out of the range of −2.25V to + 9.50V, the output of window detector (U17) will go low to indicate that phase lock has been lost.

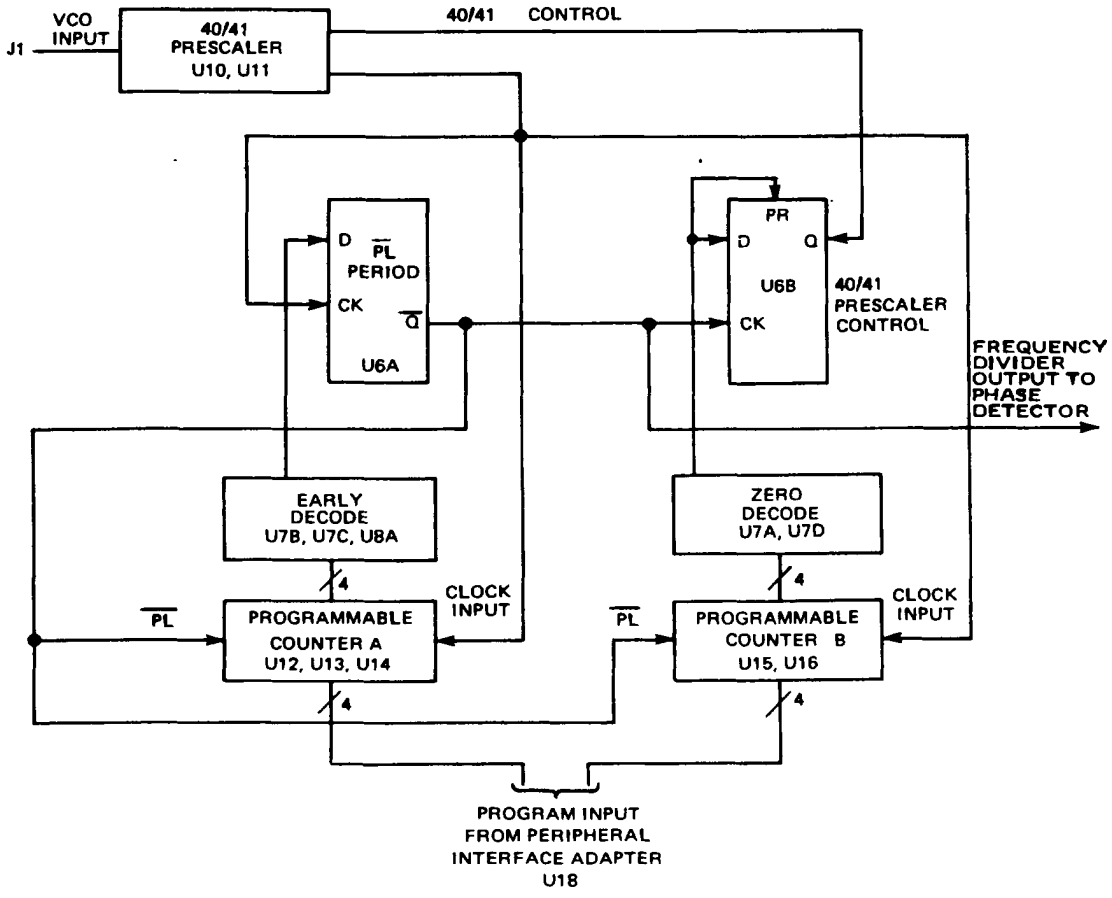


Figure 108b. Programmable Frequency Divider Block Diagram

PROGRAMMABLE FREQUENCY DIVIDER

The programmable frequency divider uses a two modulus (divide number) prescaler (U10, U11) and two programmable counters (A & B). The prescaler is used to divide the VCO frequency down to a lower frequency which can be handled by low power schottky TTL programmable counters. The two modulus prescaler permits prescaling without loss of resolution. At the start of the programmable frequency divider cycle, the prescaler is set to divide by the larger modulus (41), and both programmable counters have been loaded with their respective program numbers from the PIA (U18). The programmable counters each decrement 1 count for each output pulse from the prescaler. When programmable counter B (U15, U16) reaches the count of zero the 40/41 control flip-flop (U6B) changes state and causes the prescaler to divide by the lower modulus (40). When programmable counter A reaches the count of 2 the D input of the PL period flip-flop (U6A) goes high, so that on the count of 1 the flip-flop changes state, which causes both programmable counters to be reloaded with their respective program numbers and the 40/41 control flip-flop to reset (prescaler in ÷ 41 state). The very next count causes the PL period flip-flop to reset, starting the programmable frequency divider cycle over again. The equation for the divide ratio of the programmable frequency divider N_d is:

$$N_d = 40\ (N_{\text{counter A}}) + N_{\text{counter B}}$$

will the condition that:

$$N_{\text{counter B}} \text{ must not exceed } N_{\text{counter A}}$$

The weighting of the command bits is:

U12 P_1 – 400MHz	U14 P_1 – 4MHz
U12 P_0 – 200MHz	U14 P_0 – 2MHz
U13 P_3 – 160MHz	U15 P_3 – 1.6MHz
U13 P_2 – 80MHz	U15 P_2 – 0.8MHz
U13 P_1 – 40MHz	U15 P_1 – 0.4MHz
U13 P_0 – 20MHz	U15 P_0 – 0.2MHz
U14 P_3 – 16MHz	U16 P_1 – 100KHz
U14 P_2 – 8MHz	U16 P_0 – 50KHz

A108 CONVERTER CONTROL

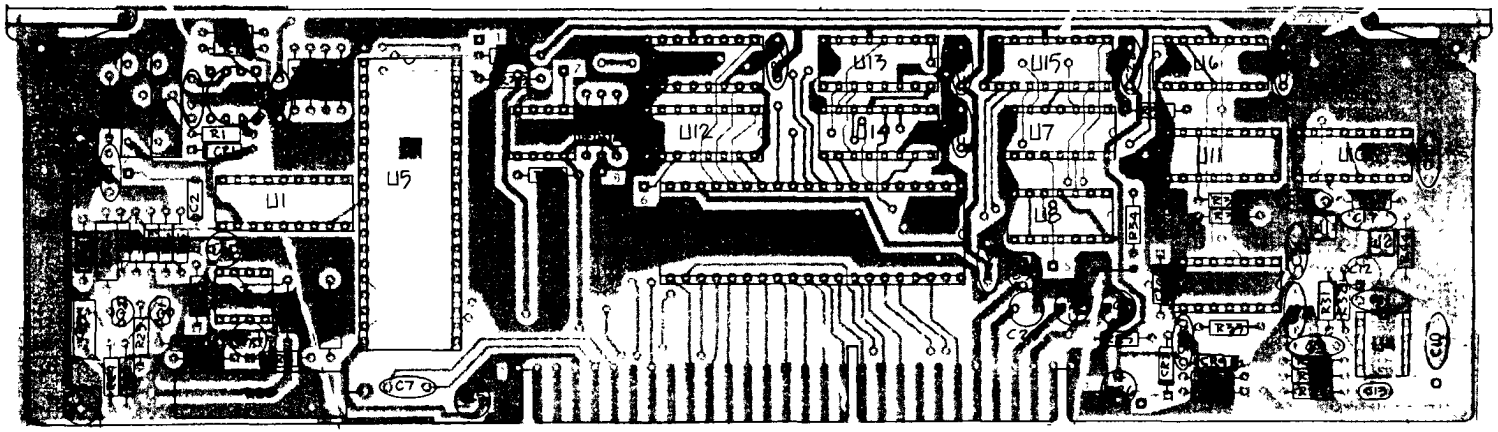
2020138-N

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A108	Converter Control Assy	2020138	1	EIP	
C1	Cer, .01μF, 20%, 100V	2150003	14	TG - S10	56289
C2	Mono, .022μF, 15%, 50V	2350027	1	2130X7R050R223K	26654
C3	C1				
C4	Cer, .005μF, 20%, 100V	2150008	1	TG - D50	56289
C5	Tant, 1μF, 10%, 35V	2300008	3	TAG20 - 1/35V	14433
C6	C5				
C7	Cer, .001μF, 20%, 1KV	2150001	4	SGA - D10	56289
C8	C1				
C9	C7				
C10	C1				
C11	C1				
C12	Tant, .47μF, 10%, 35V	2300005	1	TAG20 - .47/35	14433
C13	Cer, .047μF, 20%, 50V	2150016	1	6123X7R473KA50	26654
C14	C1				
C15	Not Used				
C16	C1				
C17	C7				
C18	C7				
C19 thru C24	C1				
C25	Tant, 33μF, 10%, 10V	2300015	3	TAG20 - 33/10V	14433
C26	C25				
C27	C5				
C28	Tant, 10μF, 20%, 25V	2300029	2	DF106M259	72136
C29	C28				
C30	C25				
C31	C1				
CR1	Zener, 6.2V	2700827	1	1N827	07263
CR2	Hot Carrier	2710004	1	FH1100	07263
CR3	General Purpose	2704154	5	1N4154	07263
CR4	Zener, 51V	2704757	1	1N4757	07263
CR5	Rectifier	2704001	1	1N4001	07263
CR6 thru CR8	CR3				
CR9	CR3				
J1	Mini Jack	2610038	2	S1 - 451 - 0000	98291
J2	J1				
Q1	NPN, General Purpose	4704124	1	2N4124	04713
Q2	PNP, Amplifier	4710018	1	MPSLS1	04713
Q3	PNP,	4710009	1	MJE350	04713
R1	Comp, 750, 5%, 1/4 W	4010751	1	RC07GF751J	81349
R2	Comp, 10K, 5%, 1/4 W	4010103	4	RC07GF103J	81349
R3	Comp, 82K, 5%, 1/4 W	4010823	1	RC07GF823J	81349
R4	Comp, 160K, 5%, 1/4 W	4010164	1	RC076F164J	81349
R5	R2				
R6	R2				
R7	Comp, 824K, 5%, 1/4 W	4010824	1	RC07GF824J	81349
R8	Comp, 1K, 5%, 1/4 W	4010102	3	RC07GF102J	81349
R9	Cmt Film, 4.99M, 1%	4120017	1	CC4994F	01121
R10	Prec, 8.4K, 1%,	4120019	1	VAR - 1/10C - 61%, 8.45K	
R11	Var, Cer, MT, 20K	4280011	2	89PR - 20K	

A108 CONVERTER CONTROL, continued

2020138-N

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R12	Prec, 49.9K, 1%, 1/4 W	4054992	1	RN55C4992F	81349
R13	Met Ox, 10K, 2%, 1/4 W	4130103	2	C4/2%/10K	24546
R14	R11				
R15	Prec, 1meg, 1%, 1/10 W	4051004	1	RN55C1004F	81349
R16	R13				
R17	Comp, 4.7K, 5%, 1/4 W	4010472	1	RC07GF472J	81349
R18	Prec, 3.01K, 1%, 1/10 W	4120020	1	UAR - 1/10 - C6 - 1% - 3.01K	
R19	Met Ox, 1.6K, 2%, 1/4 W	4130162	1	C4/2%/1.6K	24546
R20	Wire Wound, 5, 1%, 7 W	4110003	1	T7 (10PPM)	
R21	Met Ox, 390, 2%, 1/4 W	4130391	2	C4/2%/390	24546
R22	R21				
R23	R8				
R24	R8				
R25	Comp, 3.9K, 5%, 1/4 W	4010392	1	RC07GF392J	81349
R26	Comp, 5.1K, 5%, 1/4 W	4010512	2	RC07GF512J	81349
R27	Comp, 51, 5%, 1/4 W	4010510	2	RC07GF510J	81349
R28	Factory Select		1		
R29	Comp, 470, 5%, 1/4 W	4010471	1	RC07GF471J	81349
R30	R26				
R31	Comp, 1.5 meg, 5%, 1/4 W	4010155	1	RC07GF155J	81349
R32	Comp, 220K, 5%, 1/4 W	4010224	1	RC07GF224J	81349
R33	Comp, 680, 5%, 1/4 W	4010681	1	RC07GF681J	81349
R34	Comp, 300, 5%, 1/4 W	4010301	1	RC07GF301J	81349
R35	R27				
R36	Comp, 390, 5%, 1/4 W	4010391	3	RC07GF391J	81349
R37	R36				
R38	R36				
R39	R2				
R40	Met Ox, 1K, 2%, 1/4 W	4130102	1	C4/2%/1K	24546
R41	Met Ox, 4.7K, 2%, 1/4 W	4130472	1	C4/2%/4.7K	24546
R42	Met Ox, 47K, 2%, 1/4 W	4130473	2	C4/2%/47K	24546
R43	Met Ox, 3.9K, 2%, 1/4 W	4130392	1	C4/2%/3.9K	24546
R44	R42				
R45	Comp, 6.2K, 5%, 1/4 W	4010622	1	RC07GF622J	81349
TP1 thru TP8	Pin, .04D, Gold	2620032	8	460 - 2970 - 02 - 03	71279
U1	12 Bit DAC	3057541	1	AD7541KN	0000X
U2	Prec, J FET, Op Amplifier	3041016	1	OP16F	06665
U3	Op Amplifier	3040741	1	LM741CN	0000X
U4	Op Amplifier - BI/FET	3040341	1	TL071CP	0000X
U5	Peripheral Interface Adaptor	3086820	2	MC6820	04713
U6	Dual "D" Flip-flop	3070014	1	SN74LS74	01295
U7	2 INP NOR Buffer	3070016	1	DM74S02N	01295
U8	2 IMP NAND Gate	3087400	1	DM74LS00N	0000X
U9	Phase Freq. Detector	3014044	1	MC4044P	04713
U10	Two-Mod Prescaler (-02)	3112013	1	MC12013L	04713
U11	Digital Dual "D" Flip-flop	3110131	1	MC10131P	0000X
U12 thru U15	UP/DN Counter	3084192	4	DM74LS192N	0000X
U16	UP/DN Counter	3084193	1	DM74LS193N	0000X
U17	Comparator	3050393	1	LM393	0000X
U18	U5				



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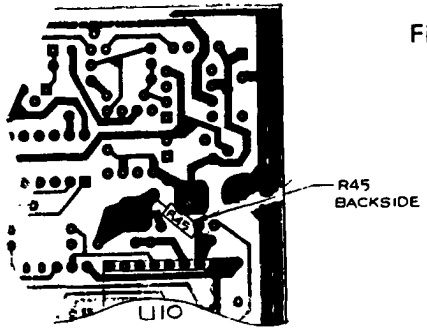
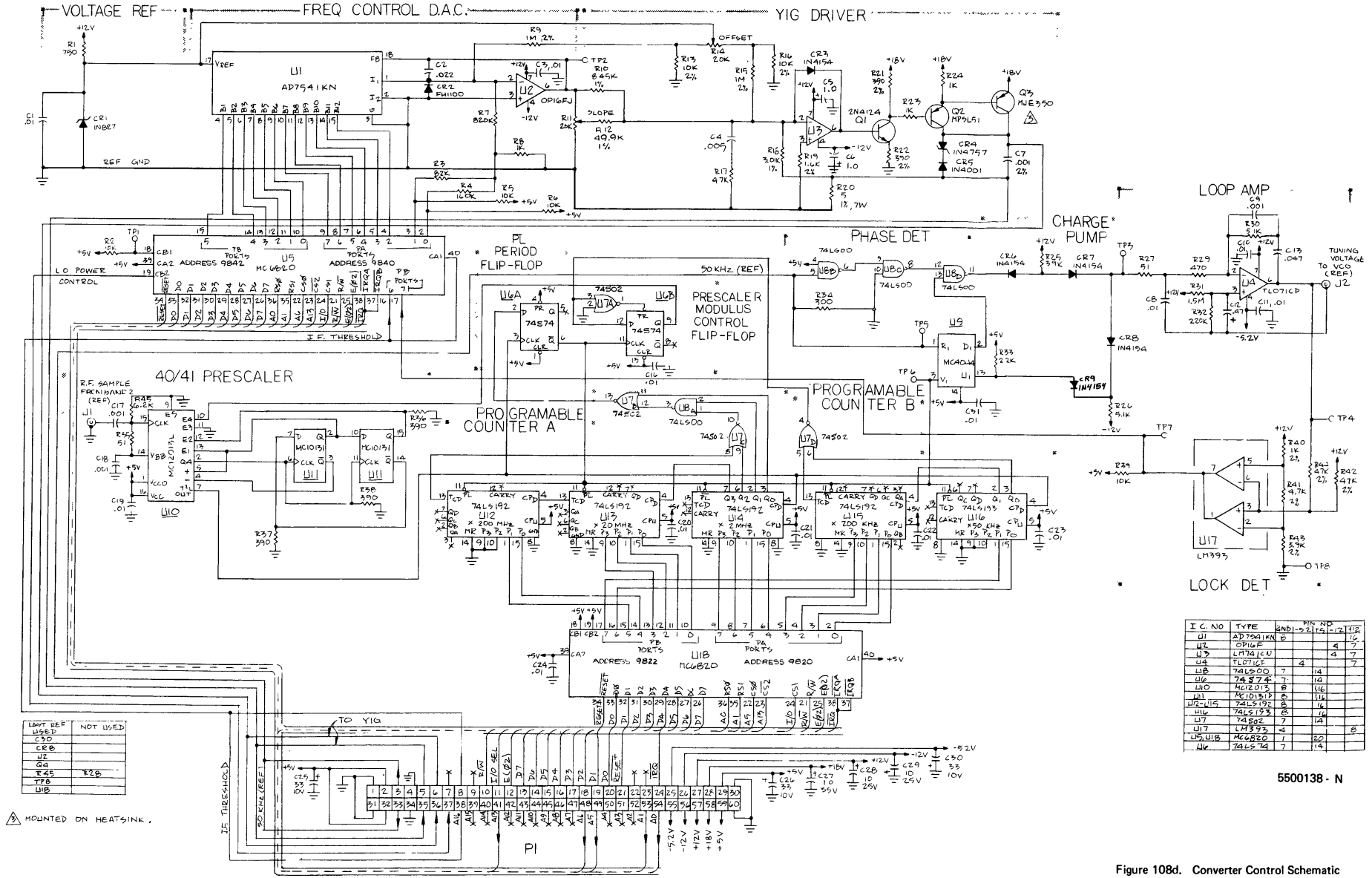


Figure 108c. Converter Control Component Locator



I.C. NO	TYPE	PIN NO GND	-5.2	+5	+12	+18
U1	AD7541KN	8				16
U2	OP16F			4	7	
U3	LM741CN			4	7	
U4	TL071CP	4			7	
U5,U8	74LS00	7		14		
U6	74S74	7		14		
U10	MC12013	8		16		
U11	MC10131P	8		16		
U12-U15	74LS192	8		16		
U16	74LS193	8		16		
U17	74S02	7		14		
U17	LM393	4				8
U5,U18	MC6820	1		20		
U6	74LS74	7		14		

5500138 - N

Figure 108d. Converter Control Schematic

A109
BAND 2 CONVERTER
(2020139)

The Band 2 Converter accepts Band 1 and Band 2 RF signals from the front panel, and local oscillator (LO) signal from the Band 3 Converter (A203). The appropriate signal is selected and processed to produce an IF signal between 10 Hz and 200 MHz. The IF signal output is sent to the Count Chain board (A106), and lock information is routed through the PIA (peripheral interface adapter) U2 to the Microprocessor (A105).

IMPEDANCE CONVERTER

Band 1 input from the front panel enters the converter at J6 and is terminated by R75. The signal is coupled to the input of a field effect transistor (FET) amplifier (Q15) through an RC network (R73, C42). Two limiter diodes (CR4, CR5) protect the FET against large input signals. The FET is a source follower with slightly less than unity gain. The FET drives a buffer amplifier (Q14) which has enough gain to increase the impedance converter overall gain to near unity. A decoupling capacitor (C39) controls the amplifiers low frequency cutoff, and C41 provides high frequency peaking to keep the gain flat to frequencies above 100 MHz.

SIGNAL SELECT

The output of the impedance converter circuit drives one input of the signal select circuitry. Signal selection is made by enabling one of three differential amplifiers, U4A, U4B, or U5A. When Band 1 is selected, a logic high signal on the PIA (U2 pin 2) turns on Q16. Q16 biases on the current source in U4A. This current source generates an 11ma current which is split between the two differential amplifier transistors in U4A. The currents from pins 5 and 6 flow through matched collector loads (R94, L7/R95, L8). R94 and R95 are equal, and are selected for the proper low frequency gain during board alignment. Inductors L7 and L8 provide peaking to give an approximate flat gain through 200MHz. Diodes CR9 and CR10 provide limiting on very strong signals to prevent the next stage from being over driven.

The next stage is a differential amplifier similar to U4A, but it is driven differentially. To generate a single ended output signal, one output of U5B (pin 12) is passed through a current mirror (Q18). The output of the current mirror is then added to the second output of U5B (pin 11) at J5. The load for this stage is a 51 ohm resistor located on the A106 Count Chain board in order to terminate the coax for RF signals. In the quiescent state, the current from Q18 equals the collector current of the differential amplifier U5B, and the output current is zero. When a signal is applied, the current will be unbalanced to generate a signal at the load resistor. To provide frequency compensation of the current mirror, an RC network (R108, C34) is connected between the emitter of Q18 and ground.

BAND 1 LOCK DETECTOR

The output signal at J5 is coupled to detector CR12. Amplifier U6 is a threshold comparator that will produce a logic low signal when the IF output from J5 is more than –6dBm. The output of U6 goes through a resistor divider network to generate a 5V TTL logic signal for the PIA. R90 provides about 1 dB of positive feedback at threshold level to prevent eratic output from the comparator.

ISOLATION AMPLIFIER

The Band 2 input signal enters on J4. This RF signal is terminated in 50 ohms by the combination of R1 and the input impedance of the amplifier. The input signal level is detected by CR1, filtered by C3, and applied to one input of the Band 2 lock detector (U1).

The isolation amplifier is a common base amplifier with a gain of −10 dB. An input signal range of +10 to −20dBm is translated to a 0 to −30dBm range into the mixer so the mixer will be in its linear range for all signal input levels. The amplifier peaks slightly near 1 GHz to overcome an increase in mixer conversion loss at these frequencies.

MIXER OPERATION

The local oscillator (LO) is applied to the IF terminal and the IF is removed from the LO terminal. This swap allows the mixer (MX1) to be unbalanced and act as a low loss attenuator for signals between 10MHz and 200MHz where no mixing is necessary. The mixer has a nominal 400MHz LO for signals between 200MHz and 600MHz; and has a nominal 800MHz LO for signals between 600MHz and 1GHz. A 980MHz LO allows operation with input signals to 1160MHz.

IF AMPLIFIER

The output of the mixer drives an IF amplifier through a 7 section, 200MHz low-pass filter. The IF amplifier is a "feedback pair" amplifier whose gain is stabilized by feedback, to be equal to 24dB. Inductor L6 is used to extend the high frequency response to 200MHz. The 1 pF capacitor (C26) between R34 and R35 is a low pass filter to reduce the 1200 to 1500 MHz LO harmonics that reach the IF amplifier.

BAND 2 LOCK DETECTOR

The IF amplifier output goes to the signal select circuit and to the Band 2 Lock Detector. The Band 2 Lock Detector has a voltage proportional to the IF level on the positive input, and a voltage proportional to the RF signal on the Negative input. The conversion gain from RF input to IF amplifier output is a +6dB for all valid signals, and less than −6dB for all spurious signals. The output of U1 is positive only when a valid IF signal is present. A small offset is added by R12 and R13 to guarantee a non lock condition when no signal is present. Resistor R90 provides about 1dB of positive feedback to prevent eratic output from noise at the point of threshold.

LO BUFFER

The VCO signal from the Band 3 Converter (A201A, J2) enters on J1. The signal goes through a 6 dB attenuator (R111, R112, R114), and a low pass filter (L1, C63, C64 to attenuate high order harmonics), and is terminated by a 51 ohm resistor (R16). Two high input impedance signal splitters (Q2, Q3) get their input signals from R16. Q2 and Q3 operate on the same basic principal. One output is taken from the emitter (acting as an emitter follower) which provides unity gain for the input signal. The AC terminating impedance on the emitter is adjusted to be 50 ohms so the amplifier will act as a unity gain amplifier for the 50 ohm load which terminates the collector when a coax cable is connected. U2 has an additional transformer (T1) in its collector lead to increase the signal output to J3 by about 4 dB.

DIVIDE-BY-TWO

The emitter output of Q3 drives the input of a divide-by-two IC (U3). The impedance is held at 50 ohms by two terminating/biasing resistors (R61, R62). The resistors keep the input bias to U3 below the emitter-coupled logic (ECL) low level (approx. −2.0V). The microprocessor enables self-test by putting a low level signal on pin 5 of the PIA (U2). This turns on Q13, and raises the voltage at U3 pin 7 to the center of an ECL signal (approx. −1.2V). This allows U3 to divide the input signal by two. The output of U3 goes to the signal select circuits.

LO SELECT

The signal from the emitter of Q2 drives the LO select circuitry. The LO provides one (of three) signals to the mixer (MX1). In Band 2A a bias current is generated to unbalance the mixer and allow signals below 190MHz to pass. In Band 2B a 370MHz or 425MHz LO signal is generated that will mix with signals of 200 to 600MHz, and provide the 10 to 200MHz IF signal desired. In Band 2C a 750MHz, 850MHz or 980MHz LO signal is generated to mix with input signals between 600MHz and 1160MHz to provide the desired IF signal.

In Band 2A, the 3ma current to bias mixer MX1 is generated when Q12 is turned on by the PIA, to apply +12V to MX1 through R57. This will allow signals to pass that are less than the cutoff frequency of the low pass filter (200MHz). The LO signal to mixer MX2 from Q2 is not allowed to pass MX2 because of the inherent balance of the mixer. No signal can enter pin 2 of MX2 because Q7 has been saturated, removing bias from buffer Q5, and shunting any RF signals to ground.

When Band 2B is selected, Q12 is turned off thus balancing mixer MX1; Q6 is turned on to unbalance mixer MX2. With MX2 unbalanced, the LO signal from Q2 can pass through MX2 and be amplified by Q10 and Q11, and be applied to mixer MX1.

When Band 2C is selected both Q6 and Q12 are off, and both mixers are balanced. In this mode Q7 is shut off and an LO signal is applied to pin 1 and 2 of MX2. The sum output of MX2 is selected by a DC blocking capacitor (C31). This sum (that is two times the incoming LO frequency) is amplified by Q10 and Q11 and applied to MX1.

The Q10 and Q11 amplifier is a series shunt pair. Q10 applies most of the RF input signal across the emitter resistor R47. This determines the transistor emitter current, which will be the collector current if the output is terminated in a low impedance. Q11 is used as a current-to-voltage converter. The output voltage of this converter is the product of the input current times the feedback resistor (R51). Since the input of this stage is a summing junction, it appears very close to zero ohms to the previous stage, Q10. The voltage gain of the two transistors can be approximated by R51/R47, which is about 3 or 10dB. Since the gain required at 800MHz is slightly greater than required at 400MHz, a low pass matching network (consisting of L2 and C20 peaks the output signal current to MX1 at 800 MHz. The remaining components around Q10 and Q11 are used to bias the transistors. Shunt biasing is used to provide collector bias voltages of 3.4V for Q10, and 4.7V for Q11.

OPTION SELECTION

Provision has been made on this assembly for a set of jumpers that will let the microprocessor know when it has the components required for a 548 (26.5GHz) counter, and if it has an extended frequency option (Option 06). These jumpers are read by the microprocessor when the counter is turned on, and will select micro code which is applicable only when those options are available. A jumper from E1 to E3 (from pins 8 and 9 on the PIA U2) indicate that this is a 548 counter. A jumper from E2 to E4 indicates that Option 06 (Band 4) has been installed in the counter.

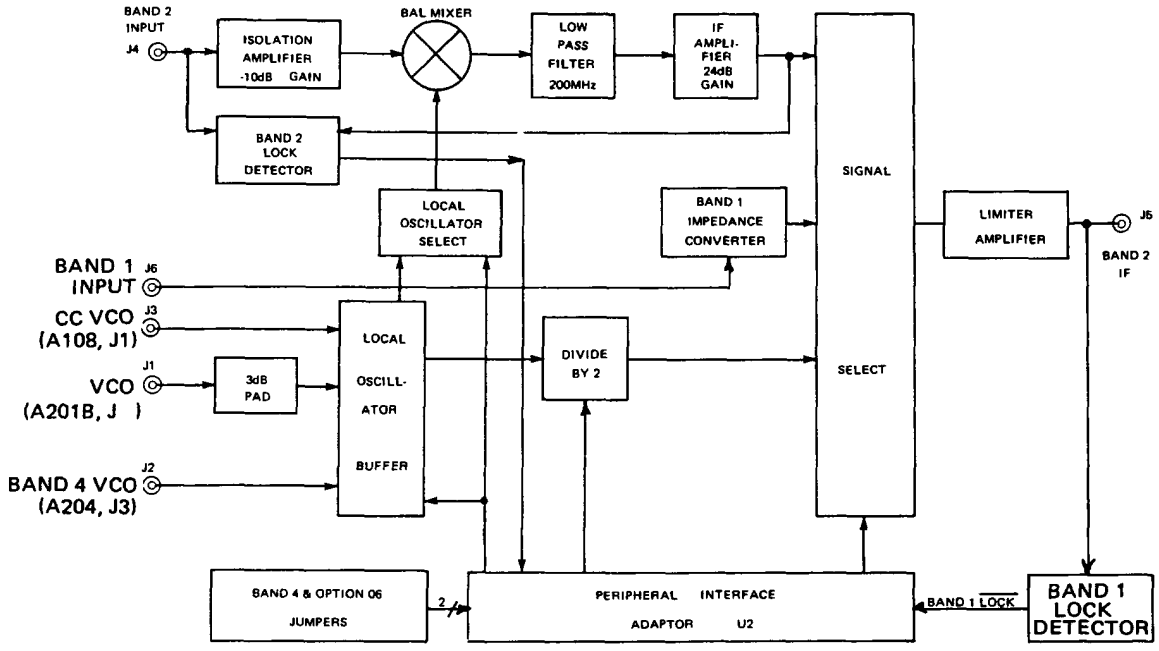


Figure 109a. Band 2 Converter Block Diagram

A109 BAND 2 CONVERTER

2020139-L

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A109	Band 2 Converter Assy	2020139	1	EIP	
C1	Cer, .01μF, 10%, 100V	2150014	9	6123X7R103KA100	26654
C2	C1				
C3	Cer, .001μF 10%, 100V	2150015	11	6183X7R102KA100	26654
C4 thru C6	C1				
C7	Mica, 100pF, 5%, 500V	2260034	3	FD101J03	72136
C8	Disc, .001μF, 20%, 1KV	2150001	8	SGA - D10	56289
C9	Disc, .01μF, 20%, 100V	2150003	11	TG - S10	56289
C10	C8				
C11	C8				
C12	C7				
C13	C8				
C14	C7				
C15 thru C18	C3				
C19	C8				
C20	Mica, 1pF, 5%, 500V	2260005	2	CD010C03	56289
C21	Mica, 18pF, 5%, 500V	2260015	3	CD180J03	56289
C22	Mica, 33pF, 5%, 500V	2260021	2	ED330J03	56289
C23	C22				
C24	C21				
C25	C1				
C26	C20				
C27	Not Used				
C28	C1				
C29	C9				
C30	C1				
C31	C3				
C32	C3				
C33	C1				
C34 thru C36	C3				
C37	C9				
C38	C3				
C39	Tant, 100μF, 20%, 6.3V	2300024	1	TAG20 - 47/6.3 - 50	14433
C40	C9				
C41	Mica, 22pF, 5%, 500V	2660017	1	ED220J03	72136
C42	Mica, 47pF, 5%, 500V	2260004	1	DM10 - 470J	72136
C43	Tant, 33μF,10%, 10V	2300015	6	TAG20 - 33/10 - 50	14433
C44	C9				
C45	C43				
C46	C8				
C47 thru C49	C9				
C50	Tant, 10μF, 20%, 25V	2300029	3	DF106M258	14433
C51	C43				
C52	C9				
C53	C9				
C54	C21				
C55	C8				
C56	C8				
C57	C50				

A109 BAND 2 CONVERTER, continued

2020139-L

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
C58	C43				
C59	C9				
C60	C43				
C61	C50				
C62	C43				
C63	Mica, 8pF, 5%, 500V	2660011	2	CD080J03	56289
C64	C63				
CR1	Mix UHF	2710038	2	ND4991	00005
CR2	Not Used				
CR3	CR1				
CR4	General Purpose	2704154	3	1N4154	07263
CR5	CR4				
CR6	Not Used				
CR7	Not Used				
CR8	Not Used				
CR9	Not Used				
CR10	Not Used				
CR11	CR4				
CR12	CR1				
L1 thru L5	Part of Board				
L6	Inductor, 0.47 =H	3510014	1	1025 - 10	99800
L7	L1				
L8	L1				
MX1	Balanced Mixer	2030016-00	2	TFM-2	
MX2	MX1				
Q1	NPN, RF	4710030	9	BFR-90	04713
Q2	Q1				
Q3	Q1				
Q4	PNP, General Purpose	4704124	1	2N4124	04713
Q5	Q1				
Q6	PPNP, General Purpose	4704126	6	2N4126	04313
Q7 thru Q11	Q1				
Q12	Q6				
Q13	Q6				
Q14	NPN, RF	4710023	2	A5T4261	01295
Q15	NN-Channel, JFET	4704416	1	2N4416	04713
Q16	Q6				
Q17	Q6				
Q18	Q14				
Q19	Q6				
R1	Comp, 150, 5%, 1/4 W	4010151	1	RC07GF151J	81349
R2	Met Ox, 75, 2%, 1/4 W	4130750	2	C4/2%/75	24546
R3	Comp, 1.1K, 5%, 1/4 W	4010112	1	RC07GF112J	81349
R4	Comp, 820, 5%, 1/4 W	4010821	3	RC07GF821J	81349
R5	Comp, 33, 5%, 1/8 W	4000330	1	RC05GF330J	81349
R6	Comp, 51, 5%. 1/4 W	4000510	1	RC05GF510J	81349
R7	Comp, 10K, 5%. 1/4 W	4010103	3	RC07GF103J	81349
R8	Met Ox, 8.2K, 2%, 1/4 W	4130822	2	C4/2%/822	81349
R9	Met Ox, 30K, 2%, 1/4 W	4130303	1	C4/2%/30K	24546
R10	Met Ox, 43K, 2%, 1/4 W	4130433	2	C4/2%/43K	24546
R11	Comp, 43K, 5%, 1/4 W	4010433	1	RC07GF433J	81349
R12	Met Ox, S.A.T., Nom, 15K	4130999	1	C4/2%/15K	24546
R13	Met Ox, 12, 2%, 1/4 W	4130120	1	C4/2%/12	24546

A109 BAND 2 CONVERTER, continued

2020139-L

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R14	Comp, 36, 5%, 1/4 W	4010360	1	RC07GF36J	81349
R15	Comp, 11, 5%, 1/4 W	4010110	2	RC07GF110J	81349
R16	Met Ox, 51, 2%, 1/4 W	4130510	2	C4/2%/51	24546
R17	Comp, 1K, 5%, 1/4 W	4010102	5	RC07GF102J	81349
R18	R4				
R19	R15				
R20	R17				
R21	Comp, 220, 5%, 1/4 W	4010221	2	RC07GF221J	81349
R22	Comp, 20K, 5%, 1/4 W	4010203	1	RC07GF203J	81349
R23	R4				
R24	Comp, 10, 5%, 1/8 W	4010100	11	RC07GF100J	81349
R25	Met Ox, 750, 2%, 1/4 W	4130751	2	C4/2%/750	24546
R26	Comp, 11k, 5%, 1/4 W	4010113	3	RC07GF113J	81349
R27	Met Ox, 4.7K, 2%, 1/4 W	4130472	1	C4/2%/4.7K	24546
R28	Met Ox, 33, 2%, 1/4 W	4130330	2	C4/2%/33	24546
R29	Comp, 4.7K, 5%, 1/4 W	4010472	2	RC07GF472J	81349
R30	R26				
R31	Comp, 8.2K, 5%, 1/4 W	4010822	2	RC07GF822J	81349
R32	R7				
R33	R7				
R34	Met Ox, 27, 2%, 1/4 W	4130270	1	C4/2%/27	24546
R35	Met Ox, 24, 2%, 1/4 W	4130240	1	C4/2%/24	24546
R36	R24				
R37	Comp, 10, 5%, 1/8 W	4000100	1	RC05GF100J	81349
R38	R8				
R39	Met Ox, 1K, 2%, 1/4W	4150102	1	C4/2%/1K	24546
R40	Met Ox, 820, 2%, 1/4 W	4130821	2	C4/2%/820	24546
R41	R24				
R42	R16				
R43	R24				
R44	Comp, 910, 5%, 1/4 W	4010911	1	RC07GF911J	81349
R45	Comp, 3.9K, 5%, 1/4 W	4010392	2	RC07GF392J	81349
R46	Comp, 27K, 5%, 1/4 W	4010273	1	RC07GF273J	81349
R47	R28				
R48	Comp, 3.3K, 5%, 1/4 W	4010332	1	RC07GF332J	81349
R49	Comp, 390, 5%, 1/4 W	4010391	1	RC07GF391J	81349
R50	Comp, 13K, 5%, 1/4 W	4010133	1	RC07GF133J	81349
R51	Met Ox, 120, 2%, 1/4 W	4130121	1	C4/2%/120	24546
R52	R24				
R53	R31				
R54	R26				
R55	R25				
R56	R24				
R57	Met Ox, 3.9K, 2%, 1/4 W	4130392	4	C4/2%/3.9K	24546
R58	R17				
R59	R45				
R60	Met Ox, 560, 2%, 1/4 W	4130561	1	C4/2%/561	24546
R61	Met Ox, 82, 2%, 1/4 W	4130820	1	C4/2%/82	24546
R62	Met Ox, 130, 2%, 1/4 W	4130131	2	C4/2%/130	24546
R63	Comp, 510, 5%, 1/4 W	4010511	1	RC07GF511J	81349
R64	Comp, 51, 5%, 1/4 W	4010510	2	RC07GF510J	81349
R65	Comp, 200, 5%, 1/4 W	4010201	1	RC07GF201J	81349
R66	Comp, 160K, 5%, 1/4 W	4010164	1	RC07GF160J	81349
R67	Met Ox, 1.8K, 2%, 1/4 W	4130182	1	C4/2%/1.8K	24546
R68	R24				
R69	Met Ox, 510, 2%, 1/4 W	4130511	2	C4/2%/510	24546
R70	Met Ox, S.A.T. Nom 1.2K	4130999	1	C4/2%/1.2K	24546
R71	R29				
R72	R24				

A109 BAND 2 CONVERTER, continued

2020139 - L

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R73	Comp, 1M, 5%, 1/4 W	4010105	2	RC07GF105J	81349
R74	R6				
R75	R73				
R76	Met Ox, 2.2K, 2%, 1/4 W	4130222	3	C4/2%/2.2K	24546
R77	R57				
R78	Comp, 5.6K, 5%, 1/4 W	4010562	1	RC07GF562J	81349
R79	Comp, 3.6K, 5%, 1/4 W	4010362	3	RC07GF362J	81349
R80	Met Ox, 7.5K, 2%, 1/4 W	4130752	3	C4/2%/7.5K	24546
R81	R76				
R82	R24				
R83	Met Ox, 200, 2%, 1/4 W	4130201	3	C4/2%/200	24546
R84	R57				
R85	Met Ox, 330, 2%, 1/4 W	4130331	1	C4/2%/330	24546
R86	Comp, 6.8K, 5%, 1/4 W	4010682	2	RC07GF682J	81349
R87	R79				
R88	R80				
R89	R8				
R90	Comp, 75K, 5%, 1/4 W	4010753	1	RC07GF753J	81349
R91	Met Ox, 33K, 2%, 1/4 W	4130333	1	C4/2%/33K	24546
R92	Met Ox, 160, 2%, 1/4 W	4130161	1	C4/2%/161	24546
R93	R21				
R94	Met Ox, S.A.T.	4130999	2	12NOM/2%	24546
R95	R94				
R96	R83				
R97	R83				
R98	R57				
R99	R86				
R100	R79				
R101	R80				
R102	R10				
R103	R76				
R104	Comp. 180, 5%, 1/4 W	4010181	1	RC07GF181J	81349
R105	R24				
R106	Met Ox, 91, 2%, 1/4 W	4130910	1	C4/2%/91	24546
R107	R62				
R108	R24				
R109	R69				
R110	R17				
R111	Comp, 160, 5%, 1/4 W	4010161	2	RC07GF161J	81349
R112	R111				
R113	R94, S.A.T.				
R114	Met Ox, 2K, 2%, 1/4 W	4130202	1	C4/2%/2K	24546
R115	R114				
R116	Met Ox, 9.1K, 2%, 1/4 W	4130912	1	C4/2%/9.1K	24546
R117	R116				
T1	RF Transformer Assy	4910001	1	EIP	
TP1 thru TP16	Conn, Pin, .04D	2620032	16 1	460 - 2970 - 02 - 03	71279
U1	Prec, JFET Op Amplifier	3041016	1	OP16FJ	06665
U2	Periph. Interface Adaptor	3086820	1	MC6820	04713
U3	750MHz, D-Type Flip Flop	3001106	1	11C06	07263
U4	Dual/Diff. Amplifier	3043049	2	CA3049	0000X
U5	U4				
U6	Op Amplifier	3040741	1	LM741CN	0000X

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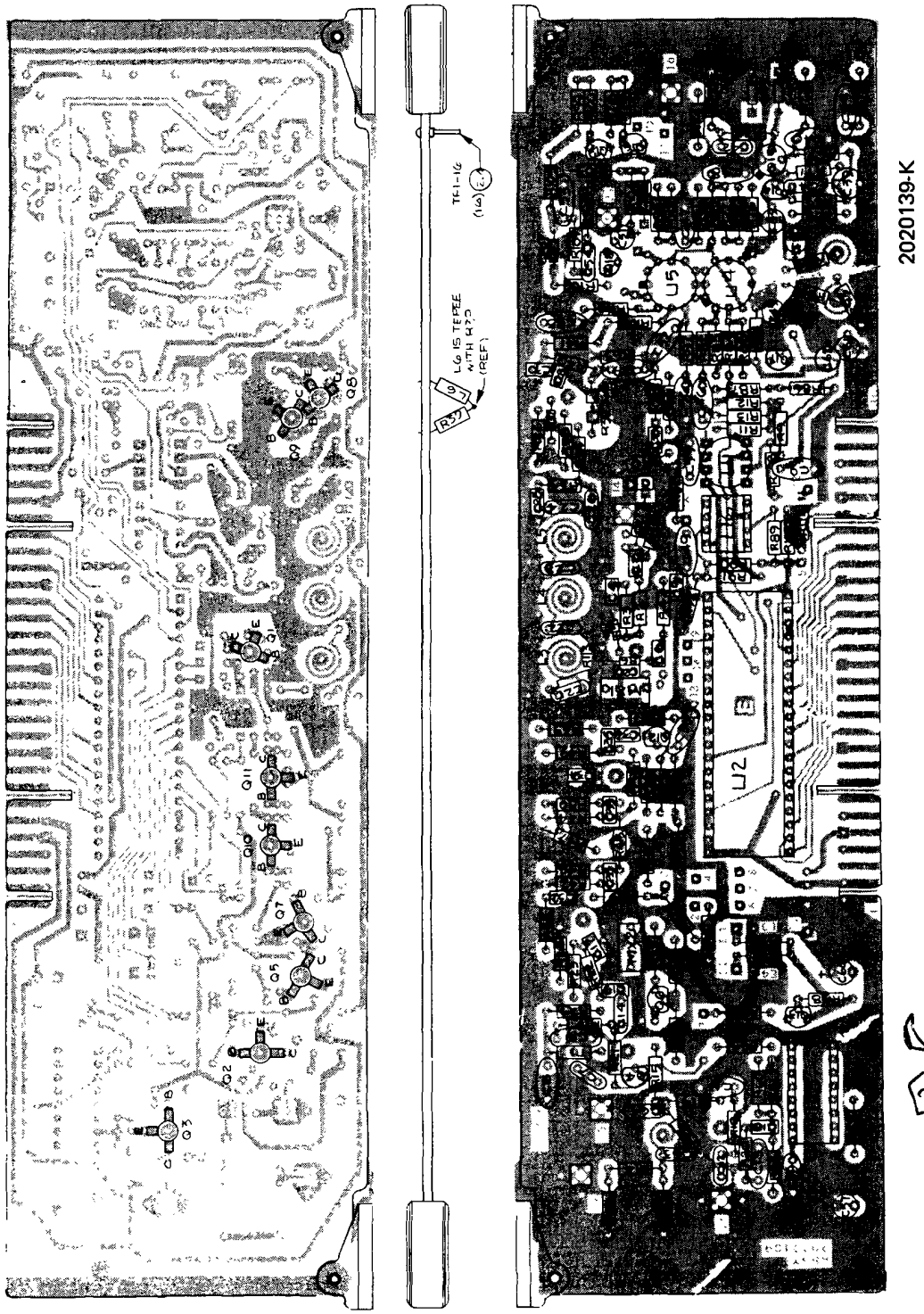
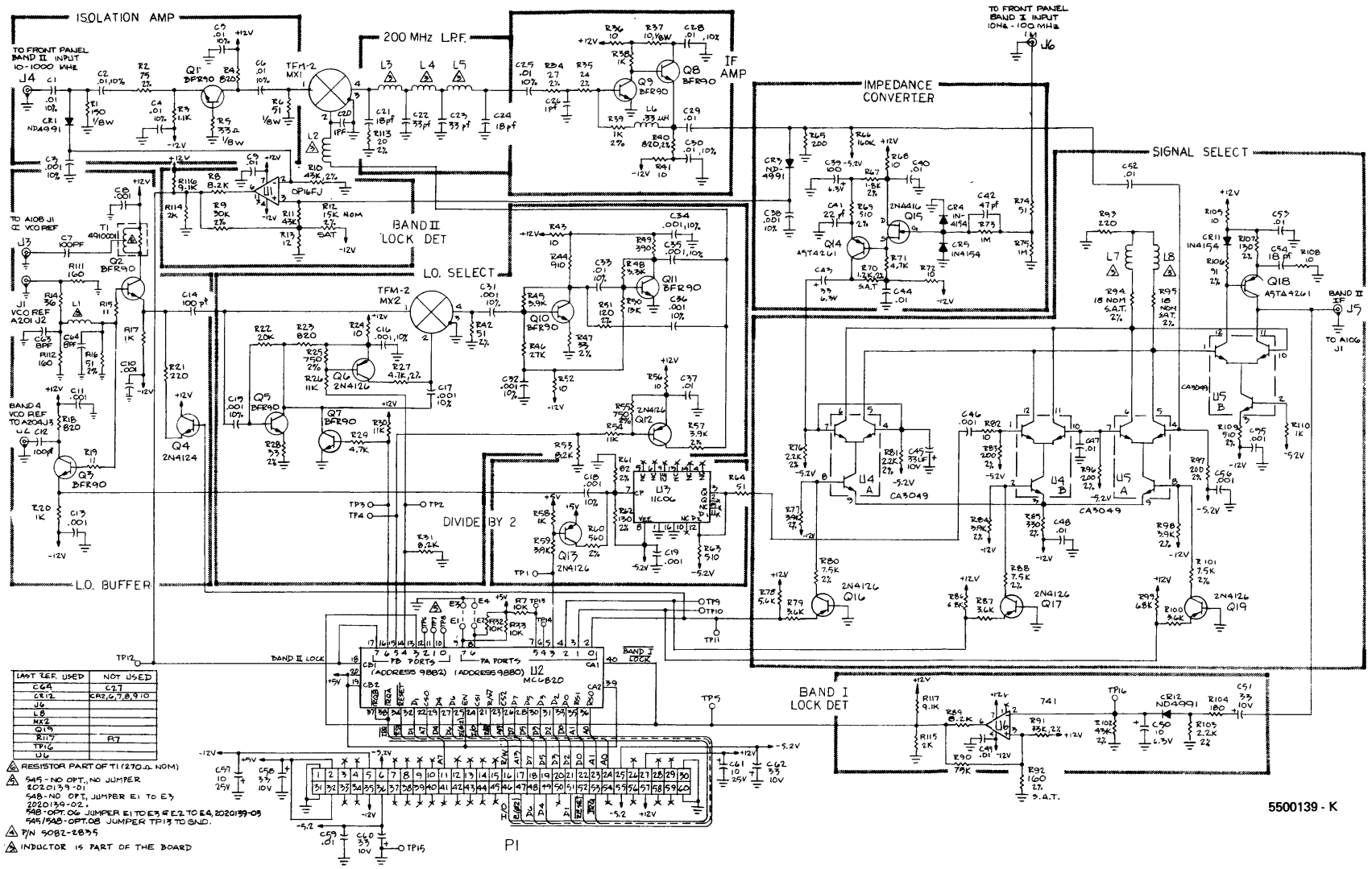


2020139-K

Figure 109 b. Band 2 Converter Component Locator



LAST REF. USED	NOT USED
C64	C67
CR12	CR2,6,7,8,9,10
J6	
L8	
MX2	
Q19	
R117	R7
TP16	
U6	

⚠ RESISTOR PART OF T1 (270-Ω NOM)

⚠ 548 - NO OPT., NO JUMPER 2020139-01
548 - NO OPT., JUMPER E1 TO E3 2020139-02.
548 - OPT. 06 JUMPER E1 TO E3, E2 TO E4, 2020139-03
545/548 - OPT. 08 JUMPER TP13 TO GND.

⚠ P/N 5082-2835

⚠ INDUCTOR IS PART OF THE BOARD

5500139 - K

Figure 109 c. Band 2 Converter Schematic

A110
FRONT PANEL
DISPLAY AND KEYBOARD
(2020140)

The Front Panel Display and Keyboard assembly (A110) is divided into two functional sections.

- Numeric display and annunciators
- Keyboard

NUMERIC DISPLAY AND ANNUNCIATORS

This section of the assembly contains twelve common anode 7-segment numeric display units (DS1-DS12), two green LED's (DS37 and DS38), and a maximum of twenty-four yellow LED's (DS13-DS36).

The twelve 7-segment LED's are mounted side-by-side, with space between each third digit from the right. The corresponding cathode segments of the 7-segment LED's are connected, and the drive signals come from the segment drivers Q3 through Q10. The signals to drive the digits come from the digit drivers located on the Front Panel Logic board (A111).

The twenty-four yellow LED's (DS13-DS36) are divided into three groups of 8 LED's each. The anodes of all LED's in each group are connected. The cathode of each LED in a group are connected to one of the segment drivers (Q3-Q10). With this arrangement each group of annunciator lights can be regarded as similar to one 7-segment LED. The digit drives for the 3 groups of annunciator lights also come from the Front Panel Logic board (A111).

The two green LED's (DS37 and DS38) are driven by Q1 and Q2. When these LED's light they indicate that GATE and CONVERTER SEARCH are in operation.

KEYBOARD

This section of the assembly contains a maximum of twenty-five (single-pole double-throw) switches. The switches are arranged in a 4 row by 6 column matrix, with the extra switch taking the row 4 column 7 position. The columns are connected to +5V through the resistor network (RN1) on the Front Panel Logic board (A111).

The keyboard is continuously scanned. The signals scanning the keyboard are derived from A111. To scan the keyboard the 4 rows are grounded sequentially. When a row is grounded, and a key in that row is pushed, one of the columns will be grounded. This information is sent to the A111 board where key debouncing is performed.

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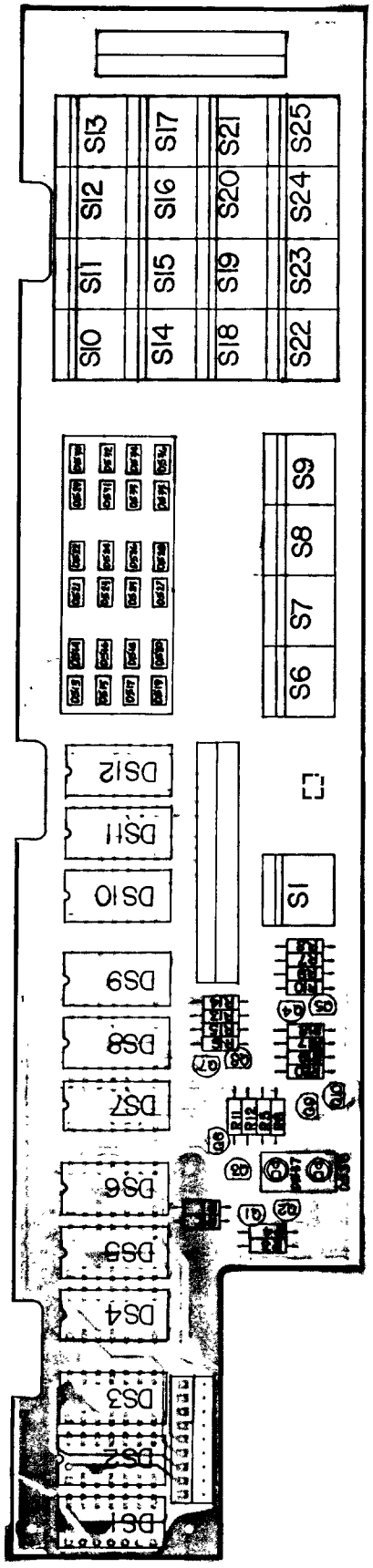
A110 FRONT PANEL DISPLAY AND KEYBOARD

2020140-B

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
Q1 thru Q10	PNP, Amp.	4710019	10	MPS - D55	04713
R1	Comp, 4.7K, 5%, 1/4 W	4010472	2	RC07GF472J	81349
R2	Comp, 130, 5%, 1/4 W	4010131	2	RC07GF131J	81349
R3	R1				
R4	R2				
R5	Comp, 240, 5%, 1/4 W	4010241	8	RC07GF241J	81349
R6	Comp, 18, 5%, 1/4 W	4010180	8	RC07GF180J	81349
R7	R5				
R8	R6				
R9	R5				
R10	R6				
R11	R5				
R12	R6				
R13	R5				
R14	R6				
R15	R5				
R16	R6				
R17	R5				
R18	R6				
R19	R5				
R20	R6				
DS1 thru DS12	LED, Numeric, Red	2800004	12	HP5082 - 7730	28480
DS13 thru DS36	LED, Lamp, Yel	2800020	24	MV57124	50522
DS37	LED, Lamp, Grn	2080018	2	MV5274	50522
DS38	DS37				
S1					
S2 thru S5	Not Used				
S6 thru S25	Switch, Mon, SPDT	4500013	21	REK	
P1	9 pin Recept.	2620065	1	22 - 14 - 209	0000A
P2	17 pin Recept.	2620067	1	22 - 14 - 2171	0000A
P3	13 pin Recept.	2620066	1	22 - 14 - 212	0000A



2020140 - B

Figure 110a. Front Panel Display and Keyboard Component Locator

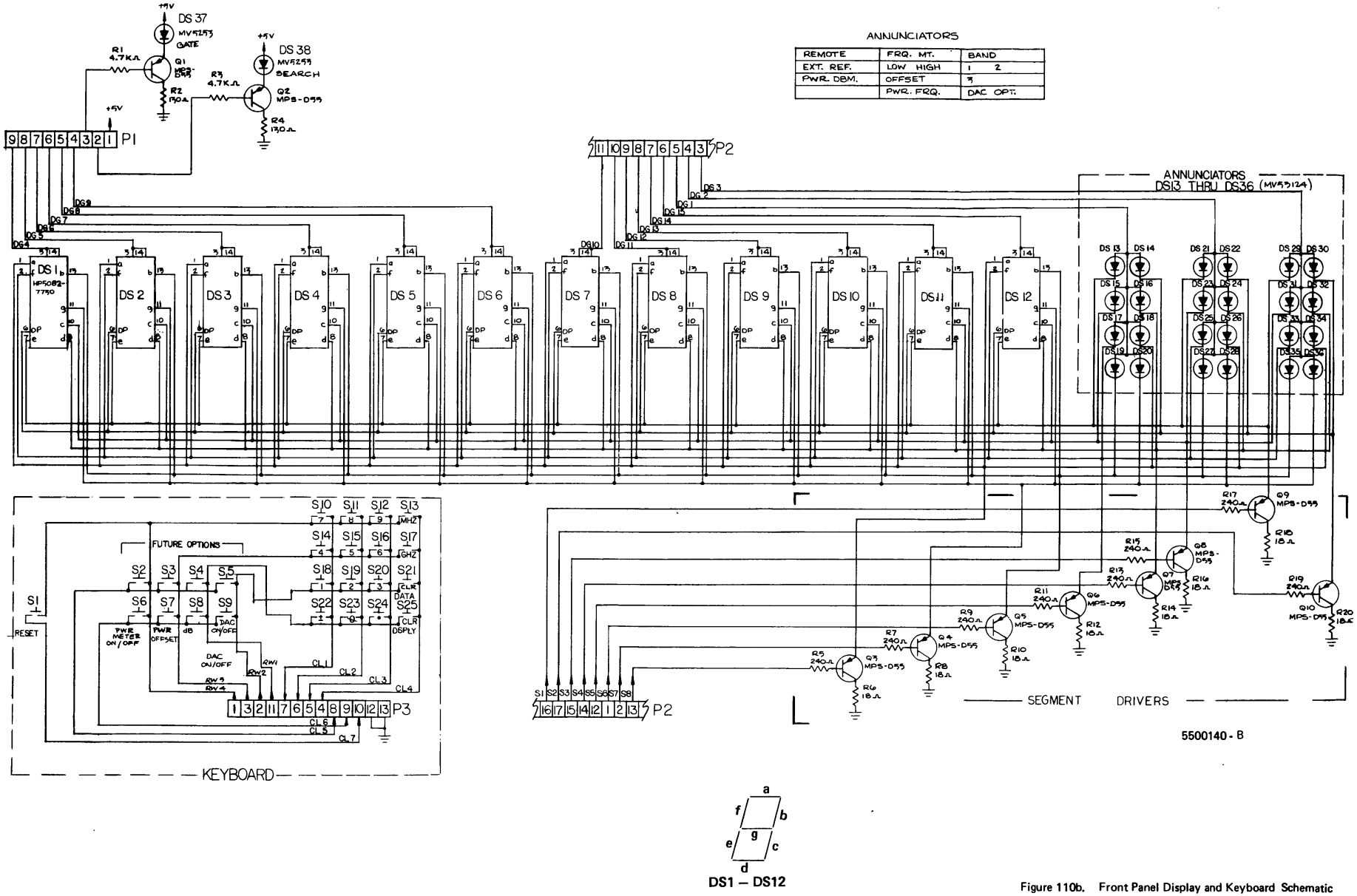


Figure 110b. Front Panel Display and Keyboard Schematic

A111
FRONT PANEL LOGIC
(2020141)

The Front Panel Logic assembly (A111) contains logic circuitry for control of two functions.

- Display Control
- Keyboard Control

The +5V power supply to the front panel assemblies (A110 and A111) is regulated by a voltage regulator that is located behind the A111 board. For heatsinking purposes, this voltage regulator is mounted on the chassis. Please refer to figure 111b. Front Panel Logic block diagram on page 111-3.

DISPLAY CONTROL

The twelve 7-segment LED's and the three groups of annunciator lights on A110 are multiplexed. To turn on a particular segment in a digit, both the digit driver for that digit and the segment driver for that segment must be on.

The display logic is in constant operation in either the self-scan mode or the memory update mode.

SELF-SCAN MODE

This is the normal operating mode. In this mode the display scan clock is clocking the display counter (U6). The state of the display counter determines which digit will be turned on.

The state of the display counter is decoded by 4 to 16 line multiplexer (U2), and the appropriate digit driver is turned on. At this time the display memory (U7 and U8) is read, and the on/off information (stored in the display memory for that specific digit), turns the segment drivers (A110) on or off.

The display intensity is controlled by varying the duty cycle of the multiplexing. This is done by varying the resistance of the potentiometer (R4) which, in turn, varies the length of time the decoder (U2) and the display memories (U7, U8) are disabled between each scan clock cycle.

At the start of each gate operation the GATE light control is triggered, and the GATE LED lights for the length of the GATE.

MEMORY UPDATE MODE

In this mode the multiplexer logic is disabled by setting the display scan/$\overline{\text{update}}$ control line (PA7) to logic 0. The microprocessor controlled clock ($\overline{\text{clock}}$, PA1) is used to clock the display counter (U6).

Before updating the display memory (U7 and U8), the display counter is cleared by setting the clear/load control line (PA5) to logic 1, and clocking the clock input of U6. Update mode timing is illustrated in Figure 111a.

KEYBOARD CONTROL

The keyboard logic operates in either the self-scan mode or the read keyboard mode.

SELF-SCAN MODE

In this mode the keyboard is scanned by grounding the four rows of keys sequentially. This is done by shifting the contents of the shift register (U3).

When no key on the keyboard is pushed, all the inputs to the 8-input NAND gate (U13) are at logic 1 level. If the key being pushed is in a row that is grounded, the column containing that key will also be grounded. Then U13 output goes to logic 1 and stops the keyboard scan clock, and C7 (in the debounce circuit) starts to discharge. When the voltage across C7 reaches approximately +0.7V above ground, the debounce circuit will trigger the interrupt input on the PIA (U11, pin 18) indicating that a key is being pushed.

READ KEYBOARD MODE

In this mode a logic 1 is put on the keyboard read/$\overline{\text{scan}}$ control line (PA0). This enables the data buffer (U9), and selects the microprocessor controlled clock for clocking the shift register (U3). The keyboard is then scanned once, under microprocessor control, to determine which key is being pushed.

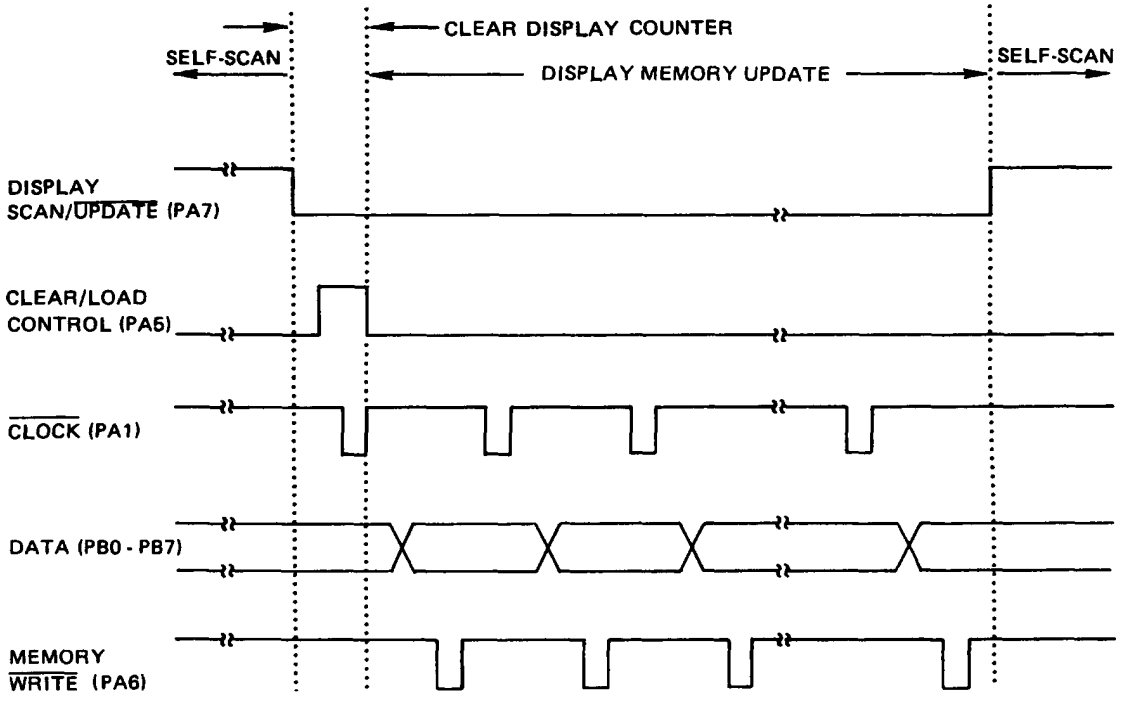


Figure 111a. Memory Update Mode Sequence

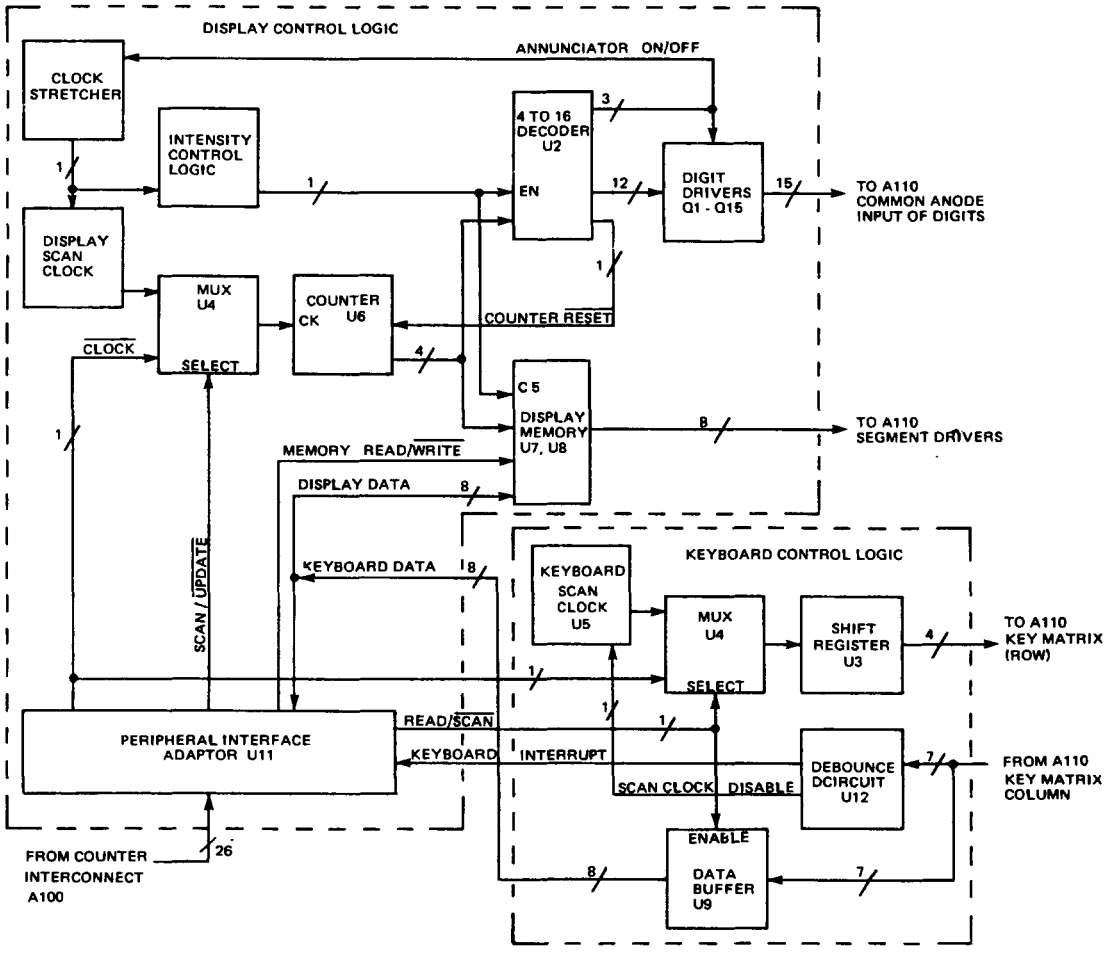


Figure 111b. Front Panel Logic Block Diagram

A111 FRONT PANEL DRIVER

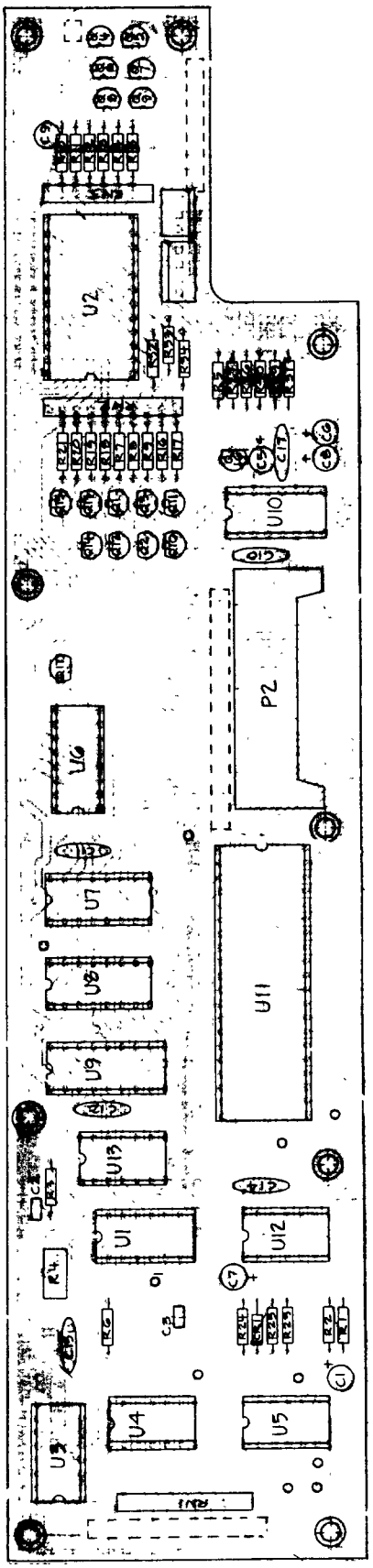
2020141-F

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A111	Front Panel Driver Assy	2020141	1	EIP	
C1	Tant, 0.1μF, 10%, 35V	2300020	1	TAG20 - 0.10/35	14433
C2	Cer, 2200pF, 10%, 100V	2150020	1	6183X7R222KA100	80031
C3	Cer, 1500pF, 10%, 100V	2150019	1	6183X7R152KA100	80031
C4	Not Used				
C5	Tant, 47μF, 20%, 16V	2300025	1	TAG20 - 47/16 - 20	14433
C6	Tant, 2.2μF, 20%, 16V	2300012	1	TAG20 - 2.2/16 - 20	14433
C7	Tant, 22μF, 20%, 16V	2300030	1	TAG20 - 22/16	14433
C8	Tant, 0.33μF, 20%, 35V	2300031	1	TAG20 - .33/35 - 50	14433
C9	Tant, 33μF, 20%, 10V	2300015	1	TAGE20 - 33/10 - 50	14433
C10 thru C15	Cer, .01μF, 20%, 100V	2150003	6	TG - S10	56289
C16	Not Used				
C17	C10				
CR1	General Purpose	2704154	1	1N4154	07263
J1	9 pin male	2620062	1	22-03-2091	0000B
J2	13 pin male	2620063	1	22-03-2131	0000B
J3	17 pin male	2620064	1	22-03-2171	0000B
J4	4 pin FR Lock	2620068	1	640456-4 AMP	
J5	3 pin male	2620121	1	640456-3 AMP	
P2	26 pin, RT Angle	2620131	1	3493-1002	76381
Q1 thru Q15	PNP, Power	4710027	15	MPS-D54	04713
Q16	NPN, General Purpose	4704124	2	2N4124	04713
Q17	Q16				
R1	Comp, 10K, 5%, 1/4 W	4010103	2	RC07GF103J	81349
R2	Comp, 220, 5%, 1/4 W	4010221	1	RC07GF221J	81349
R3	Comp, 75K, 5%, 1/4 W	4010753	1	RC07GF753J	81349
R4	VAR. Cer, 200K	4250022	1	72XR200	73138
R5	Comp, 120K, 5%, 1/4 W	4010124	1	RC07GF124J	81349
R6	Comp, 5.1K, 5%, 1/4 W	4010512	1	RC07GF512J	81349
R7 thru R21	Comp, 1K, 5%, 1/4 W	4010102	15	RC07GF102J	81349
R22	Not Used 4 W				
R23	Comp, 15K, 5%, 1/4 W	4010153	1	RC07GF153J	81349
R24	Comp, 390, 5%, 1/4 W	4010391	1	RC07GF391J	81349
R25	Comp, 200, 5%, 1/4 W	4010201	1	RC07GF201J	81349
R26	Comp, 820, 5%, 1/4 w	4010821	2	RC07GF821J	81349
R27	R1				
R28	Not Used				
R29	Comp, 2.2K, 5%, 1/4 W	4010222	1	RC07GF222J	81349
R30	R26				
R31	Comp, 27K, 5%, 1/4 W	4010273	1	RC07GF273J	81349
R32	Comp, 39K, 5%, 1/4 W	4010393	3	RC07GF393J	81349
R33	R32				
R34	R32				

A111 FRONT PANEL DRIVER

2020141-F

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
RN1	Network, 10K	4170003	2	4310R - 101 - 103	32997
RN2	RN1				
RN3	Network, 10K	4170004	1	4308 - 101 - 103	32997
TP1 thru TP10	Conn pin, .04 D, Gold	2620032	10	460 - 2970 - 02 - 03	71279
U1	TTL, Monostable, MV	3084123	2	DM74LS123N	0000X
U2	4-16 Line Decoder	3074154	1	DM74154N	0000X
U3	4 Bit Shift Register	3084195	1	DM74LS195N	0000X
U4	AND - OR - INVERT Gates	3087451	1	SN74LS51N	01295
U5	Quad, 2 INP NAND Gate	3084132	1	DM74LS132N	0000X
U6	Binary Sync Clear	3084163	1	SN74LS163	01295
U7	Bipolar RAMS	3057489	2	DM74LS189	0000X
U8	U7				
U9	Oct Bus Trans	3084244	1	SN74LS244N	01295
U10	U1				
U11	Periph, Interface Adapter	3086820	1	MC6820	04713
U12	Hex Inverter	3087414	1	SN74LS14N	01295
U13	8INP NAND Gates	3087430	1	DM74LS30N	0000X
U14	Pos. Voltage Regulator (reference only - U14 part of front panel power supply)	3057805	1	MC7805CT	04713



2020141 - F

Figure 111c. Front Panel Logic Component Locator

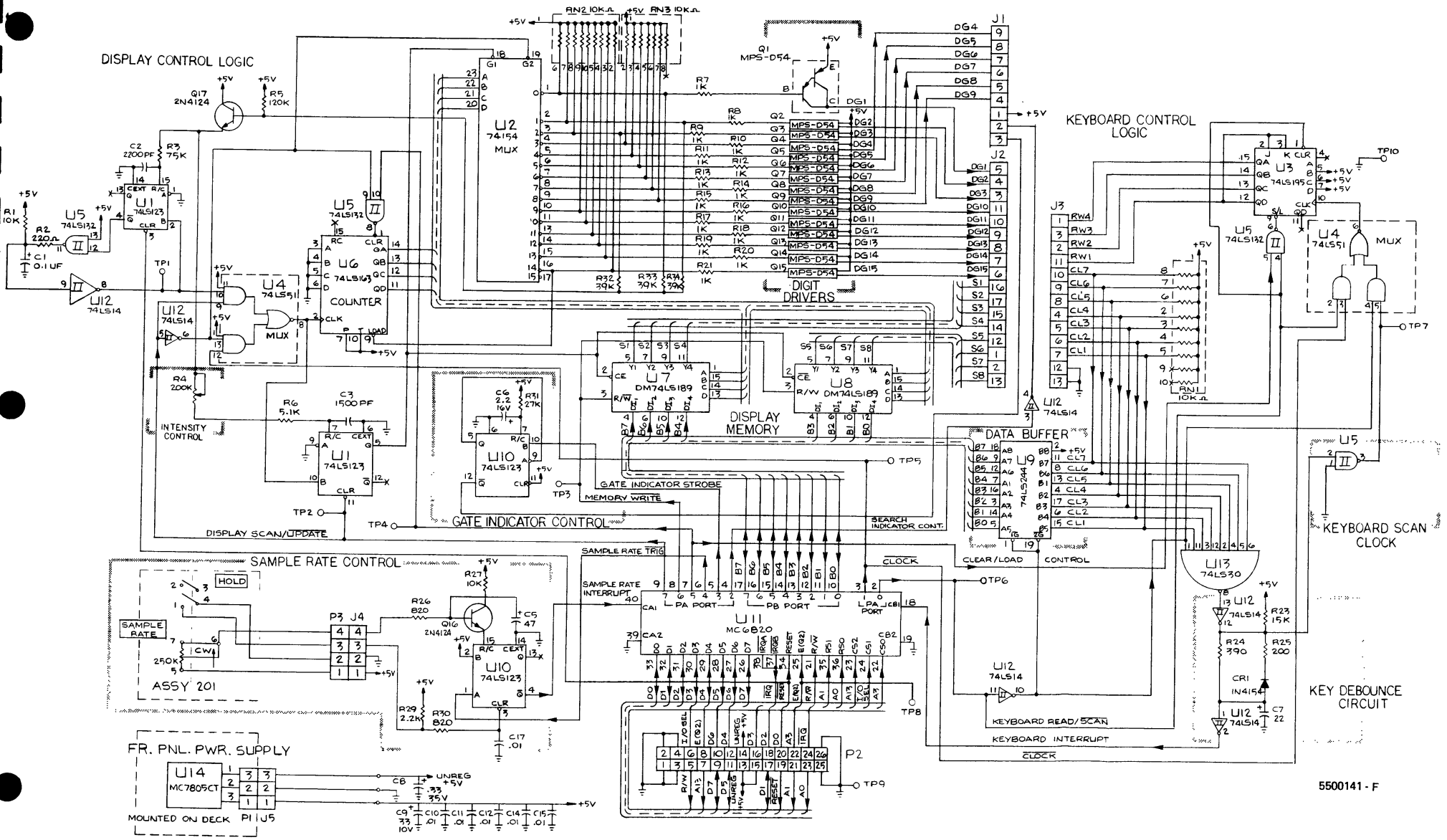


Figure 111d. Front Panel Logic Schematic

A203
BAND 3 MICROWAVE CONVERTER

The A203 Microwave Converter consists of three sub-assemblies.

- A201A Voltage Control Oscillator
- A201B IF Amplifier
- A202 Microwave (yig)

CAUTION

Disassembly of the A202 Microwave assembly, or removal of it from the A201A VCO or A201B IF Amplifier will void the EIP warranty.

The assembly drawing and schematic for both the VCO and IF circuits are included only for reference. The entire A203 assembly must be tested as a complete unit to ensure proper performance of the counter. Repair of the A202 Microwave assembly can only be done at the factory. The VCO and IF Amplifier boards require special test equipment, therefore field repair is not recommended.

The Band 3 Converter is a complete microwave subsystem (see Figure 200a.) which converts an input signal in the 1 to 18 (26.5) GHz range down to an IF of 125MHz. Down conversion is achieved in this heterodyne system by combining the input signal with a harmonic of a precisely known reference signal (F_{VCO}). The mixer then produces a signal (F_{IF}) equal to the difference between the input and reference harmonic. If this difference is close to 125MHz, it is amplified to a level of about 0dBm and then counted. The input signal is then determined from the equation $F_{IN} = NF_{VCO} + F_{IF}$. F_{VCO} is set by the instrument program via a phase locked loop located on the converter control board (A108) and is thus known exactly. Harmonics of the VCO are produced by the comb generator and coupled to the mixer. The frequency ranges of the VCO and IF are such that for any VCO frequency and any input frequency, only one harmonic can produce an IF frequency. The YIG filter located between the RF input and the mixer is used to approximatley determine the input frequency and from this information the desired values of N, F_{VCO} and +/– are determined.

Two other outputs are obtained from the Band 3 Converter. The first is an anlaog signal which is a measure of input RF power. The second is a digital signal $\overline{\text{(IF THRESHOLD)}}$ which indicates that an IF signal exists at a level of –3dBm or greater.

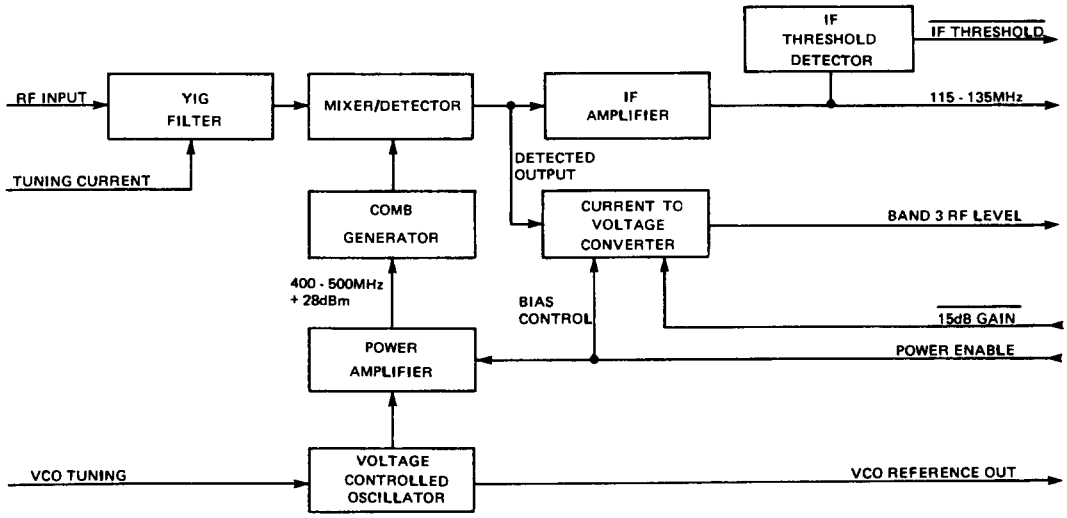


Figure 203-1. Band 3 Microwave Converter Block Diagram

A201A
VOLTAGE CONTROL OSCILLATOR
(2020142)

The VCO Assembly contains three sub-functions as shown in Fig. 201A-1. The VCO consists of a transistor oscillator (Q1), whose frequency is determined by an inductor (L1) and a variable capacitor (CR2). The capacitance of CR2 is determined by the applied tuning voltage at J3. For increased stability and noise reduction, an internal voltage regulator (R3, C4, CR3) is used.

The second function is performed by a single stage common base amplifier that is broadly tuned and loaded with 50 ohms. The output level is approximately + 8 dBm over the range 370 - 500MHz. This output is the VCO reference.

The third function is performed by a three stage power amplifier consisting of a common base amplifier (Q3) and two class C stages, Q4 and Q5. This amplifier provides approximately 20dB of gain and 0.6 watts output over the tuning range 400 to 500MHz. The variable capacitors C17, C25, and C28 are adjusted to optimize output power and flatness. Output power is switched on or off by the Pin switch CR3, CR4 which is controlled by U1. On to off power ration is in excess of 50dB.

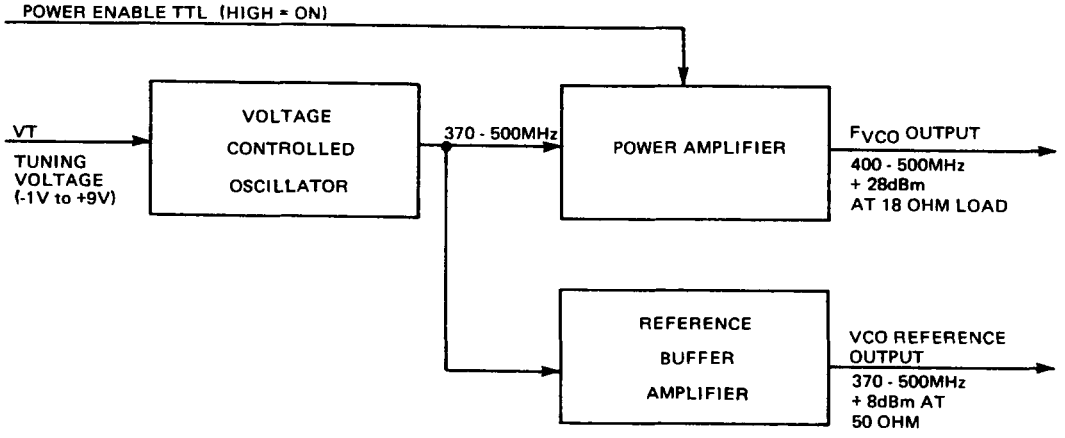


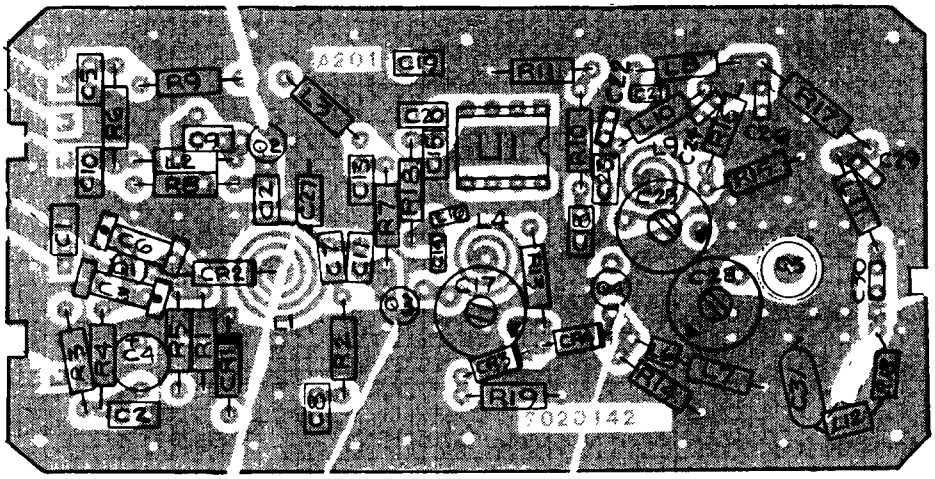
Figure 201A-1. VCO Block Diagram

A201A VOLTAGE CONTROL OSCILLATOR

2020142-F

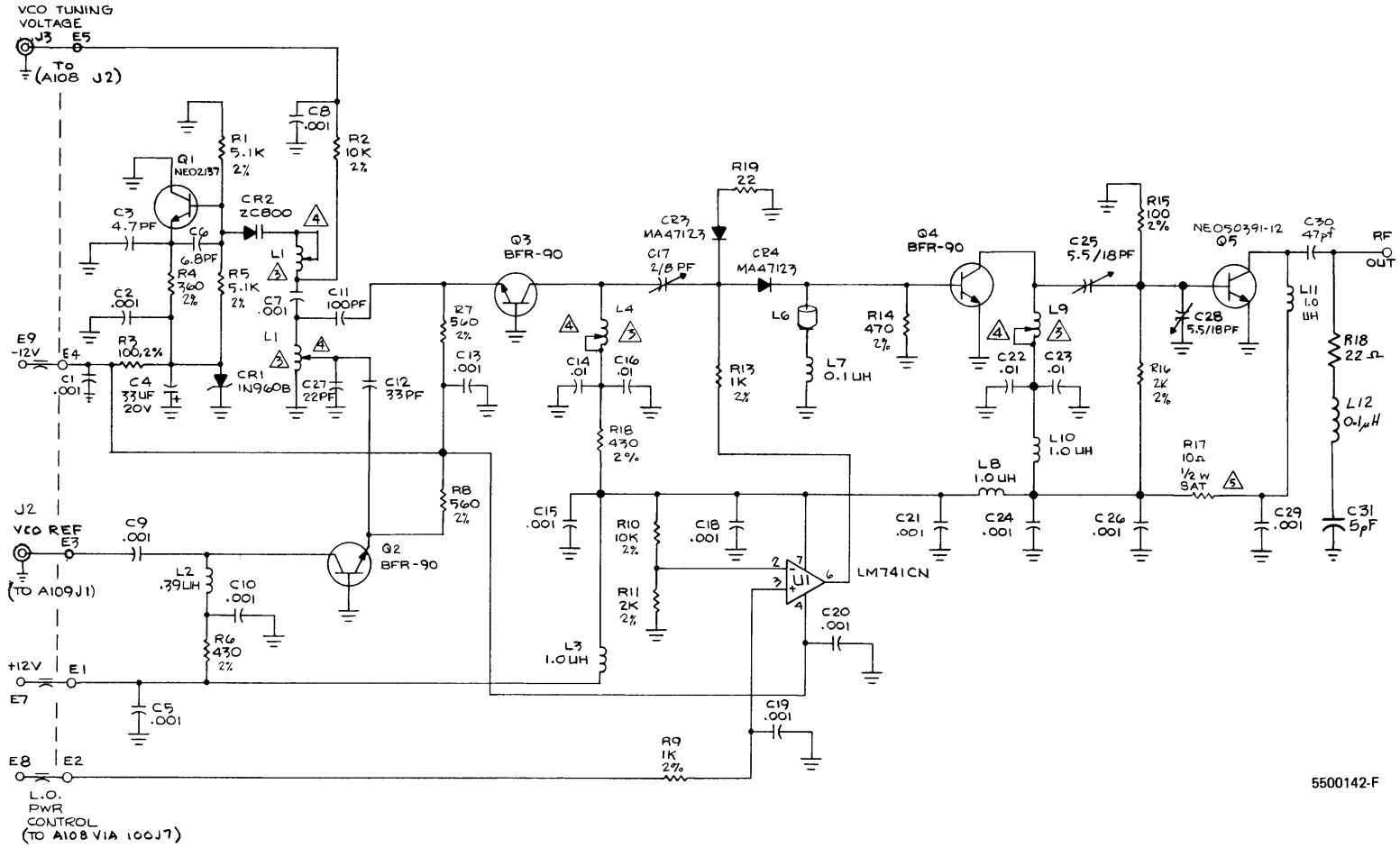
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A201A	Voltage Control Oscillator Assy P/O VCO/IF Module Assy 203	2020142 2010142	1 Ref		
C1	Cer, .001μF, 10%, 100V	2150015	16	UR1515S100X7R102K	80031
C2	C1				
C3	Cer, 4.7pF, 25%, 500V	2160013	1	301000C0H0479C	72982
C4	Tant, 33μF, 20%, 20V	2300023	1	TAG20 - 30/20%	14433
C5	C1				
C6	Cer, 6.8pF, 25%, 500V	2160014	1	301000C0H0689C	72982
C7 thru C10	C1				
C11	Cer, 100pF, 10%, 180V	2150056	1	6183X7R101KA100	80031
C12	Cer, 33pF, 10%, 100V	2150069	1	6183C0G330KA100	80031
C13	C1				
C14	Cer, .01μF, 10%, 100V	2150014	4	6123X7R103KA100	80031
C15	C1				
C16	C14				
C17	Var, 2-8pF, 250V	2350001	1	10S - T - 22 - 2/8	0000B
C18 thru C21	C1				
C22	C14				
C23	C14				
C24	C1				
C25	Var, 5.5 - 18pF, 250V	2350002	2	10S - T - 22 - 02	0000B
C26	C1				
C27	Cer, 22ρF	2150067	1	6183COG220KA100	80031
C28	C25				
C29	C1				
C30	X7R, 47pF	2150039	1	6183C0G470KA100	80031
C31	5pF Nom. S.A.T.	2260999	1	DM10	56289
CR1	Zener, 9.1V	2730960	1	1N960B	04713
CR2	Tun, UHF/VHV HYPERABRPT	2710037	1	ZC800	18518
CR3	Pin	2710024	2	MA47123	
CR4	CR3				
L1	Part of Board		3		
L2	.39μH	3150014	1	1025 - 10	72259
L3	1.0μH	3150003	4	DD - 1.00	72259
L4	L1				
L5					
L6	Ferrite Bead	3500011	1	56 - 590 - 65/33	
L7	0.1μH	3510001	2	DD - 0.10	72259
L8	L3				
L9	L1				
L10 thru L11	L3				
L12	L7				
Q1	Microwave Transistor	4710032	1	NE02137	0000S
Q2	NPN, RF	4710030	3	BFR - 90 - MOT	04713
Q3	Q2				
Q4	Q2				
Q5	UHF/VHF NPN Power	4710029	1	NE050391 - 12	0000S

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R1	Met Ox, 5.1K, 2%, 1/4 W	4130512	2	C4/2%/5.1K	24546
R2	Met Ox, 10K, 2%, 1/4 W	4130103	2	C4/2%/10K	24546
R3	Met Ox, 100, 2%, 1/4 W	4130101	2	C4/2%/100	24546
R4	Met Ox, 360, 2%, 1/4 W	4130361	1	C4/2%/360	24546
R5	R1				
R6	Met Ox, 430, 2%, 1/4 W	4130431	2	C4/2%/430	24546
R7	Met Ox, 560, 2%, 1/4 W	4130561	2	C4/2%/560	24546
R8	R7				
R9	Met Ox, 1K, 2%, 1/4 W	4130102	2	C4/2%/1K	24546
R10	R2				
R11	Met Ox, 2K, 2%, 1/4 W	4130202	2	C4/2%/2K	24546
R12	Comp, 22 ohm, 5%, 1/8W	4000220	1	RC05GF220J	81349
R13	R9				
R14	Met Ox, 470, 2%, 1/4 W	4130471	1	C4/2%/470	24546
R15	R3				
R16	R11				
R17	Comp, 10 ohm, 5%, 1/2 W (SAT)	4020999	1	RC07GFXXX	81349
R18	R6				
R19	Carbon, 22, 5%,	4010220	1		
U1	Lin. Op Amplifier	3040741	1	LM741CN	0000X



2020142 - F

Figure 201A-2. Voltage Controlled Oscillator Component Locator



△5 R17, 10Ω NOMINAL, SAT RANGE 1Ω TO 20Ω. REFER TO TEST PROCEDURE FOR SELECTION CRITERIA (5540142).

△4 SELECT AT TEST ADJUSTMENT

△3 PART OF P.C. BOARD.

Figure 201A-3. Voltage Controlled Oscillator Schematic

A201B
IF AMPLIFIER
(2020143)

The IF Amplifier performs three major functions.

- Amplifies the down-converted intermediate IF frequency to ± 0dBm.
- Provides a digital threshold output when the IF power exceeds -3dBm.
- Provides an analog signal that is proportional to the [illegible] at the Band 3 input. A gain scaling control alters the output by 15dB (=X30).

The Microwave assembly mixer output is the input to the IF board. The IF goes through a high pass filter to three similar amplifier stages. Stage 1 consists of transistors Q1 and Q2 operating under closed loop feedback via R4. Resonant peaking of the output at 125MHz using L4 and C8 gives a power gain of 23dB. Successive stages are similar except that stagger tuning is used for optimum response shape. Inductors L4, L5, and L7 are printed on the circuit board and are adjusted by means of shorting bars placed across portions of the spiral. The IF output signal is sampled by a detector CR3. It's level is compared to a voltage corresponding to –3dBm. When this level is exceeded, the IF threshold output goes low.

The low frequency signal from the mixer is the current caused by rectification of the input power. This is converted to a voltage in U2. To provide a larger dynamic range, a gain change is made by switching the Field Effect Transistor (FET) Q7, thus lowering the feedback resistor. Assemblies used in –02 converters (26.5 GHz) also include transistors Q8 & Q9 to translate a TTL input to ± 12V necessary to drive FET Q10. This circuit sets the mixer bias current to 0 when the VCO power amplifier is enabled.

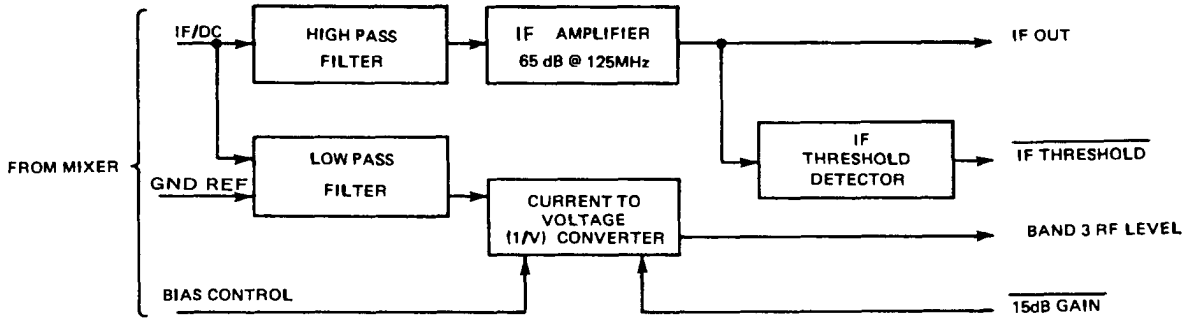


Figure 201B-1. IF Amplifier Functional Diagram

A201B IF AMPLIFIER

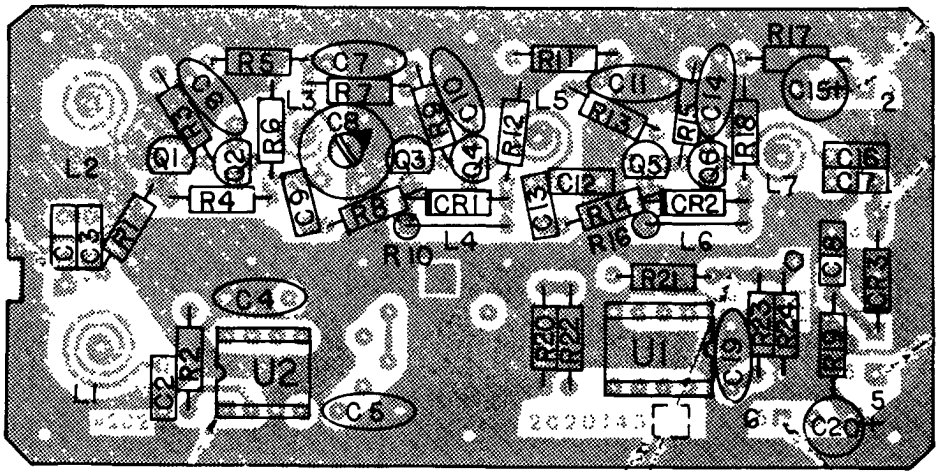
2020143-K

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A201B	IF Amplifier Assy	2020143	1		
	P/O VCO/IF Mod Assy	2010142	Ref		
C1	Mica, 8pF, 13%, 500V	2260011	1	CD080C03	56289
C2	Mica, 100pF, 5%, 500V	2260034	5	FD101J03	72136
C3	Mica, 12pF, 5%, 500V	2260013	2	CD120J03	56289
C4	Not Used				
C5	Not Used				
C6	Cer, .01μF, 20%, 100V	2150003	6	TG - S10	56289
C7	C6				
C8	Mica, 33pF, 5%, 500V	2260021	1	ED330J03	56289
C9	C2				
C10	C6				
C11	C6				
C12	Mica, S.A.T. (47pF, 5%, NOM)	2269999	1	DM - 10	72136
C13	C2				
C14	C6				
C15	Tant, 10μF, 20%, 25V	2300029	2	TAG20 - 10/25(M)	14433
C16	Mica, S.A.T. (39pF, 5%, NOM)	2269999	1	DM - 10	72136
C17	C2				
C18	C3				
C19	C6				
C20	C15				
C21	Not Used				
C22	C2				
C23	Cer, .001μF, 10%, 100V	2150015	1	UR1515S100X7R102K	80031
CR1	Hot Carrier	2710004	2	FH1100	07263
CR2	CR1				
CR3	Zero Bias Shottky	2710038	1	ND4991	21843
L1	Inductor, 0.1μH	3510001	2	DD - 0.10	72259
L2	Inductor, 0.47μH	3510006	1	DD - 0.47	72259
L3	L1				
L4	Part of Board				
L5	Part of Board				
L6	Not Used				
L7	Part of Board				
L8	Inductor, 1μH	3510003	2	DD - 1.00	72259
L9	L8				
Q1 thru Q6	NPN, RF	4710026	6	NE73432B	0000S
Q7	D - MOS FET Switch	4710031	1	SD215	18324
R1	Met Ox, 51, 2%, 1/4 W	4130510	1	C4/2%/51	24546
R2	Prec, 1.82K, 1%, 1/10 W	4051821	1	RN55C1821F	81349
R3	Comp, 1K, 5%, 1/4 W	4010102	2	RC07GF102J	81349
R4	Met Ox, 510, 2%, 1/4 W	4130511	1	C4/2%/510	24546
R5	Comp, 10, 5%, 1/4 W	4010100	5	RC07GF100J	81349
R6	Met Ox, 82, 2%, 1/4 W	4130820	2	C4/2%/82	24546
R7	R5				
R8	Met Ox, 47, 2%, 1/4 W	4130470	2	C4/2%/47	24546
R9	Comp, 2K, 5%, 1/4 W	4010202	1	RC07GH202J	81349
R10	Met Ox, 470, 2%, 1/4 W	4130471	2	C4/2%/470	24546
R11	R5				
R12	Met Ox, 75, 2%, 1/4 W	4130750	1	C4/2%/75	24546

A201B IF AMPLIFIER, continued

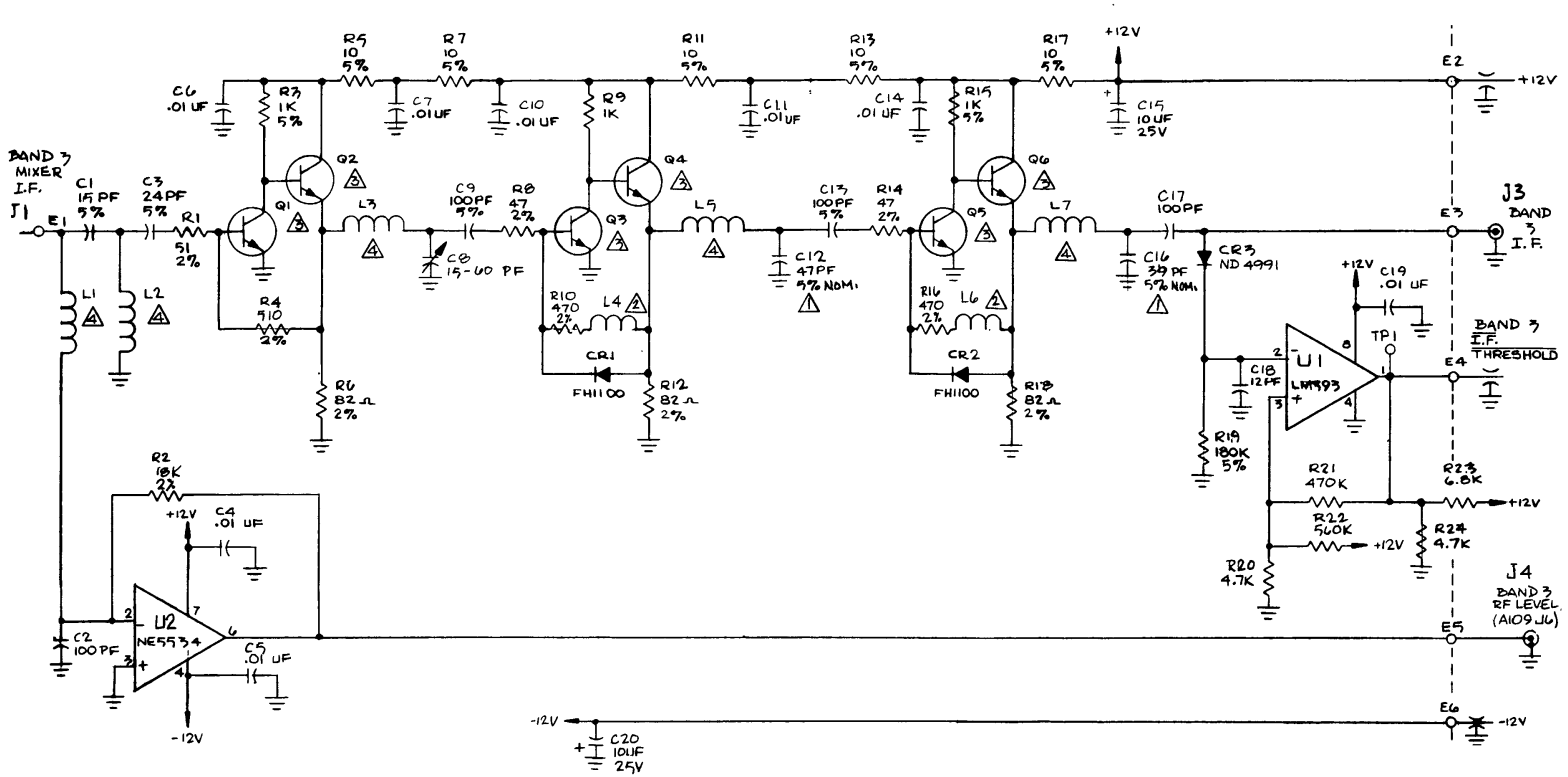
2020143-K

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R13	R5				
R14	R8				
R15	R3				
R16	R10				
R17	R5				
R18	R6				
R19	Comp, 180K, 5%, 1/4 W	4010184	1	RC07GF184J	81349
R20	Comp, 4.7K, 5%, 1/4 W	4010472	2	RC07GF472J	81349
R21	Comp, 470K, 5%, 1/4 W	4010474	1	RC07GF474J	81349
R22	Comp, 560K, 5%, 1/4 W	4010564	1	RC07GF564J	81349
R23	Comp, 6.8K, 5%, 1/4 W	4010682	1	RC07GF682	81349
R24	R20				
R25	Not Used				
R26	Prec, 56.6K, 1%, 1/10 W	4055762	1	RN55C5762F	81349
R27	Met Ox, 100, 2%, 1/4 W	4130101	1	C4/2%/100	24546
R28	Comp, 100K, 5%, 1/4 W	4010104	1	RC07GF104J	81349
R29	Comp, 15K, 5%, 1/4 W	4010153	1	RC07GF153J	81349
U1	Dual Comp, Low Power	3050393	1	LM393	0000X
U2	Lin Op Amp	3041458	1	MC1458P1	0000X



2020143 - A

Figure 201B-2. IF Amplifier Component Locator



⚠4 L1, L2, L3, L5 & L7 ARE PART OF P.C.B.

⚠5 Q1-Q6 ARE NE73432B.

⚠2 PART OF RESISTOR LEAD. (SEE ASSY DWG. 2020143)

⚠1 FACTORY SELECT NOM. VALUE SHOWN

5500143 - A

LAST USED REF. DES.	NOT USED
C20	
CR3	
E6	
L7	
Q6	
R24	
U2	

Figure 201B-3. IF Amplifier Schematic

Section 10
Options

Section 10 provides descriptions, specifications (where applicable), schematic diagrams and component locators for the options available for use with the Model 545 or 548 counter.

OPTION

01 D TO A CONVERTER

DAC will convert any three consecutively displayed digits into an analog voltage output on rear panel.

02 POWER MEASUREMENT

1 to 18/26.5 GHz will measure sine wave amplitude to 0.1 dBm resolution and display simultaneously with frequency.
Power offset to 0.1 dB resolution, selectable from front panel.
Option will not degrade the basic performance of the counter.

03 TIME BASE OSCILLATOR $< 5 \times 10^{-9}$ (2010143-03).

04 TIME BASE OSCILLATOR $< 1 \times 10^{-9}$ (2010143-04).

05 TIME BASE OSCILLATOR $< 5 \times 10^{-10}$ (2010143-05).

06 EXTENDED FREQUENCY CAPABILITY - 548
Use in conjunction with: Mod. 591 Remote Sensor

07 REMOTE PROGRAMMING/BCD output

08 GENERAL PURPOSE INTERFACE BUS (GPIB)

09 REAR INPUT

10 CHASSIS SLIDES

OPTION 01
DIGITAL TO ANALOG CONVERTER

Option 01 will convert three consecutive digits to an analog voltage, available on the rear panel. The output will be reflect the display, substituting zeros for any non-numeric characters that appear. The output will be updated after every display update.

SPECIFICATIONS

Output Voltage	0.000 volts to 0.999 volts
Accuracy (25° C)	± 0.5 % ±1 mV
Temp. Stability (0-50° C)	± 0.01 % / °C
Resolution	1 mV
Load Impedance	1 K ohm minimum
Connector	BNC female (on rear panel)
Protection	± 10 V AC or DC applied to output connector will not cause damage. No damage will occur by any load.

OPERATION

On power up the DAC is in off state.

LOCAL OPERATION WITH KEYBOARD

A three key sequence selects the location of the three digits desired, by entering the most significant digit wanted. Digits are numbered 01 through 12.

PRESS : DAC [ ] [X] [X] XX can vary from 01 to 12.

EXAMPLES :

DAC [ ] [0] [1] 1 Hz digit selected

DAC [ ] [0] [2] 10 Hz, 1 Hz digits selected

DAC [ ] [0] [3] 100 Hz, 10 Hz, 1 Hz digits

DAC [ ] [0] [4] 1 kHz, 100 Hz, 10 Hz digits

•
•
•

DAC [ ] [1] [2] 100 GHz, 10 GHz, 1 GHz digits

After pressing DAC [ ] , the display will show the present DAC status, like DAC OFF or DAC XX, and three decimal points will show the locations of the currently selected digits (if DAC is on).

After pressing the first [X], the display will show the temporary entry, like DAC X , but the three decimal points will still show the previous DAC status.

After pressing the second [X], the display will show the new entry, like DAC X X , and the three decimal points will move to the new places. The DAC output will start to be updated accordingly. Release of the button pressed will return the display back to normal frequency display.

Any wrong key pressed will result in displaying ERROR 10. The operator must restart the key sequence to enter the correct data.

To clear display from DAC data, ERROR display, or ignoring half-sequence entered, press [CLEAR DISPLAY]. Display will return to normal and DAC status will not be changed.

To shut off DAC press [DAC] [DATA CLEAR] or [DAC] [0] [0]

REMOTE OPERATION

For remote operation through GPIB refer to the GPIB (Option 08) section of this manual.

For remote operation through BCD/RMT refer to the BCD/RMT (Option 07) section of this manual.

THEORY OF OPERATION

A simplified block diagram of the DAC board is shown in figure 01-1.

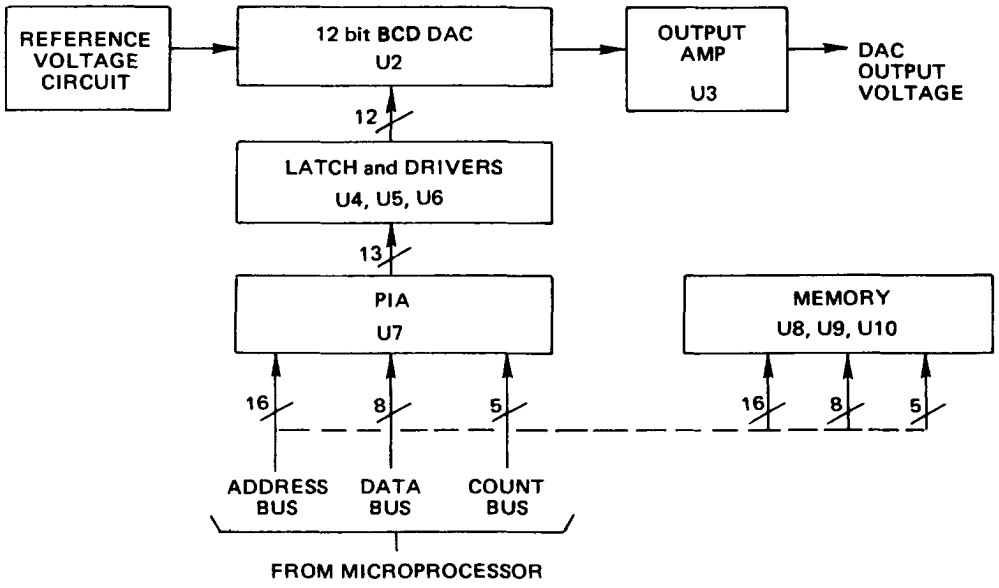


Figure 01-1. DAC Board, Simplified

HARDWARE

MEMORY BLOCK

All the DAC program is contained in the U9 PROM on the DAC board. Refer to the MEMORY block in figure 01-1. U8 is used to drive the data bus back to the counter. U10 is an address decoder that enables U9 on addresses between hexidecimal 4800 and 4BFF.

PIA AND LATCH DRIVER BLOCKS

The three selected digits are manipulated by the program and sent to the PIA. First the two LSD's are sent to port A, then the third digit (MSD) plus a positive-going pluse (on pin 14 of U7) that triggers the latch U6 so that the complete 12 bit word appears to the DAC inputs (U2). U4 and U5 are level translators from T^2L to CMOS for the DAC.

ANALOG BLOCKS

The DAC is referenced to a 1 volt reference voltage that is generated by CR1 zener and U1 Operational Amplifier. Gain adjustment is provided to calibrate the 1 volt. The DAC U2 converts the 12 bit digital inputs to an analog voltage (0.000 V up to 0.999 V). The output amplifier U3 provides the necessary I/V conversion, output isolation and protection. Zero offset adjustment is provided for calibration purposes, also.

SOFTWARE

The DAC software is described in figures 01-2 and 01-3.

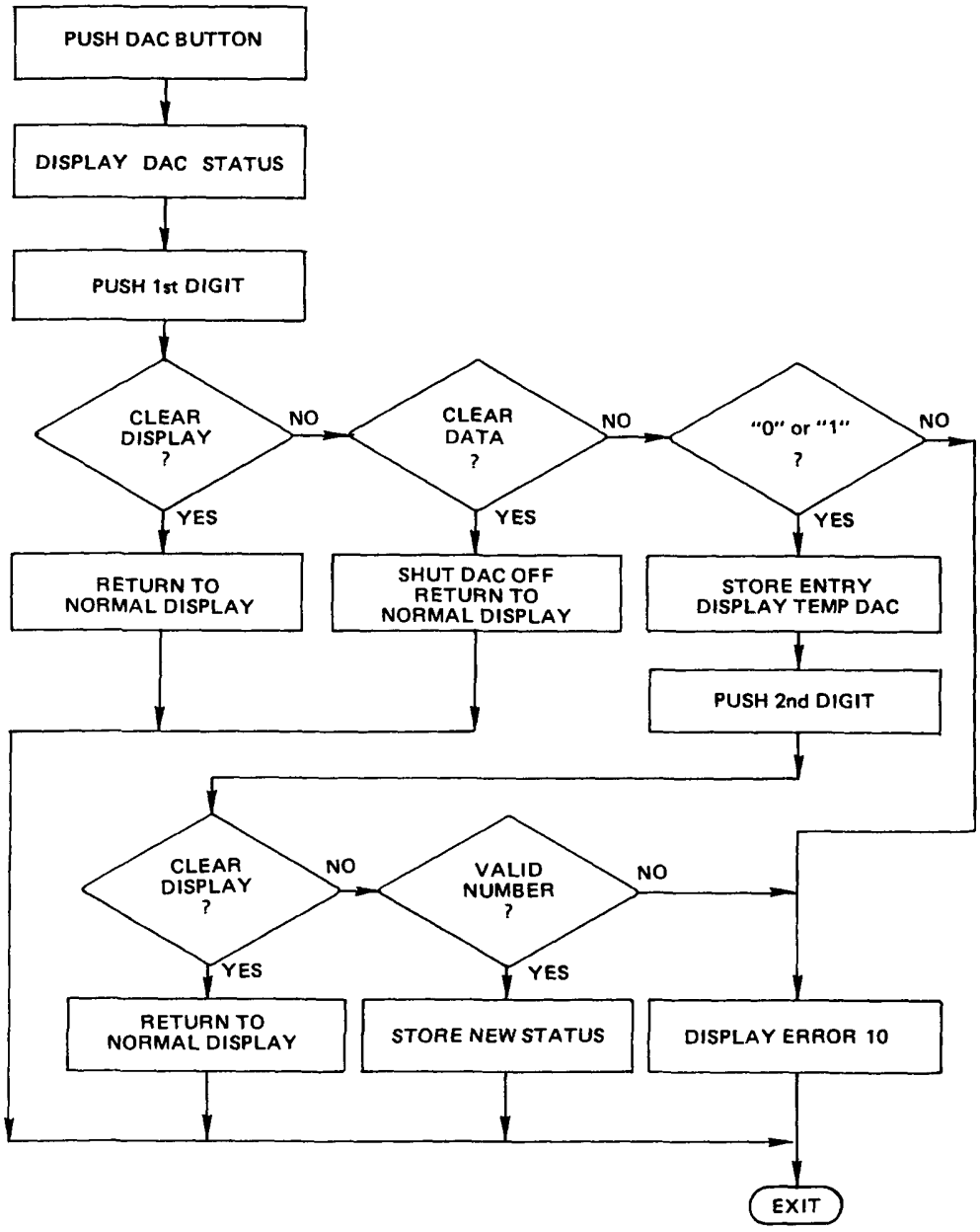


Figure 01-2. Keyboard Control

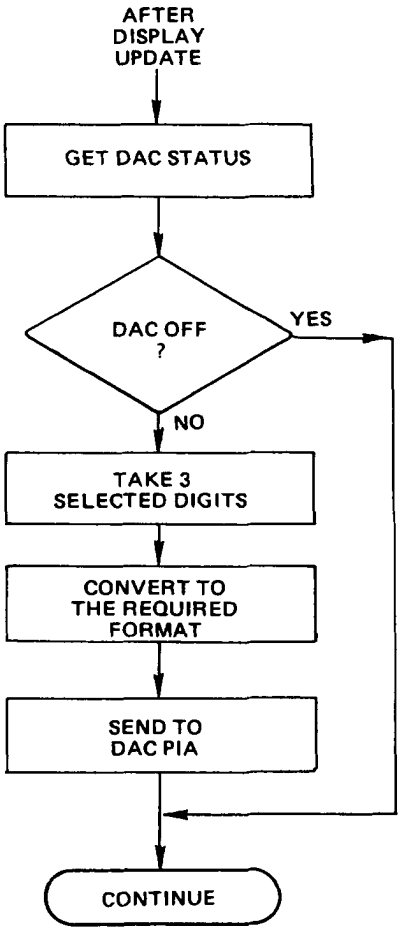


Figure 01-3. DAC Board Update

CALIBRATION

The following instruments or their equivalents are required to perform calibration of the DAC board. Calibration is required every six months or after the board has been repaired.

BRAND	MODEL	TYPE	SPECIFICATIONS
Fluke	8050A	DVM	4 ½ digit resolution

ZERO OFFSET CALIBRATION

1. Turn on the counter with no input, so that the display shows all zeros.
2. PUSH DAC [ ] [0] [3]
3. Connect digital volt meter to the rear DAC output.
4. Adjust R6 to reach 0.000 volts on the DVM display.

FULL SCALE CALIBRATION

1. Short TP3 to TP4.
2. Adjust R4 to reach 1.000 volts on the DVM display.
3. Remove the short.

The calibration for the DAC board is complete.

PERFORMANCE TESTS

Refer to the instruments table in Calibration for the required test equipment.

Connect the DVM to the DAC output (rear panel). Connect rear 10 MHz output to Band 1 input.

ENTER : BAND [ ] [1] RESOL [ ] [2] Display shows 10.000 0 MHz .

ACCURACY TEST

ENTER : DAC [ ] [0] [6] DVM should read 0±1mV.

ENTER : FREQ OFFSET [ ] [•] [9] [9] [9] MHz [ ] DVM should read 0.999±0.006 V.

Repeat the second test in accuracy for entries between .888 and .111. DVM should read the entry ± 1 mV ± 0.5 % of entry.

TROUBLESHOOTING

1. If zero offset calibration cannot be achieved check that all digital inputs to U2 (pins 3 to 15) are at "low" levels (< + 0.5 V). If they are , try to replace U2 or U3.

2. If full scale calibration cannot be achieved check that there is 6.2 volts at TP1. If voltage is wrong, replace CR1 or R1 after verifying the + 12 V supply. If the voltage at TP1 is correct check TP2. The voltage at TP2 should read 1.000 volts. If wrong the failure is in U1 or the resistors R2, R3 or R4. If still wrong replace U2.

3. The digital lines in the DAC board can be checked in three ways.

   - A static test by connecting the rear time base 10 MHz output to Band 1 input.

     ENTER : [BAND] [1] [RESOL] [2] Display shows 10.000 0 MHz

     ENTER : [DAC] [0] [6]

     Now entering [FREQ OFFSET] [•] [X] [X] [X] [MHz] will cause a display of 10.XXX0 MHz.

     The XXX are selected to the DAC board, so the three BCD's should appear on U7, pins 2 to 13 (pin 2 is the LSB). On pin 14 there should be positive pulses. Checking two combinations like 777 and 888 can locate a fault in the digital path between U7 outputs and U2 inputs.

   - A dynamic test that is provided with the DAC option.

     ENTER : [TEST] [1] [1]

     A continuous count ramp from 000 to 999 is sent to the DAC board, regardless of DAC status or display.

     Connect the DAC rear output to an oscilloscope. A ramp should be observed going from 0 to .999 volts. The ramp is built with 1 mV amplitude steps. Any failure in one or more digital lines in the board will cause either breaking in the ramp or a multiple amplitude steps (2mV, 4 mV, ect.). Careful analysis will show the bad line or lines.

   - By Signature analysis while operating in the dynamic test just described, and checking the following signatures.

DAC OPTION SIGNATURES

	START	STOP	CLOCK
CONNECTIONS	A106 TP5	A106 TP5	A105 TP2
BUTTONS	OUT ↑	IN ↓	IN ↓

LINE		SIGNATURE
+5 V		1915
U7 pin -	2	0F91
	3	7F31
	4	4CA3
	5	3241
	6	U738
	7	5UPU
	8	0659
	9	5HHF
	10	7U60
	11	4F30
	12	9115
	13	17HP
	14	30UC
U6 pin -	2	2597
	5	7P0U
	6	U8A9
	9	P1C0
	12	7808
	15	7C4C
	16	46F0
	19	79HH
U5 pin -	2	2597
	4	7P0U
	6	U8A9
	8	P1C0
	10	7808
	12	7C4C

LINE		SIGNATURE
U4 pin -	2	46F0
	4	79HH
	6	7U60
	8	4F30
	10	9115
	12	17HP
U10 pin -	9	1757
U9 pin -	9	67A1
	10	1H57
	11	78UF
	13	2678
	14	15HH
	15	9578
	16	1U65
	17	A799
U8 pin -	18	C570
	16	8UC8
	14	9A4C
	12	074F
	3	82FF
	5	F34U
	9	C1F5

OPTION 01 – DIGITAL TO ANALOG CONVERTER

2020145 - A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A103	Digital to Analog Converter Assy	2020145-01	Ref.	EIP	
C1	Cer, .01 μ F, 20%, 100V	2150003	6	TG-S10	56289
C2	C1				
C3	Mica, 10pF, 5%, 500V	2260012	1	DM15CD100J03	56289
C4	C1				
C5	C1				
C6	Tant, 33 μ F, 20%, 10V	2300015	3	TAG20-33/10-50	14433
C7	C1				
C8	C1				
C9	C6				
C10	Tant, 10 μF, 20%, 25V	2300029	2	TAG20-10/25-20	14433
C11	C10				
C12	C6				
CR1	Zener, 6.2V	2700827	1	IN827	
CR2	Shottky, Barrier	2710004	1	FH1100	07263
R1	Comp, 750, 5%, ¼ W	4010751	1	RC07GF751J	81349
R2	Prec, 39.2K, 1%, ¼ W	4053922	1	RN55C3992F	81349
R3	Prec, 6.19K, 1%, ¼ W	4056191	1	RN55C6191F	81349
R4	Variable, 500 ohm	4280009	1	89PR500	
R5	Comp, 10K, 5%, ¼ W	4010103	1	RC07GF103J	81349
R6	Variable, 10K ohm	4280006	1	89PR10K	
R7	Comp, 1K, 5%, ¼ W	4010102	1	RC07GF102J	81349
RN1	Network of 7,10K	4170004	2	4308R-101-103	32997
RN2	RN1				
U1	Op Amplifier	3040318	1	LM318N	0000X
U2	DAC	3050752	1	AD7525KN	0000X
U3	Prec, Op Amplifier, JFET	3041016	1	OP16FP	06665
U4	Hex Buffer	3007404	2	DM7407N	0000X
U5	U4				
U6	8 Bit Latch	3034373	1	MM74C373N	
U7	PIA	3086820	1	MC6821	04731
U8	Oct. Driver	3084244	1	SN74LS244N	01295
U9	Program PROM 9	6400001-09	1	TM2708	01295
U10	6 Bit Comparitor	3078131	1	DM8131	0000X

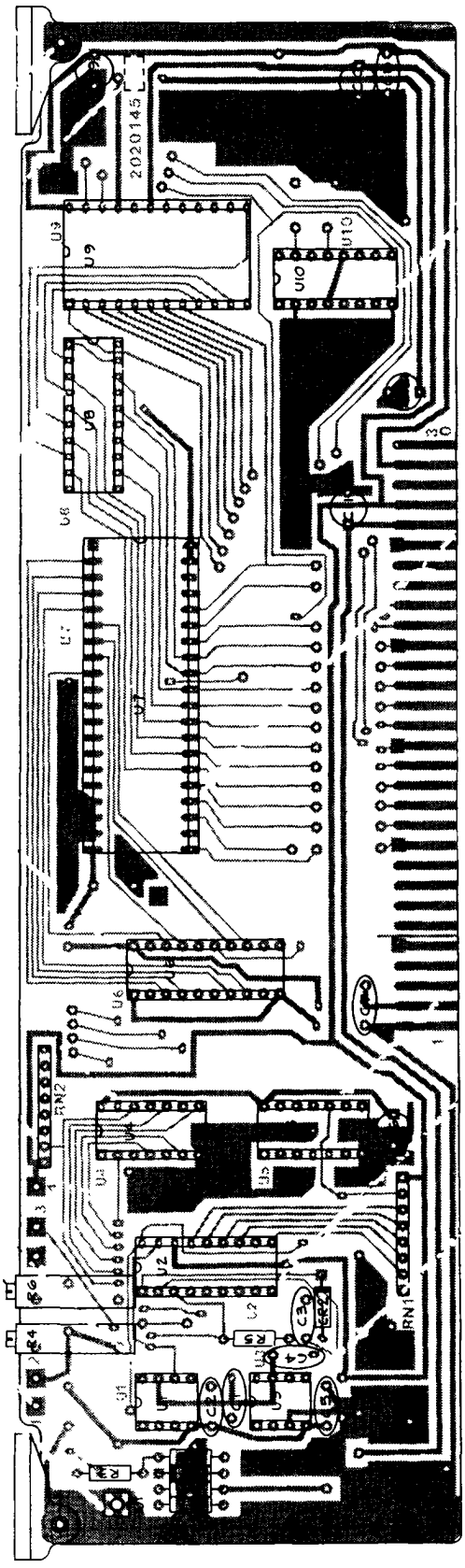
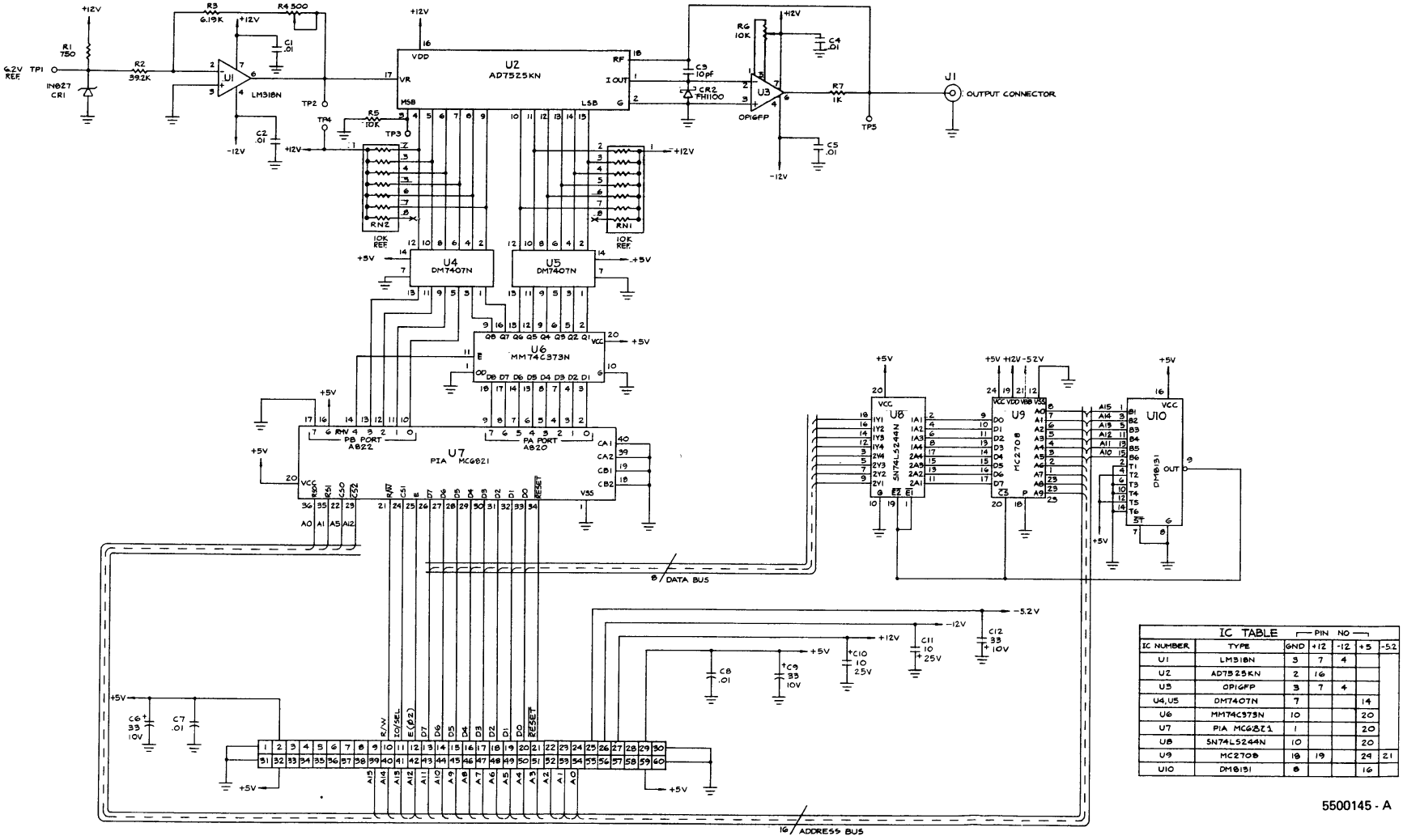


Figure 01-4. DAC Component Locator



IC TABLE		PIN NO				
IC NUMBER	TYPE	GND	+12	-12	+5	-5.2
U1	LM318N	3	7	4		
U2	AD7525KN	2	16			
U3	OP16FP	3	7	4		
U4, U5	DM7407N	7			14	
U6	MM74C373N	10			20	
U7	PIA MC6821	1			20	
U8	SN74LS244N	10			20	
U9	MC2708	18	19		24	21
U10	DM8131	8			16	

5500145 - A

Figure 01-5. DAC Schematic

OPTION 02
POWER MEASUREMENT

Option 02 measures the power of signals applied to Band 3. The power is displayed (to 0.1 dB resolution) simultaneously with frequency (to 100 kHz max. resolution). For A.M. and F.M. averaging purposes, gate time is controllable in the power meter mode, from the resolution switches. Power gate time mirrors frequency gate time. For example, in resolution 0 the frequency gate time is 1 second, and the power gate time is 1 second. In resolution 1 the frequency gate time is 100 msec., and the power gate time is 100 msec. Option 02 allows power offsets from -99.9 dB to 99.9 dB, with a 0.1 dB resolution and will not degrade the basic performance of the counter.

SPECIFICATIONS

ACCURACY	± 1.2 dB Typical 0-50° C ± 0.5 dB Typical 25° C
TIME ADDED	1 GATE TIME + 50 msec.
RESOLUTION	0.1 dB POWER, Selectable 100 kHz - 1 GHz Frequency
RANGE	ENTIRE OPERATING RANGE OF BAND 3

OPERATION

To turn the power meter on press: **POWER METER on/off** ☐

If the counter is displaying only frequency it will begin displaying frequency and power. If the counter is displaying frequency and power it will begin displaying frequency only.

Turn the power meter on. Observe the display. Frequency is displayed on the left, and power is displayed on the right. The POWER dBm annunciator lights to indicate power meter operation. If the signal is too small to measure the power, the display will show EE.E in the power meter digits. (Since 0 dBm is a valid power, 00.0 can not be used as a no power indicator.)

Power meter offsets are entered and displayed in the same manner as other data. Refer to the Display and Data Entry Sequence in Section 3.

To turn the power meter off press: **POWER METER on/off** ☐

THEORY OF OPERATION

The power meter uses the schottky diode in the microwave converter as its power sensor. The output of the diode detector is connected to a programmable gain attenuator, which consists of two switchable gain stages (one is in the IF Amplifier A201B and one is on the Gate Generator A107) and two 8 bit attenuators. A comparitor, set to 100 mV, and a TTL latch provide output information to the microprocessor. See figure 02-1.

After the counter has a signal, and has taken a frequency reading, it starts the power meter task. This triggers the gate time counter, resets the TTL power latch, moves the yig ±50 MHz (to insure that the signal peak is passed through), then checks the TTL power latch. If the latch is set, the attenuation is increased in 3 dB steps (until the signal is attenuated below the level of the comparitor), then back one step. If maximum attenuation is reached, and the latch is still being set, the word OVERLOAD is displayed and the task is exited.

When the latch is first checked, if it is still reset, the attenuation is decreased in 3 dB steps until the comparitor level is reached. If minimum attenuation (maximum gain) is reached, the display is set to EE.E, and the task is exited.

After the attenuation is adjusted to a 3 dB resolution a successive approximation is performed to find the attenuation to a 0.1 dB resolution. The attenuation is stored, and if the gate time counter is not finished, the cycle is repeated. If the gate time counter is finished all the readings are averaged to eliminate the effects of AM on the signal.

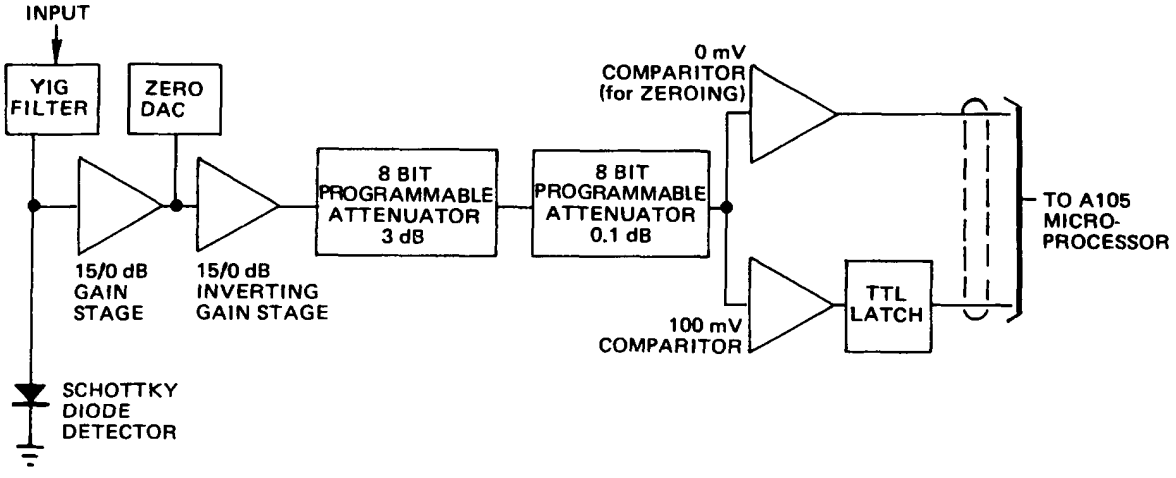


Figure 02-1. Power Meter Hardware

The "power vs power" and "power vs frequency" corrections are added, and the sum is displayed. A detailed flowchart of the power meter is shown is figure 02-2.

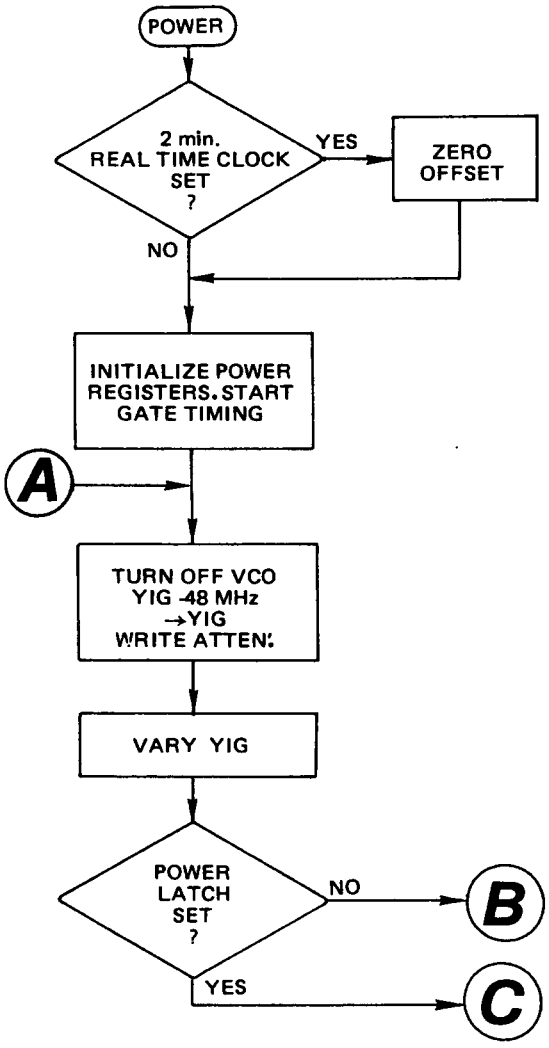


Figure 02-2. Power Meter Task

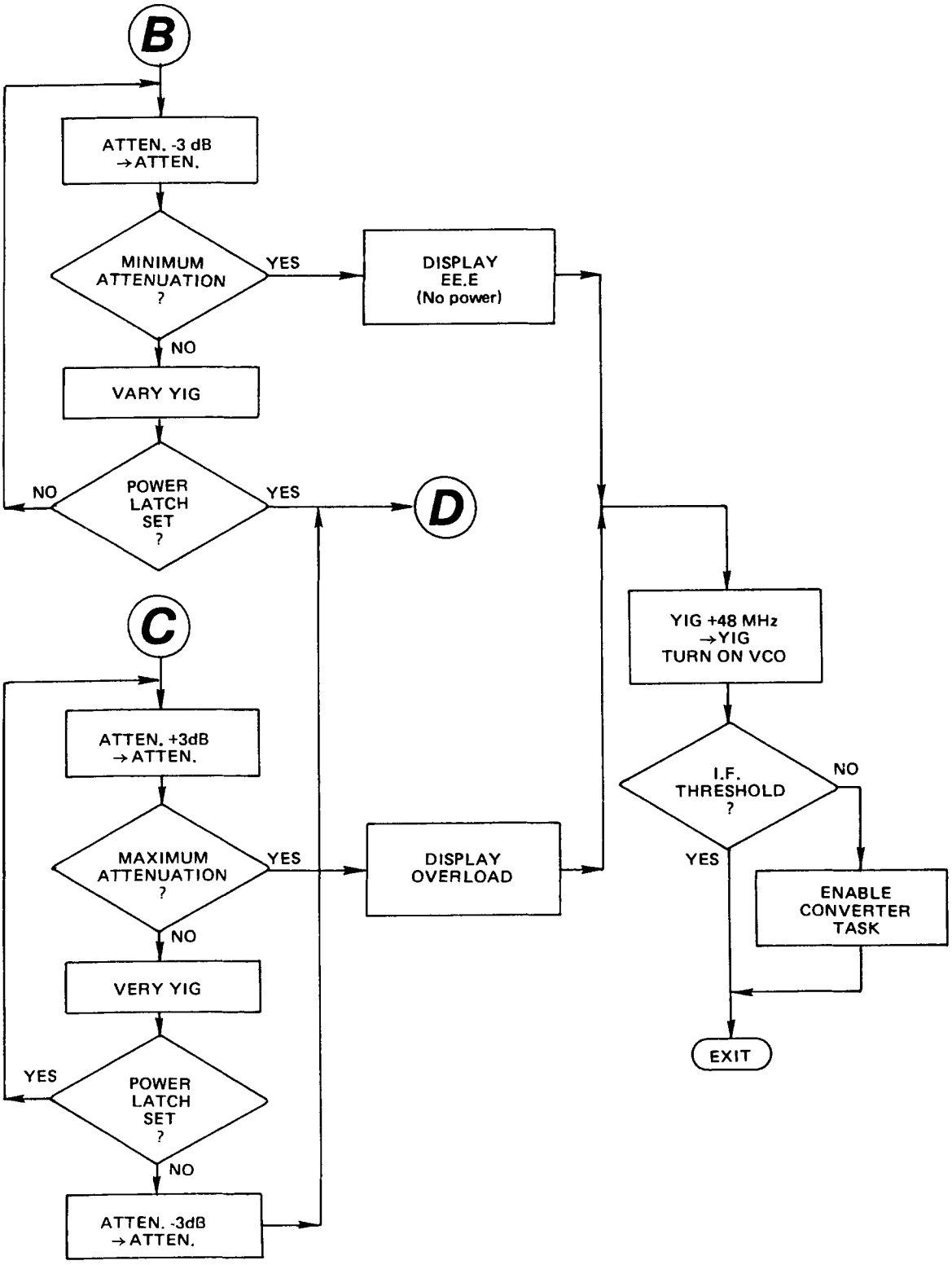


Figure 02-2. Power Meter Task, continued

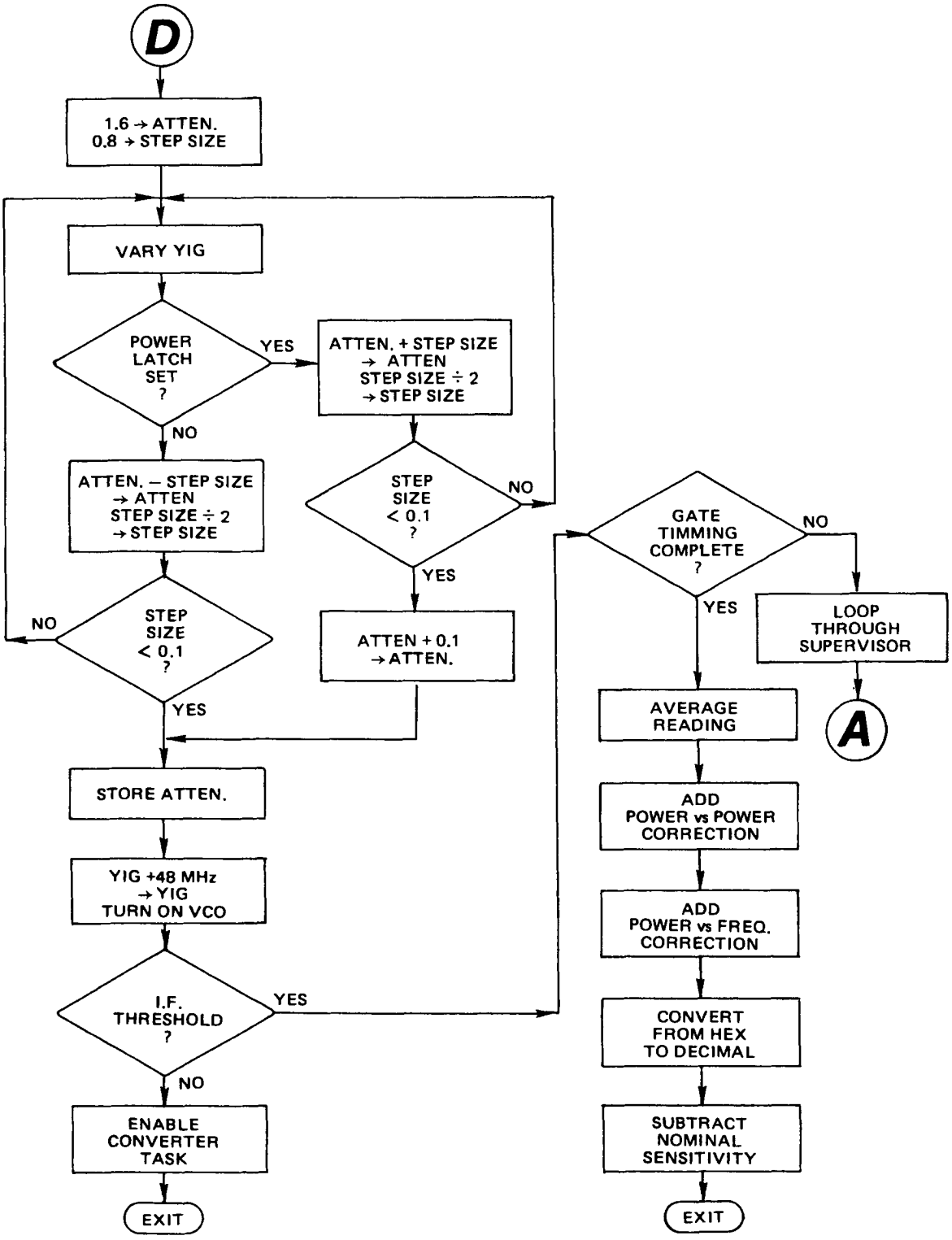


Figure 02-2. Power Meter Task, continued

CALIBRATION

The power meter contains 690 correction factors, stored in PROM.

The 150 "power vs power" correction factors compensate for variations from square law in the detector and power meter circuits. They are divided into three tables. The first table corrects variations below 10 GHz. The second corrects variations between 10 and 20 GHz. The third corrects variations above 20 GHz.

The 540 "power vs frequency" correction factors compensate for variations in the detector output at different frequencies. "Power vs frequency" corrections cover 0-27 GHz every 50 MHz.

The power meter is calibrated at the factory using specialized automatic test equipment. Because of the accuracy required, recalibration in the field is not recommended. If, however, recalibration is required, use the procedures given herein.

The test equipment required for calibration is:

MFG	MODEL	DESCRIPTION	CRITICAL PARAMETERS
H.P.	435A	Power Meter	Measures -30 to +15 dBm
Wavetek	2002	Sweeper	950 MHz - 2 GHz
Wiltron	6100	Microwave Sweeper	2 GHz - 18 GHz
Wiltron	6100	Microwave Sweeper	18 GHz - 26.5 GHz
E.H.		PROM Programmer	Programs TI 2516 PROMS

CAUTION

Be sure all connections are clean
and tight. Loose or dirty connections
will cause calibration errors.

1. Duplicate the power meter PROM, zeroing all corrections (address 0000-02B2 in the PROM). Install the uncorrected PROM in the counter.

2. Set the Wavetek to 2 GHz ±1 MHz. Connect the Wavetek to band 3 of the counter. Adjust the output until the counter reads -35 dBm.

3. Connect Wavetek to the power meter. Subtract the counter reading from the power meter reading. Round the result (R_1) to 0.1 dBm.

4. Using the following formulas, justify the correction to a number between 10 and 20.

$$\text{int}\,(R_1) - 1 = N \; ; \; (\text{int}\,(R_1) = \text{Whole number portion of } R_1)$$

$$10\,(R_1 - N) = \text{CORR}_{10}$$

$$\text{Convert CORR}_{10}\,\text{(decimal)} \rightarrow \text{CORR}_{16}\,\text{(hexidecimal)}$$

(R_1 is the result of step 3.)

5. Program the correction in these locations.

   0000 - 0005 inclusive
   0032 - 0037 inclusive
   0064 - 0069 inclusive

6. Connect the Wavetek to the counter. Increase power until the counter reads 1 dB higher.

7. Connect the Wavetek to the power meter. Subtract the counter reading from the power meter reading. Round the result (R_2) to 0.1 dBm.

8. Using the following formulas, calculate the correction.

$$10 (R_2 - N) = CORR_{10}$$

$$\text{Convert } CORR_{10} \rightarrow CORR_{16}$$

(R_2 is the result of step 7, and N was found in step 4.)

9. Program the correction in the 3 addresses found by the following formulas.

$$40 + P = Add\ 1_{10},\ Add\ 1_{10} \rightarrow Add\ 1_{16}$$

$$40 + P + 50 = Add\ 2_{10},\ Add\ 2_{10} \rightarrow Add\ 2_{16}$$

$$40 + P + 100 = Add\ 3_{10},\ Add\ 3_{10} \rightarrow Add\ 3_{16}$$

(P is the power the counter was set at in step 6.)

10. Repeat steps 6 through 9 until overload is reached on the counter.

11. Install the partially corrected PROM in the counter.

12. Set the Wavetek to 950 MHz, about -15 dBm.

13. Measure the power on the counter and power meter. Subtract the counter reading from the power meter reading. Round the results to 0.1 dBm. Multiply the results by 10 and convert to hex.

14. Program the correction in the address found by the following formula.

$$\frac{\text{FREQ (MHz)}}{50} + 150 = Add_{10}$$

$$Add_{10} \rightarrow Add_{16}$$

15. Increase frequency by 50 MHz. Repeat steps 13 and 14. Adjust the sweepers as necessary, until the upper frequency limit of the counter is reached.

Refer to section 9, pages 107-5 through 107-9, for parts list and schematic diagram. The counter recalibration is now complete.

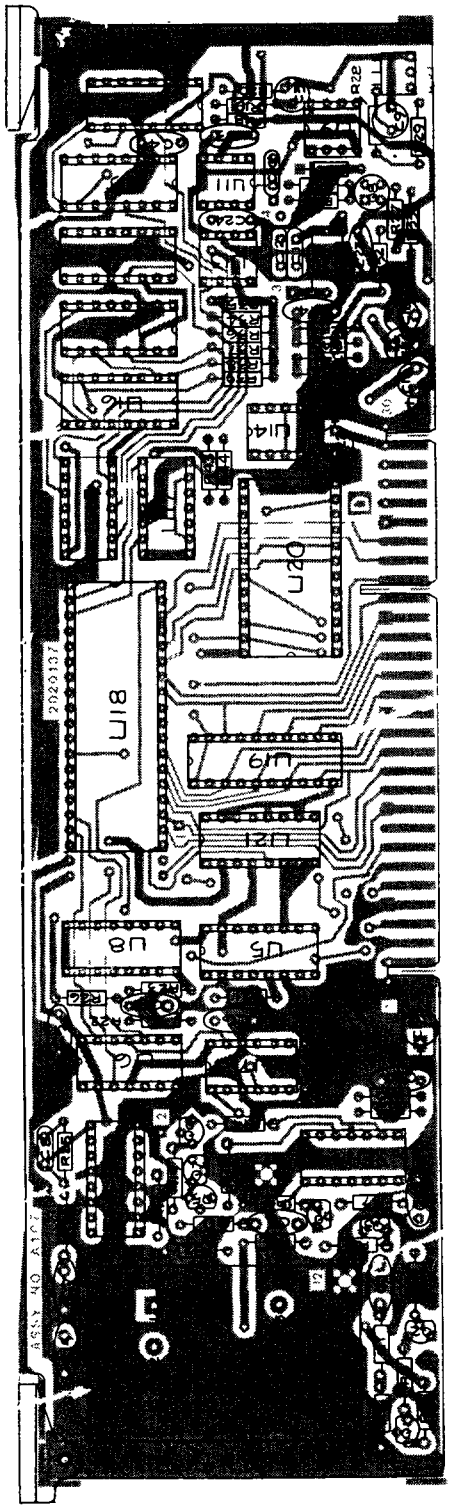


Figure 02-3. Gate Generator (Option 02) Component Locator

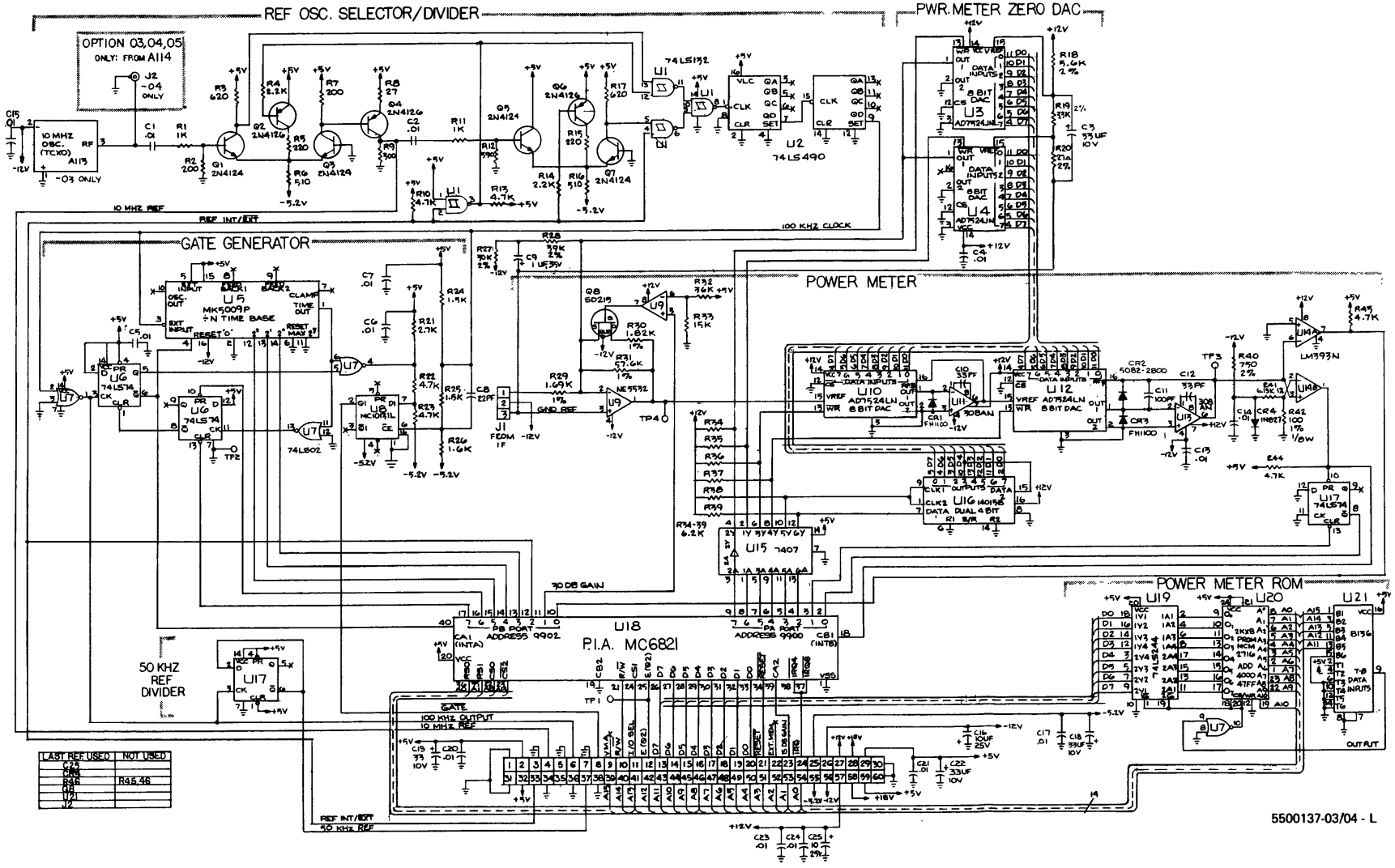


Figure 02-4. Gate Generator (Option 02) Schematic

OPTIONS 03, 04, 05
TIME BASE OSCILLATORS

Three Time Base Oscillators are available as options for either the model 545 or 548. These high stability options enhance the accuracy of the counter by the addition of oven stabilized crystal oscillators. These oscillators improve counter operation by reducing both time temperature variations.

When any one of these options is installed, the TCXO is removed from the Gate Generator board (A107) and the following components are added.

- One of three Oven Oscillators (A114) mounted on the chassis.
- 28 VDC Power Supply board (A112).
- Power Supply Transformer (T1) mounted on A112.
- Time Base Adjustment Pot (J2) mounted on the rear panel.
- Related interconnecting cable harnesses.

CHARACTERISTIC	OPTION 03	OPTION 04	OPTION 05
AGING RATE/24 HOURS (After 72 hour warm-up)	$< \lvert 5 \times 10^{-9} \rvert$	$< \lvert 1 \times 10^{-9} \rvert$	$< \lvert 5 \times 10^{-10} \rvert$
SHORT TERM STABILITY (1 second average)	$< 1 \times 10^{-10}$ rms	$< 1 \times 10^{-10}$ rms	$< 1 \times 10^{-10}$ rms
0° to + 50° C TEMPERATURE STABILITY	$< \lvert 6 \times 10^{-8} \rvert$	$< \lvert 3 \times 10^{-8} \rvert$	$< \lvert 3 \times 10^{-8} \rvert$
± 10% LINE VOLTAGE CHANGE	$< \lvert 5 \times 10^{-10} \rvert$	$< \lvert 2 \times 10^{-10} \rvert$	$< \lvert 2 \times 10^{-10} \rvert$

Figure 03/04/05-1. Time Base Oscillator Option Specifications

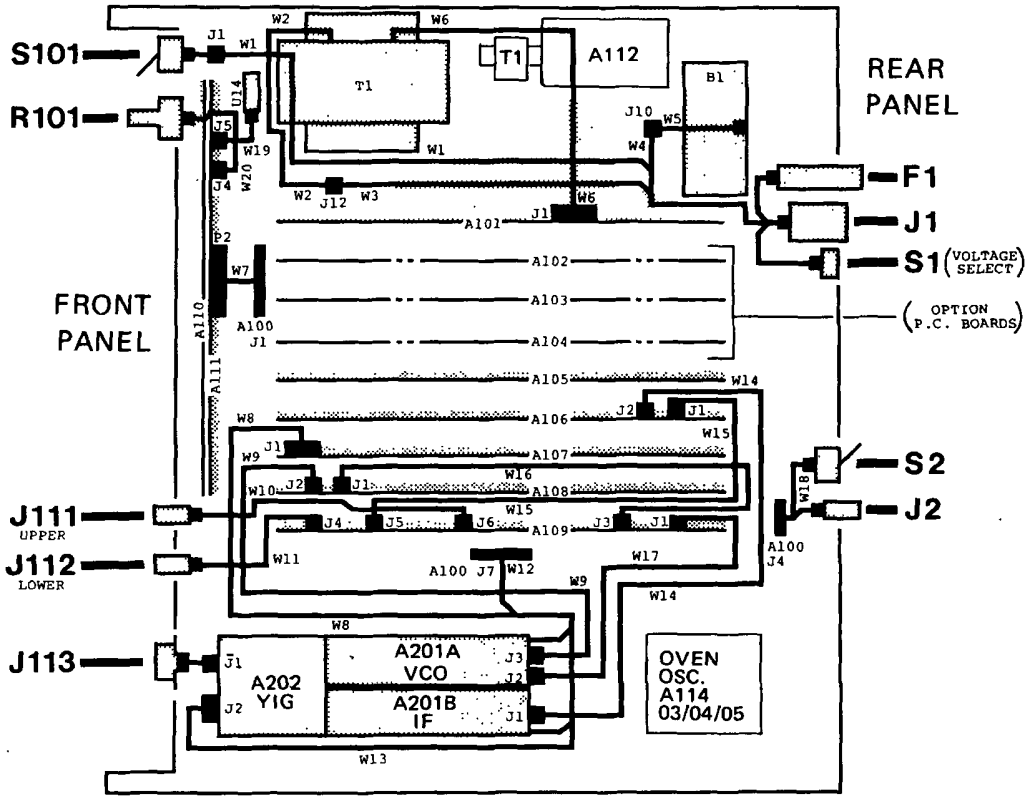


Figure 03/04/05-2. Component Location, Time Base Option

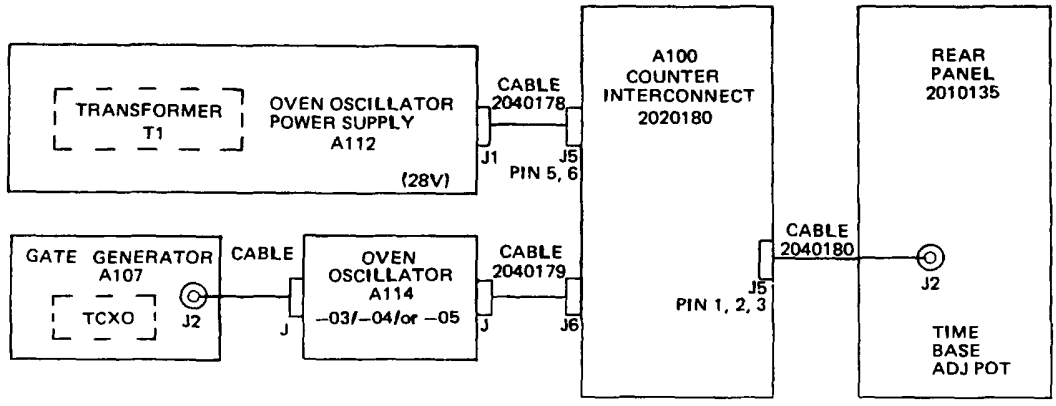


Figure 03/04/05-3. Time Base Option, Interconnection Diagram

OVEN OSCILLATOR POWER SUPPLY

The Oven Oscillator Power Supply board (A112) is a simple 28V regulated, current limited power supply. U1 and U2 provide voltage regulation, thermal protection and current limiting.

The transformer T1, CR1, C1 and C2 provide a 40V nominal unregulated DC voltage. The output voltage is set by voltage divider R5, R3 and R4. These resistors were selected so that 28V out provides 2.23V at U2 pin 2 (to U2 pin 1). Diode CR2 protects the supply from being pulled more negative than ground. See the schematic in figure 03/04/05-6.

The power supply (A112) is on and operating as long as the counter is connected to an active AC power source. The counter's POWER ON/OFF switch on the front panel does not control this assembly.

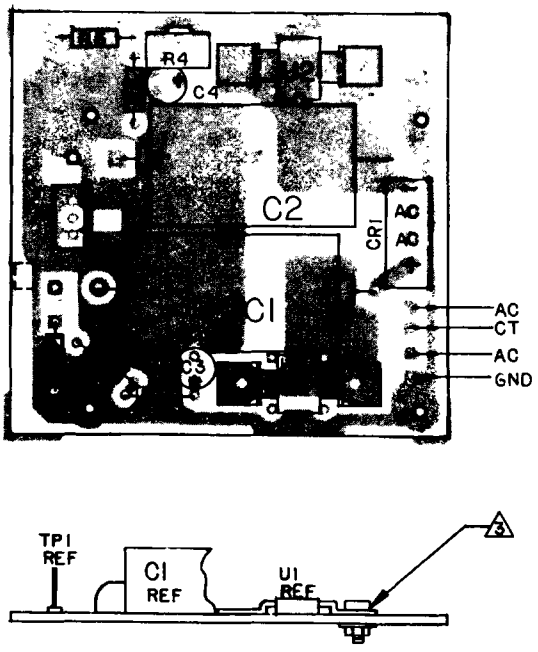


Figure 03/04/05-4. Oven Oscillator Power Supply (A112) Component Location

OVEN OSCILLATOR CALIBRATION

When options 03, 04 or 05 are installed in the counter, the effects of temperature perturbations and aging must still be considered, although the magnitude of the inaccuracies associated with each oscillator are greatly reduced.

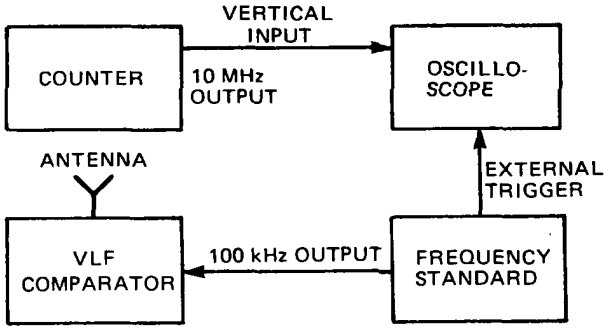
Full benefit of the oven stabilized oscillator characteristics can only be realized if the oscillator is running continuously (with counter always connected to a source of AC power). Under these conditions the perturbations in frequency will generally be in the positive direction for either an increase or decrease in temperature from + 25° C. The aging characteristic is also generally in the positive direction.

How frequently the oscillator is adjusted is determined by the level of accuracy required. To adjust the oscillator to an inaccuracy of less than 1×10^{-9} parts, relative to a standard, use this procedure. The test is illustrated in figure-5.

Observe the drift of the oscilloscope pattern. The fractional frequency offset is computed from:

$$\frac{T_{\text{drift of zero crossing}}}{T_{\text{observation time of drift}}} = \frac{\triangle f}{f}$$

If the pattern drifts, at a rate of .01 microsecond every 10 seconds, the frequency is in error by 1 part in 10^9.



OVEN OSCILLATOR A114

Figure 03/04/05-5. Time Base Calibration.

All frequency checks and adjustments should be made only after the oscillator has been connected to its power source for 24 hours. If the oscillator has been disconnected from its power source for more than 24 hours it may require 72 hours of continuous operation to achieve the specified frequency aging rate.

To measure oscillator frequency:

1. Connect the counter's internal oscillator output signal from the 10 MHz IN/OUT connector (on the rear panel of the counter) to the vertical input of the oscilloscope.

2. Trigger oscilloscope externally with the frequency standard. The VLF Comparator is used to determine the absolute frequency of the standard.

3. Set oscilloscope sweep rate to 0.1 μ sec/cm and expand X10; this results in a sweep rate of .01 μ sec/cm.

4. Adjust oscilloscope vertical controls for maximum gain.

5. Determine the frequency difference (see page 6-24).

6. Horizontal drift of oscilloscope display in μ sec/sec, is a measure of the difference between the frequency standard and the counter oscillator frequency. If the difference is excessive for the desired counter application, vary the TIME BASE ADJUST control on the rear panel of the counter until the pattern stops drifting.

NOTE

For highest accuracy, the counter should be operated for 72 hours prior to adjustment.

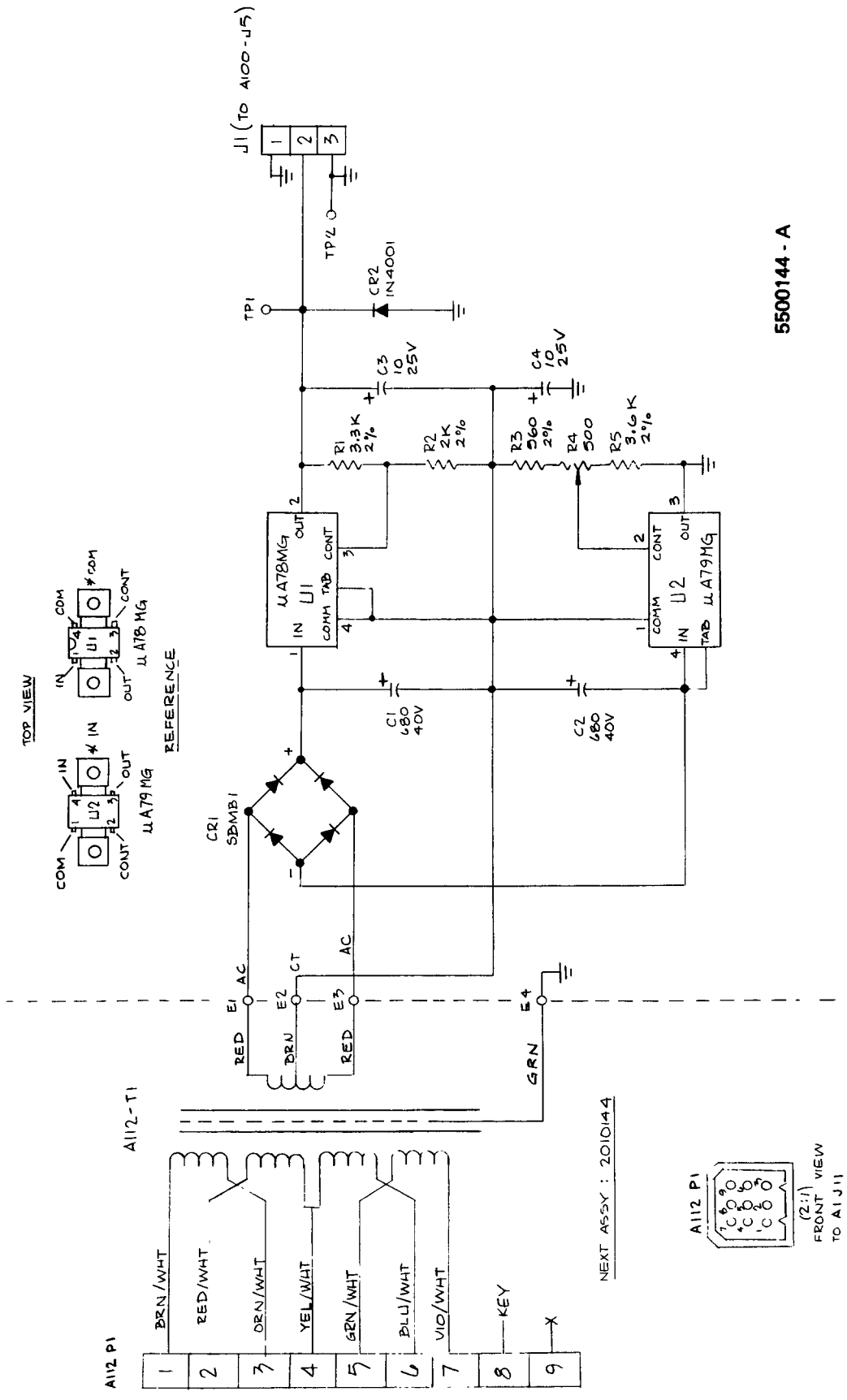


Figure 03/04/05-6. Time Base Option Schematic

OPTION 06
EXTENDED FREQUENCY CAPABILITY

The frequency range extention option is available on the model 548 counter. This option, when used with a remote sensor (model 591 for example), enables the counter to count signals in the frequency range that exceeds 26.5 GHz. This option consists of the following.

- Band 4 Converter Module, A204
- Band 4 Software
- Modified Front Panel Overlay
- Coax Cables, 2

SPECIFICATIONS

BAND	FREQUENCY RANGE	SENSITIVITY	MAX. INPUT	REMOTE SENSOR MODEL
41	26.5-40 GHz	-20 dBm	+5 dBm	591
42	40-60 GHz			*
43	60-90 GHz			*
44	90-110 GHz			*

* NOT YET AVAILABLE

OPERATION

To operate the counter in the 26.5—40 GHz range, connect the short cable (supplied with the remote sensor) from the lower output jack on the front panel, to the Band 3 input. Connect the long cable from the upper output jack to the remote sensor.

PRESS:	BAND	BAND annunciator blinks
PRESS:	4	BAND 4 annunciator blinks
PRESS:	1	BAND 4 annunciator lights stays on

The counter is now in the proper mode for operation.

NOTE: Before connecting the remote sensor to the frequency source, verify that the power level is within the limits specified for the sensor. When you connect the sensor the counter will automatically display the reading.

THEORY OF OPERATION – HARDWARE

When measuring a signal frequency greater than 26.5 GHz the 548, using the Option 06 Frequency Extension with a model 59X remote sensor, down converts the input to approximately 1.0 GHz. This signal is then fed to the Band 3 input, where a second conversion produces a 125 MHz 1F.

A multiplier chain increases the VCO output frequency to the 5.28–6 GHz range, which is referenced to the time base. See Figure 06-1. This signal provides the local oscillator (LO) power, which is transmitted to the remote sensor, an external harmonic mixer. When the input frequency and harmonics of the LO, (generated in the mixer) combine, a first IF is generated in the range of 1.00–1.35 GHz.

A diplexer separates the LO and IF signals received from the harmonic mixer. The level of the IF is then increased to a minimum of -25 dBm via the IF amplifier, then supplied to the Band 3 converter input.

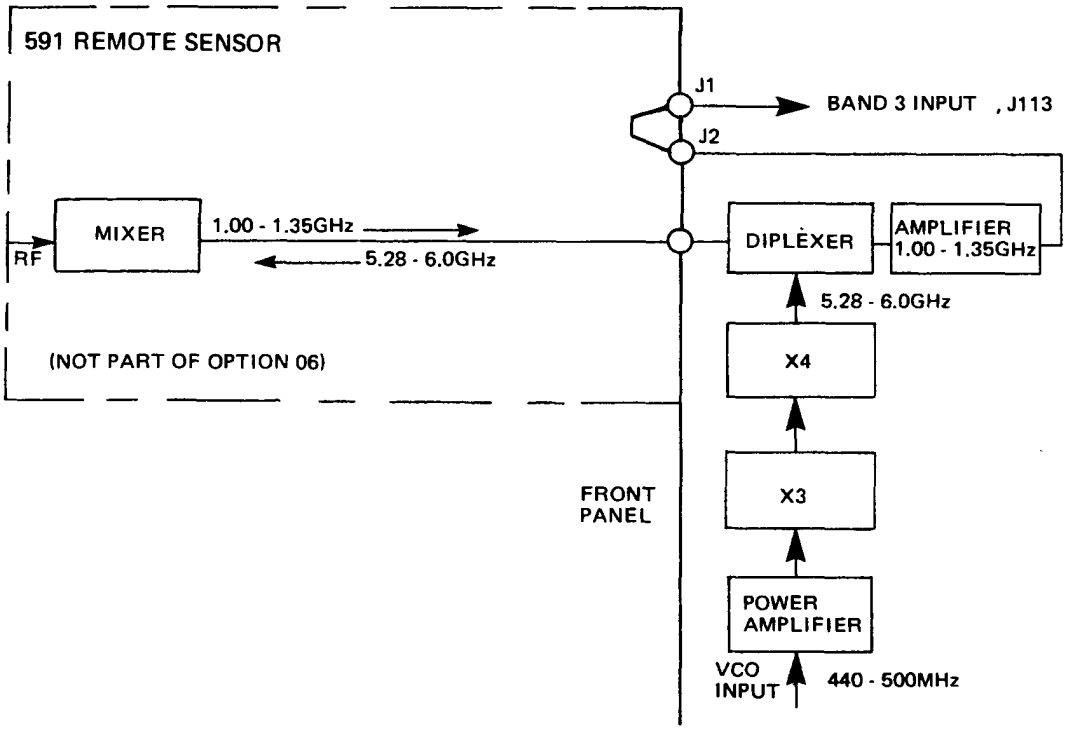


Figure 06-1. Frequency Extension Block Diagram

THEORY OF OPERATION – SOFTWARE

Band 4 acquires a signal by using a double conversion process. The microprocessor has control over the YIG filter and the VCO, thus making it possible to compute the approximate RF input signal, and down-convert the IF signal so it can be counted.

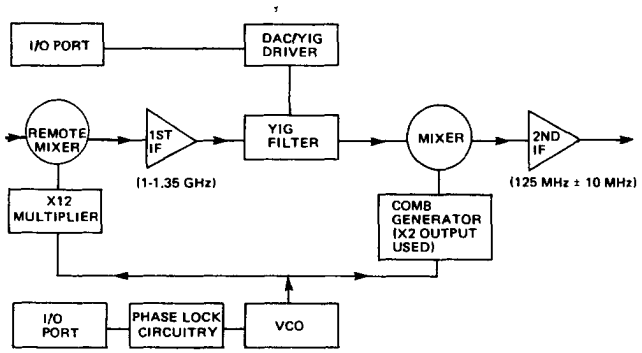


Figure 06-2. Down-conversion of Band 4 Signal

The following equations characterize this process.

$$RF\ INPUT = 12\ N\ F_{VCO} \pm 1st\ IF$$

$$1st\ IF = 2\ F_{VCO} + 2nd\ IF$$

therefore:

$$RF\ INPUT = \underbrace{F_{VCO}}_{\text{Controlled by Processor}}\ \underbrace{(12N \pm 2)}_{\text{calculated}}\ \underbrace{\pm 2nd\ IF}_{\text{IF counted}}$$

Sign depends on hi/low side mixing to produce 1st IF.

Where N = the harmonic number which is mixing with the RF to produce the first IF.

There are two main functions that the Band 4 program performs. It locks on to an incoming RF signal, and tracks an RF signal once it is locked.

The locking routine is called by the supervisor when any of the following conditions are met.

1. Selection of Band 4
2. Loss of IF threshold after being locked
3. Any reset condition

The tracking routine is used under the following two conditions.

1. After locking, the tracking routine is used to "fine tune" the locked signal.
2. When the RF signal is moving, the tracking routine is used to give a constant update of corrected parameters so that the YIG filter and VCO can stay locked onto the signal.

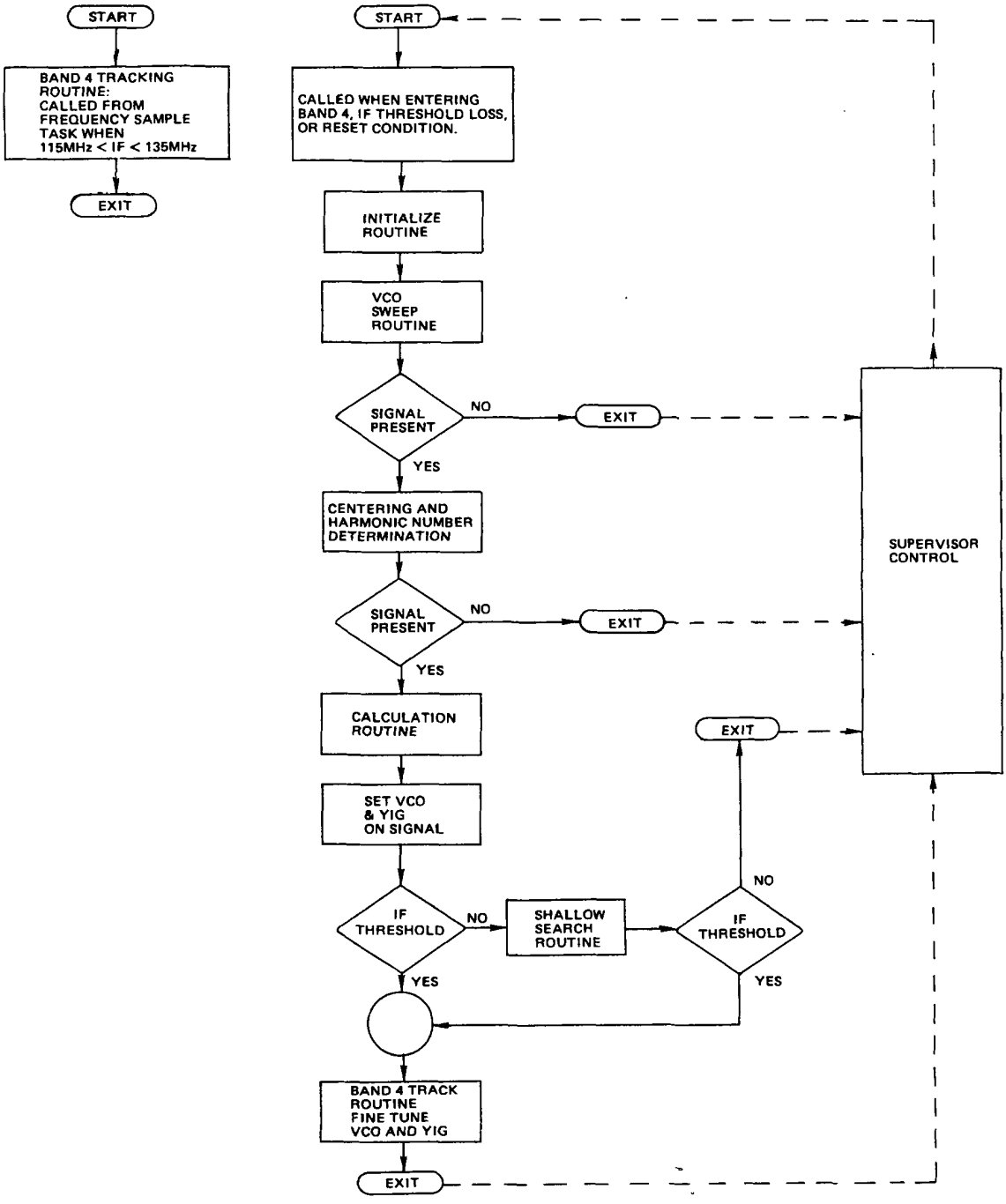


Figure 06-3. Band 4 Program, Flow Diagram

The process by which the program locks onto an RF signal is defined in the next six sections. Refer to Figure 06-3.

INITIALIZATION – The working table (BANDTP) for band 4 is cleared and the appropriate table of constants, used by the program for the particular Band 4 that has been selected, are loaded from PROM in this area. BANDTP is an area in RAM that is 27 bytes long.

VCO SWEEP – This routine steps the VCO frequency by a step size stored in BANDTP. After each step, the VCO frequency is checked for three stop points.

1. Top VCO frequency limit (500 MHz)
2. Wraparound frequency
3. Lockout frequency

If the top VCO frequency has been reached and no signal has been found, the program will return to the supervisor. If the top frequency is reached, and a signal has been detected, then the VCO is set to its low limit and the bottom range is searched until the wraparound frequency is reached.

If the wraparound frequency has been reached (the frequency at which the last VCO frequency has produced the strongest IF frequency), then the program will stay at this frequency, and will perform the centering and harmonic number determination routines.

If a lockout frequency (a VCO frequency at which erroneous locking results) is detected, the VCO frequency will be incremented by:

13 * STEP SIZE = NEW VCO FREQUENCY

and the program will continue from this frequency.

After each VCO step the YIG filter is swept to see if a signal is detected by the power DAC attenuator. If a signal was detected, the YIG is swept back and forth, and the attenuation is increased until the signal is lost. At this point a new VCO frequency is stepped and the process of signal detection continues, thus leaving the power DAC at the last setting to detect the next highest signal.

CENTERING AND HARMONIC NUMBER DETERMINATION – This routine will determine the harmonic number of the VCO which is causing the mix product to be in the proper range. (Refer to Figure 06-4).

First we obtain the proper step size for the calculation of the harmonic number (N). After the VCO sweep routine is complete and the VCO frequency is set, the incoming signal is mixed with a harmonic of the VCO frequency to produce a signal in a predetermined passband region. This signal is stepped to the outer edge of the passband (± step depending on whether the signal is high or low side mixed) by the following process.

1. Increment the VCO
2. Power level the IF signal
3. Center on the signal
4. Test for band limits

These steps are repeated until the edge of the passband is reached.

Harmonic Number N	Input Frequency Ranges	
	High Side Mixing (GHz)	Low Side Mixing (GHz)
5	25,395 – 28,875	27,405 – 31,125
6	30,675 – 34,875	32,685 – 37,125
7	35,955 – 40,875	37,965 – 43,125
8	41,235 – 46,875	43,245 – 49,125
9	46,515 – 56,875	48,525 – 55,125
10	51,795 – 58,875	53,805 – 61,125
11	57,075 – 64,875	59,085 – 67,125
12	62,355 – 70,875	64,365 – 73,125
13	67,635 – 76,875	69,645 – 79,125
14	72,915 – 82,875	74,925 – 85,125
15	78,195 – 88,875	80,205 – 91,125
16	83,475 – 94,875	85,485 – 97,125
17	88,755 – 100,875	90,765 – 103,125

Figure 06-4. Harmonic Mixing Ranges

Next the VCO is stepped back into the passband and a new centering takes place. This second center frequency is stored for later calculation of the harmonic number. Next the signal is stepped to the edge of the passband position it had just left, and it is centered. This center frequency is now compared to the first edge of the passband center frequency, and must be within 8 MHz. If it is not within 8 MHz it will be assumed that the signal is moving, and the Band 4 program is exited.

The IF frequency step size, caused by the VCO frequency step, is used to determine the harmonic number by the following equation.

$$\frac{\Delta \text{ IF FREQ. DUE TO VCO STEP}}{\text{HARMONIC SPACING}} = \text{HARMONIC \#(N)}$$

Where harmonic spacing = VCO step size X 12

CALCULATION ROUTINE – The calculation routine is used to find the approximate RF frequency Fin in the following manner.

1. Compute $F' = 12\,N * F_{VCO}$
2. Center the YIG filter on the first IF
3. Convert the binary YIG frequency to BCD
4. Compute $F_{IN} = F' \pm F_{YIG}$ (where F_{YIG} gives the approximate value for the first IF).
5. Compute a corrected VCO frequency using the equation:

$$F_{VCO} = (F_{IN} \pm 125) / (12N \pm 2)$$

Then tune the VCO with the corrected frequency and center the first IF frequency in the yig passband.

SHALLOW SEARCH – This routine tests for a signal in the IF passband. If a signal is present, the routine is exited. If a signal is not present, the routine will search an RF range of ±60 MHz (in steps of 200 kHz), for the signal, and continues if a signal is found. If a signal is not found, the Band 4 program returns control to the supervisor.

BAND 4 TRACKING – The tracking routine centers the second IF in the following range.

$$115 \text{ MHz} < \text{2nd IF SIGNAL} < 135 \text{ MHz}$$

This routine is called from outside of the Band 4 program to track a signal. A test is first made to determine if an IF threshold is present. If IF threshold is present it continues, if not the program returns to the supervisor to start the locking process from the beginning.

This routine reads the second IF frequency and computes the new VCO frequency so that the second IF is in the range given above. A new YIG frequency is calculated and the VCO and YIG are "tuned" to produce a new IF. A new FLO (frequency added to the second IF to produce the displayed frequency), is calculated. The equation for this process is:

$$F_{LO} = F_{VCO} (12 N \pm 2)$$

The YIG frequency is: NEW F_{YIG} = 2 (NEW VCO) + 125 MHz.

PERFORMANCE TESTS

The Band 4 converter module is not field repairable. When a malfunction is suspected, its operation can be checked from the front panel as follows:

IF AMPLIFIER — Apply a -50 dBm signal to the diplexer port (upper output jack) from 1.0 to 1.35 GHz. Output should be -3 dBm ±3 dB as checked on a spectrum analyzer connected to the IF output (lower jack).

LO SIGNAL — Connect a spectrum analyzer to the diplexer port (upper output jack). Using the following formula, set the VCO frequency between 440 and 500 MHz. The spectrum analyzer should show the 12th harmonic of the VCO frequency (5.28-6 GHz). The spectrum analyzer signal should be +3 dBm minimum, and free of breakup and spurious signals to -30 dBc.

To convert from the desired VCO frequency to the PIA program number:

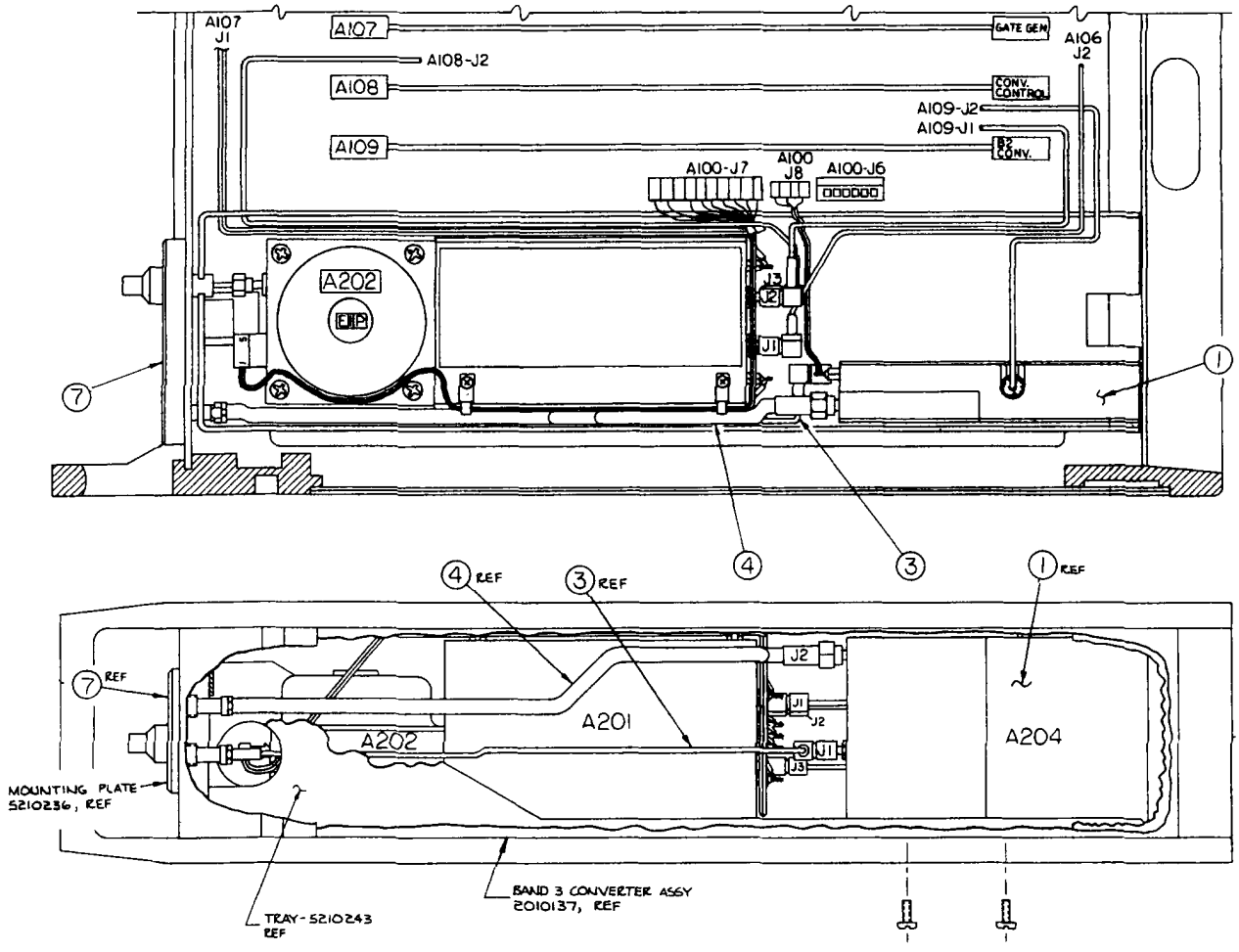
EXAMPLE (440.75 MHz)

1. Round the desired frequency to a multiple of 50 KHz (The resolution of the VCO frequency is 50 KHz).
2. Multiply the desired frequency (in MHz) by 5 . . . . . 440.75 X 5 = 2203.75
3. If the result contains no fractional part, go to step 8.
4. Multiply only the fractional part by 16 . . . . . .75 x 16 = 12
5. Add the result to the most significant digit from step 2 . . . . . MSD of 2203.75 = 2 – 2 + 12 = 14
6. Convert the result to hexadecimal . . . . . $14_{10} = E_{16}$
7. Replace the MSD from step 2 with the result from step 6 and drop the fractional part . . . . . 2203.75 → E203
8. The two most significant digits are programmed to address 9822, and the two least significant digits are programmed to address 9820.

To remove a defective converter:

1. Remove the line cord and both the top and bottom cover of the counter.
2. Remove the two screws holding the converter in place from the bottom.
3. Remove coaxial cables and unplug DC harness.
4. Lift the converter out of the counter.

To replace, proceed in the reverse order. See Figure 06-5 for location of the converter in the counter.



① Band 4 Converter – 201094

③ Cable (FP to A204J1) – 2040216

④ Cable (FP to A204J2) – 2040215

⑦ Overlay for 26.5 GHz and Extended frequency – 5210238

Figure 06-5. Location of Installed Band 4 Converter (A204)

OPTION 07
REMOTE PROGRAMMING/BCD OUTPUT

This option makes it possible to use a conventional printer or other readout device, and remotely program the functions that are normally done on the front panel of the counter.

SPECIFICATIONS

BCD OUTPUT

FORMAT	11 digits plus sign in parallel
"0" STATE	0.4 Volts at 4mA
"1" STATE	2.7 Volts at -400μA
NEGATIVE REF.	Ground
POSITIVE REF.	+5 Volts at 2K Ω Source Impedance
PRINT COMMAND	20 μs wide TTL Low level logic signal
INHIBIT INPUT	2 to 50 Volts High level logic signal

REMOTE PROGRAMMING

INPUT LOADING	1 Low power Shottky TTL load plus 10K pull up to +5 Volts
FUNCTIONS	All front panel controls except: Power ON/OFF, Sample rate, Clear Display, and test functions greater than 01.
OUTPUT LEVEL	Refer to "0" State and "1" State for BCD.

OPERATION

BCD OUTPUT

This binary-coded decimal (BCD) output (plus sign information) represents any numerical data that would normally be displayed by the eleven digits on the front panel of the counter. When the information being displayed represents the frequency alone the minus sign refers to the frequency. When the information being displayed represents frequency and power the minus sign refers to the power.

A 20 microsecond print command is provided to indicate when the data is valid. An inhibit command is provided that will prevent the data from being altered.

BCD OUTPUT PIN CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	10^1 A	16	10^8 B	31	10^3 D	46	10^0 C
2	10^1 B	17	10^9 A	32	10^4 C	47	10^0 D
3	10^2 A	18	10^9 B	33	10^4 D	48	Print Command
4	10^2 B	19	10^{10} A	34	10^5 C	49	Minus Sign
5	10^3 A	20	10^{10} B	35	10^5 D	50	Ground
6	10^3 B	21	10^0 A	36	10^6 C		
7	10^4 A	22	Inhibit	37	10^6 D		
8	10^4 B	23	10^0 B	38	10^7 C		
9	10^5 A	24	-Ref.	39	10^7 D		
10	10^5 B	25	+Ref.	40	10^8 C		
11	10^6 A	26	10^1 C	41	10^8 D		
12	10^6 B	27	10^1 D	42	10^9 C		
13	10^7 A	28	10^2 C	43	10^9 D		
14	10^7 B	29	10^2 D	44	10^{10} C		
15	10^8 A	30	10^3 C	45	10^{10} D		

NOTE

The 10^0 bit is the least significant digit, and corresponds to the 1 Hz output.

A, B, C, and D are the 1, 2, 4, and 8 bits of each binary coded decimal output digit.

REMOTE PROGRAMMING

All front panel functions can be remotely programmed except the Power on/off, Sample Rate, Clear Display, and test functions greater than 01. All the inputs are activated by a ground contact closure, or a "0" level TTL signal (0 = true). The input load is equal to one low power shottky TTL load, plus a 10 KΩ pullup to +5 volts.

CONTROL LINE FUNCTIONS

REMOTE ENABLE – A low level on this line transfers counter control from the front panel keyboard to the rear panel remote programming connector.

INPUT DATA – A low level on this line initiates a data read cycle to read the function/program data contained on the 22 data input lines. If this line is held low the counter will continuously pole the input data.

DATA ACCEPTED – This signal is output from the counter to the controller. The line goes high when data is being read by the counter, and goes low upon completion of a data read cycle.

PROGRAM DATA – A low level on this line indicates that the 22 data lines will be interpreted as program data. A high level on this line indicates that these lines will be interpreted as function data.

DATA LINE FUNCTIONS

RESET COUNTER – A low level on this line will reset the counter and initiate a new search for a valid signal.

UPDATE READING – A low level on this line will cause the counter to take a new reading, update the front panel display, and update the BCD output.

BAND SELECT (3 lines) – These lines select the band, or Test 01, in accordance with the following:

C	B	A	BAND
0	0	0	Test 01
0	0	1	Band 1
0	1	0	Band 2
0	1	1	Band 3
1	0	0	Band 4.1*
1	0	1	Band 4.2*
1	1	0	Band 4.3*
1	1	1	Band 4.4*

*In counters that do not have Option 6, the C bit does not apply.

RESOLUTION (4 lines) – These lines program the remote resolution. A four digit BCD number (0 through 9) will indicate the number of digits that are blanked.

DAC SELECT (4 lines) – These lines select the most significant digit of the DAC option (01), when it is installed in the counter. A hexadecimal number (1 to B) will select digit 1 to 11 as the MSD of the 3 digits output to the DAC. Any other digit disables the DAC option.

HOLD MODE – A low level on this line will place the counter in the hold mode (data not updated until the counter is reset).

FAST CYCLE – A low level on this line will place the counter in the fast cycle mode (no display time).

POWER METER – A low level on this line will enable the power meter on counters with Option 02.

VIEW FUNCTION LINES (5 lines) – A low level on one of these lines will cause the counter to display the indicated function on the front panel and the BCD output. If more than one line is enabled at a time, the counter will display the first one found in the following order.

1. DAC Select
2. Frequency Limit Low
3. Frequency Limit High
4. Frequenty Offset
5. Power Offset

PROGRAM LINE FUNCTIONS

PROGRAM SELECT (2 lines) – These two lines select one of four functions to be programmed by the program data in accordance with the following.

SELECT BIT b	SELECT BIT a	FUNCTION PROGRAMMED
0	0	Frequency limit low
0	1	Frequency limit high
1	0	Frequency Offset
1	1	Power Offset

MINUS SIGN – When this line is low the four digits of programming data are interpreted as a negative number.

EXPONENT (3 lines) – These three lines are interpreted as a BCD number (0 to 7). This number is the power of 10 that is to be multiplied, times the four digits of data (data X 10^{X}). This multiplier is used for all frequency input data, and is ignored for the power input data.

DIGIT 1 TO DIGIT IV (4 lines each) – These are four BCD digits that represent the input data. Digit 1 is the MSD and Digit IV is the LSD. For power input, a decimal point is located between Digit II and Digit III, and Digit IV is not used.

DATA ENTRY

Preceeding any data entry sequence, the counter must be placed in the remote mode (remote enable line low). Once in remote mode, the input data line is brought low to initiate a data read sequence. The data read is normally function data. When the program data line is brought low, the data read will be interpreted as program data. The data accept line will go high to indicate that the data has been latched in, and will remain high while the counter processes this data.

Figure 07-1 shows the data entry timing sequence. The input data line debounce time (1) is typically 16 to 18 ms. Data is latched into the counter 48 μs before the data accept line goes high (2). As soon as the data accept line goes high, all data (except remote enable) can be removed. The data accept line stays high while the counter processes the input data. This process is data dependent, and can take from 1 to 140 ms (3). To prevent the counter from setting the pole mode, the input data line must go high within 100 μs after the data accept line goes low (4). If pole mode is set, the next data read cycle will occur between 0 and 100 ms after the high to low transition of the data accept line. After this first data read cycle, all subsequent data read cycles will occur at 100 ms intervals.

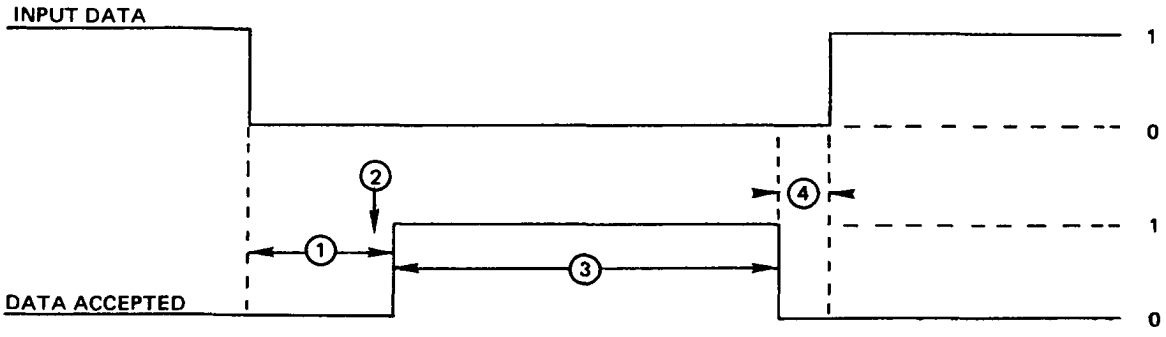


Figure 07-1. Data Entry Timing

DATA ENTRY EXAMPLE

The following example remotely programs the counter to be in Band 3 with 1 kHz resolution, and a -160 MHz frequency offset.

1. Put counter in remote mode by bringing the remote enable line low.
2. Set the program data to be entered by bringing the program data line low.
   a. Set digit 1=1
      Set digit 2=6
      Set digit 3=0
      Set digit 4=0
   b. Set the exponent =5 (1600×10^5)
   c. Set program select A=0, B=1 (frequency offset)
   d. Set minus sign low (negative offset)
3. Enter program data by bringing the input data line low until the data accept line goes high.
4. Set the remote function data.
   a. Return all lines high except the remote enable line.
   b. Set the resolution A and B lines low (resolution 3).
   c. Set the Band select C line low (Band 3).

   NOTE: Counters that do not have Option 06 (Band 4) will set Band 3, even with the select line C high.
5. Enter function data by bringing the input data line low until the data accept line goes high.

REMOTE PROGRAMMING PIN CONNECTIONS

PIN	FUNCTION DATA	PROGRAM DATA
1-5	BCD Data (Do not use these pins)	
6-12	Ground	
13	DAC Select A	Digit II A
14	DAC Select B	Digit II B
15	DAC Select C	Digit II C
16	DAC Select D	Digit II D
17	Resolution A	Digit I A
18	Resolution B	Digit I B
19	Resolution C	Digit I C
20	Resolution D	Digit I D
21-24	No connection	
25	Program Data)	Program Data)
26	Remote Enable) Control Lines	Remote Enable) Control Lines
27	Input Data)	Input Data)
28	Data Accepted)	Data Accepted)
29	View Power Offset	Digit IV A
30	View Frequency Offset	Digit IV B
31	View Frequency Limit High	Digit IV C
32	View Frequency Limit Low	Digit IV D
33	View DAC Select	Digit III A
34	Power Meter Enable	Digit III B
35	Fast Cycle Mode	Digit III C
36	Hold Mode	Digit III D
37	Ground	Ground
38-44	No connection	
45	Band Select A	Exponent A
46	Band Select B	Exponent B
47	Band Select C	Exponent C
48	(No function)	Minus Sign
49	Update Reading	Program Select A
50	Reset Counter	Program Select B

THEORY OF OPERATION

The BCD/REMOTE programming board takes data from the display and formats it as parallel data output for the rear panel. It also receives counter control and programming information from the 26 line input on the rear panel to provide for remote control of the counter.

BCD THEORY OF OPERATION

During each update cycle, the counter checks for the existence of the BCD/RMT board. If the board exists, the program checks the state of the inhibit input. If the inhibit input is true (+2 to +50V on the input), the program jumps past the BCD output but the counter continues to update the display. If the input is low, the program scans through each of the 11 digits (LSB to MSB). Each digit is checked, and any non-numerical digit is replaced by a zero. The resulting BCD digit is then sent to U2 through 4 bits of port B of the PIA (U14). After each digit is made available to U2, 4 clock pulses (BCD Clock) are sent to U2 (through U7) to shift all the data in the shift registers to the right by 4 bits (1 digit). At the end of these data shift pulses, a BCD load pulse enters the new data into U2. When the last digit (MSB) is entered into U2, the sign bit is simultaneously entered into U1. After all the data has been entered into the shift register, the program sends out a 20 microsecond print command.

REMOTE PROGRAMMING THEORY OF OPERATION

When the remote enable line is high, none of the other remote programming lines can effect the counter. When the remote enable line is brought low, the counter changes from local to remote operating conditions and switches control for the counter from the front panel keyboard to the rear panel remote programming connector. When in the remote mode, the counter waits for an input from the INPUT DATA request line. When the input data line is brought low, the data direction control line is sent low to put U9 in the low impedance buffer mode. The RMT LOAD line is then toggled to load all remote input data into the input registers (U8-U12). The counter then changes the data accepted output from a low to a high to indicate that the data has been read. The 8 bits of data into U14 (from U8 and U10), are read by the microprocessor. Groups of 4 clock pulses are then sent out (on the RMT CLOCK line), to shift the input data into U10 where the data is read by the microprocessor through U14. When all the data has been read, the data direction control line is returned to a high level, and the data accept line is returned to low, indicating the data has been accepted by the counter.

When the INPUT DATA line is held low, the counter sets a flag and returns to read the input data at approximately 100 millisecond intervals. This continues until the INPUT DATA line is returned to high, at which time the counter returns to the condition where it is waiting for a high to low transition on the INPUT DATA line.

When the remote enable line is returned to the high state (local mode), the counter exercises a clear display function and then returns to the (previous) local mode condition.

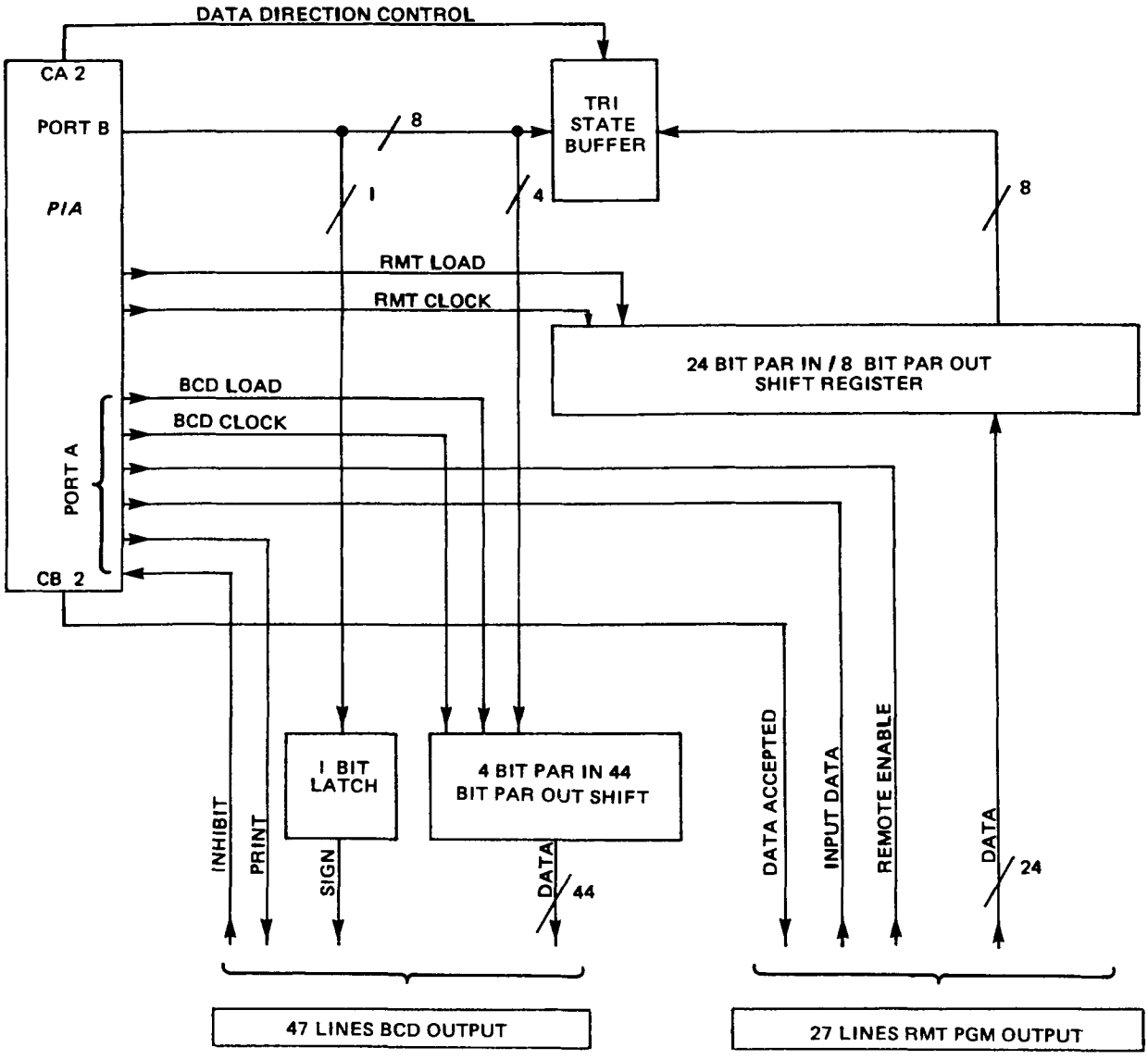


Figure 07-2. Remote Programming/BCD Output Simplified Block Diagram

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OPTION 07 - REMOTE PROGRAMMING / BCD OUTPUT

2020141 - A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
07	REMOTE PROGRAMMING / BCD	2010141		EIP	
-1	Bail Mount Kit	5000195	1	3475-1	76381
-2	Cable, Flat Ribbon	2040176	2		
-3	PCB Assy, A102 A	2020132	1	EIP	
C1	Tant, 33uF, 10%, 10V	2300015	1	TAG-20-33/10-50	14433
C2 thru C5	Cer, .01uF, 20%, 100V	2150003	4	TAG-S10	56289
Q1	Transistor, NPN	4704401	1	2N4401	04713
R1	Comp, 1 K, 5 %, ¼ W	4010102	1	RC07GF102J	81349
R2	Comp, 5.6K, 5%, ¼ W	4010562	4	RC07GF562J	81349
R3	Comp, 10K, 5%, 1/8 W	4010103	1	RC07GF103J	81349
R4	R2				
R5	Comp, 2.7K, 5%, ¼ W	4010272	2	RC07GF272J	81349
R6	R5				
R7	R2				
R8	R2				
RN1 thru RN3	Network, 10 pin , 10K, ± 2%, 1.25W	4170003	3	4310R-101-103	32997
TP1 thru TP11	.040 Dia. Conn. Pin	2620032	11	460-2970-02-03	71279
U1	4 bit Shift Register	3084195	4	SN74LS195AN	01295
U2	U1				
U3 thru U7	Serial IN/Parellel OUT Register	3084164	5	SN74LS164	01295
U8	U1				
U9	Line Driver/Octal Buffer Inverter	3084244	1	SN74LS244N	01295
U10	U1				
U11	8 bit Shift Register	3084166	2	SN74LS166N	01295
U12	U11				
U13	Hex Inverter/Schmitt Trig.	3087414	1	SM74LS14N	01295
U14	P.I.A.	3086821	1	MC6821	04713

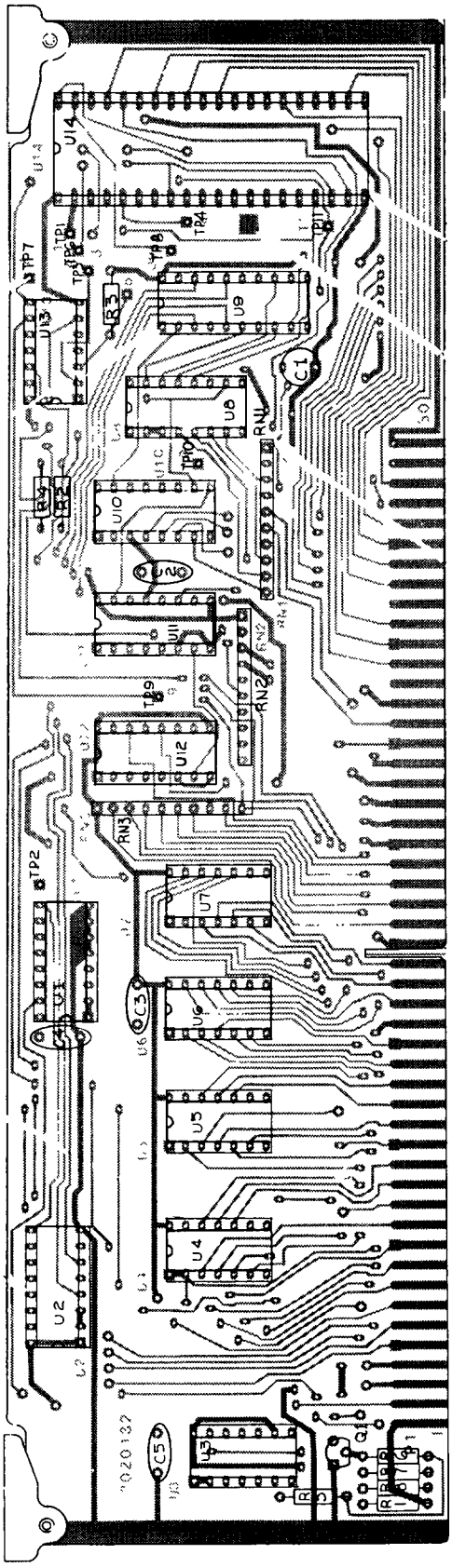
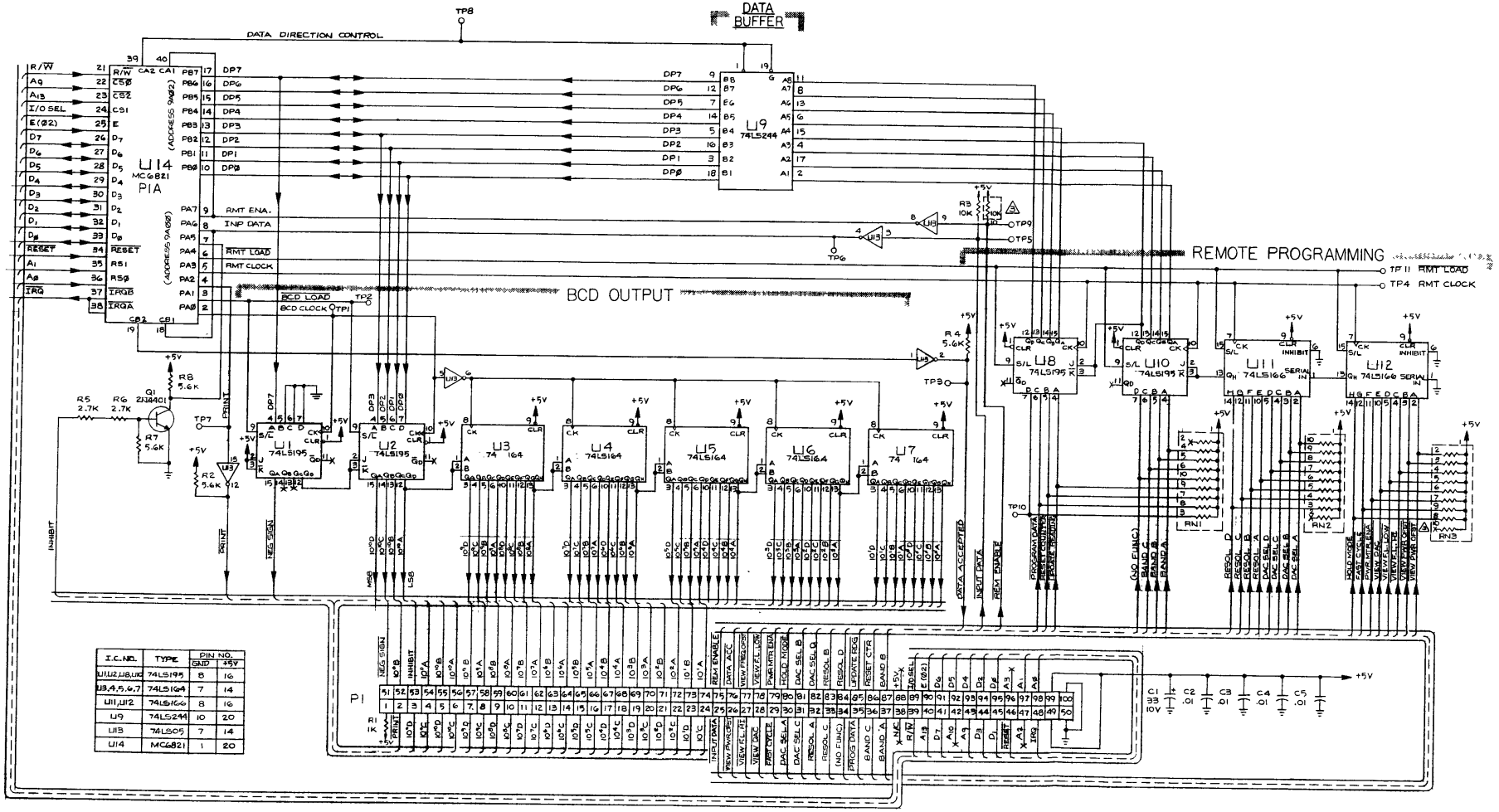


Figure 07-3. Remote Programming / BCD Output, Component Locator



I.C. NO.	TYPE	PIN NO. GND	PIN NO. +5V
U1,U2,U8,U10	74LS195	8	16
U3,4,5,6,7	74LS164	7	14
U11,U12	74LS166	8	16
U9	74LS244	10	20
U13	74LS05	7	14
U14	MC6821	1	20

△3 RESISTOR AT TP9 PART OF RN3 PIN 10.

5500132-A

Figure 07-4. Remote Programming / BCD Output Schematic Diagram

OPTION 08
GENERAL PURPOSE INTERFACE BUS

Option 08 makes the 545/548 microwave counters fully compatible with the General Purpose Interface Bus (GPIB). With this option the counters can respond to remote control instructions and can output measurement results via the IEEE 488-1978 Bus Interface. At the simplest level the 545/548 can output data to other devices such as the HP 5150A Thermal Printer. In more sophisticated systems a calculator or other system controller can remotely program the 545/548, trigger measurements, and read results. Of course, a calculator or computer adds other benefits to a GPIB based measurement system. The calculator can manipulate data to compute the mean and standard deviation, check for linearity, and compare results to limits, or perform many other functions.

This technical note describes how to use the HP 9825, 9845A, and TEK 4051 calculators to program the EIP 545/548 microwave counters. Before starting to operate a system it certainly helps to be familiar with the selected calculator, the capabilities of the GPIB, and the manual operation and capabilities of the 545/548.

EQUIPMENT

The procedures described in this note apply to a GPIB based system containing at least the following:

- EIP 545 or 548 microwave counter
- HP 9825A, 9845A, or TEK 4051 calculator
- HP 98034A GPIB calculator interface
- Appropriate interconnect cables

SETTING ADDRESS SWITCH

The EIP 545/548 automatic microwave frequency counters employ a decimal address switch located inside the units. These are set for decimal address 19 at the factory. To verify the switch setting without removing the top of the instrument, simply initiate test 10; enter 9C04 through the keyboard; and read the address right from the counters own display (see description of test 10). After reading the address, terminate test 10 by pushing the clear display key.
The examples given here assume an address setting of decimal 19 or ASCII talk address "S" and listen address "3".

The address switch is also used to put the 545/548 counter into the talk only (to) or listen only (lo) mode of operation. to put the counter into the listen only mode, simply set the address switch to any number 41 or higher.

ADDRESS CHARACTERS		ADDRESS CODES					
Listen	Talk	binary					decimal
		5	4	3	2	1	*
SP	@	0	0	0	0	0	00
!	A	0	0	0	0	1	01
"	B	0	0	0	1	0	02
#	C	0	0	0	1	1	03
$	D	0	0	1	0	0	04
%	E	0	0	1	0	1	05
&	F	0	0	1	1	0	06
'	G	0	0	1	1	1	07
(	H	0	1	0	0	0	08
)	I	0	1	0	0	1	09
*	J	0	1	0	1	0	10
+	K	0	1	0	1	1	11
,	L	0	1	1	0	0	12
–	M	0	1	1	0	1	13
.	N	0	1	1	1	0	14
/	O	0	1	1	1	1	15
0	P	1	0	0	0	0	16
1	Q	1	0	0	0	1	17
2	R	1	0	0	1	0	18
3	S	1	0	0	1	1	19
4	T	1	0	1	0	0	20
5	U	1	0	1	0	1	21
6	V	1	0	1	1	0	22
7	W	1	0	1	1	1	23
8	X	1	1	0	0	0	24
9	Y	1	1	0	0	1	25
:	Z	1	1	0	1	0	26
;	[	1	1	0	1	1	27
<	/	1	1	1	0	0	28
=	]	1	1	1	0	1	29
>	^	1	1	1	1	0	30

* Decimal Talk/Listen Address is provided as a cross reference for those controllers which use decimal address.

Figure 08-1. Allowable Address Codes

The counter can be put into 4 different modes of operation in the talk only mode. The following is a list of the address settings for entering into the 4 modes of operation.

ADDRESS	MODE OF OPERATION
31	Continuous output determined by SAMPLE RATE control. Exponent in scientific format.
32	Continuous output - fast active. SAMPLE RATE control inactive. Exponent in scientific format.
33	Continuous output determined by SAMPLE RATE control. Exponent in zero output format.
34	Continuous output - fast active. SAMPLE RATE control inactive. Exponent in zero output format.

NOTE: In the Talk Only or the Listen Only mode, the address of the counter is always automatically set to decimal 0.

GPIB FUNCTIONS IMPLEMENTED

The GPIB interface function subsets implemented are:

SH1	complete capability
AH1	complete capability
T5	basic talker, serial poll, Talk Only mode, unaddress if MLA
L3	basic listener, Listen Only mode, unaddress if MTA
SR1	complete capability
RL2	no local lockout
DC1	complete capability
DT1	complete capability

NOTE: When DEVICE CLEAR or SELECTED DEVICE CLEAR GPIB bus command is received, the 545/548 counter will revert itself to the power on state.

When DEVICE TRIGGER GPIB bus command is received, the counter will initiate a new frequency reading cycle. The converter will not be reset.

PROGRAMMING THE 545/548

The 4051 uses PRINT and the 9845A uses the OUTPUT statement to program the 545/548. The 9825A uses the WRT (I/O address) (decimal address) to program the 545/548. The calculators address the counter to talk and listen, then transmits a series of program codes. The codes to control the operation of the 545/548 are listed in the program set. Suppose you have set one counter to decimal talk/listen address 19. Then typical statements to program the counter are:

- TEK 4051: PRINT @ 19: "B3R2F01. 44M"
- HP 9845A: OUTPUT 719: "B3R2F01. 44M"
- HP 9825A: WRT 719: "B3R2F01. 44M"

PROGRAM CODE SET

Codes underlined indicate start-up conditions. These conditions are set by the device clear or selected device clear, or power on.

DISPLAY

HP – Hold Passive
HA – Hold Active
DA – Display Active: Output Frequency Reading to Front Panel and Bus
DP – Display Passive: Output Frequency Reading to Bus only
DN – Display Normal

BAND

B1 – Band 1: 10Hz - 100MHz
B2 – Band 2: 10MHz - 1GHz
B3 – Band 3: 1 GHz - 18GHz (Model 545) / 26.5 GHz (Model 548)
B4 – Band 4: 26.5GHz - 40GHz (Model 548/Opt. 06)

RESOLUTION

R0 – Resolution 0 = 1Hz
R1 – Resolution 1 = 10Hz
R2 – Resolution 2 = 100Hz
R3 – Resolution 3 = 1KHz
R4 – Resolution 4 = 10KHz
R5 – Resolution 5 = 100KHz
R6 – Resolution 6 = 1MHz
R7 – Resolution 7 = 10MHz
R8 – Resolution 8 = 100MHz
R9 – Resolution 9 = 1GHz

MEASUREMENT FUNTION

FA – Fast Active (Ignore sample rate Pot)
FP – Fast Passive (Terminates FA)
RS – Reset Basic Counter and Converter. Take a new reading after reset.

OFFSETS

FO – Frequency Offset. Take a new reading after data entry.
PO – Power Offset. Take a new reading after data entry.
* OA – Offset Active:
—Add Frequency Offset to Frequency Reading
—Add Power Offset to Power Reading if Power Meter Function is active
OP – Offset Passive (Terminates OA)

* In Start-up Condition, although OA is Active, "0" (zero) Frequency and Power Offsets are programmed.

POWER METER

PA – Power Meter Option Active. Initiate a new gate.
PP – Power Meter Option Passive (Terminates PA)

* MEASUREMENT PARAMETERS

FH – Frequency Limit High. Basic counter and converter will be reset after data entry.
FL – Frequency Limit Low. Basic counter and converter will be reset after data entry.

SELF-TEST FUNCTIONS

TA – Test Active. (200MHz self-test)
TP – Test Passive. (clear test function)

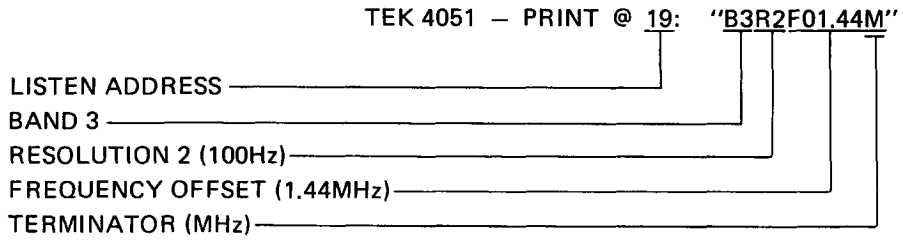
DATA FORMAT

EZ – Exponent Zero
ES – Exponent Scientific

DATA OUTPUT

RA – Stay in data output mode during data output
RP – Service other operations of the counter after outputting each BYTE.
TS – Service request enabled
TN – Service request disabled

* Measurement parameters: Standard Software
Limits of 950MHz (LOW) and 18.5GHz (HIGH) (27GHz for Model 548) are featured in each counter at turn on.



FORMAT OF GPIB INSTRUCTIONS

<OP CODE> <NUMBER> <TERMINATOR>

OPERATION CODE or OP CODE can take any of the following formats:

< LETTER> < LETTER> or <LETTER> <DIGIT>

Example = FH (Frequency limit high) or B3 (band 3)

The NUMBER portion of the statement can take the form of any of the following:

< SIGN> <DIGIT STRING> or <DIGIT STRING> <SIGN>

Example: –2457 or 2457 – = –2457

<SIGN> <DIGIT STRING>•<DIGIT STRING>

Example: –3.483

<DIGIT STRING>•<SIGN> <DIGIT STRING>

Example: 523. –416 = –523.416

<DIGIT STRING>•<DIGIT STRING> <SIGN>

Example: 478.231– = –478.231

NOTE: Spaces, carriage returns and line feeds within the <NUMBER> portion of the instructions are always ignored.

The TERMINATOR allows the operator to choose the scale of a chosen input number as well as implement special functions.

TERMINATOR = G/M/K/H/D/P/C

Example = G, M, K, H, represent GHz, MHz, kHz and Hz
D = dB, P = clear data, (equivalent to "clear data" key on keyboard)
C = clear display (equivalent to "clear display" key on keyboard)

DEFINITIONS

<SIGN> = + or – (or Omitted = +)

<DIGIT STRING> = <DIGIT ><DIGIT><DIGIT>– – – – –

<DIGIT> = 1/2/3/4/5/6/7/8/9/0

< LETTER > = A/B/C/D/E/F/G/H/I/J/K/L/M/N/O/P/Q/R/S/T/U/V/W/X/Y/Z

< NUMBER > = < SIGN > < DIGIT STRING >

<DIGIT STRING> <SIGN >

<SIGN> <DIGIT STRING> • <DIGIT STRING>

<DIGIT STRING> • <SIGN> <DIGIT STRING>

<DIGIT STRING> • <DIGIT STRING> <SIGN>

<NULL

AVAILABLE COMMANDS

FO – FREQUENCY OFFSET - Enables entry of frequency offsets. (1 Hz resolution available.) The basic counter and converter will be reset after the data entry.

FH – FREQUENCY LIMIT HIGH - Indicates the numbers and scale factor will set frequency limit high (10 MHz resolution available). The basic counter and converter will be reset after the data entry.

FL – FREQUENCY LIMIT LOW - Indicates the numbers and scale factor will set frequency limit low (10 MHz resolution available). The basic counter and converter will be reset after data entry.

RS – RESET BASIC COUNTER AND CONVERTER - Takes a new reading after RESET operation. Does not affect offsets or programmed limits. Has the same function as manual reset button.

HA – HOLD ACTIVE - The counter stops taking readings, data transmission is stopped, and the last frequency read is displayed and held.

HP – HOLD PASSIVE - Terminates HA.

DN – DISPLAY NORMAL - RESETS display only; used for clearing error messages on the display. Cannot be used after verifying preprogrammed data such as FREQUENCY OFFSETS or FREQUENCY LIMITS. This OPCODE affects only the display.

B1 thru B4 – Band 1 thru Band 4 - Chooses the operating band of interest.
Note: B4 (Band 4) requires an additional digit input to designate individual remote sensors (e.g. B41 = remote sensor 1 which covers range of 26.5 to 40 GHz).

R0 thru R9 – Resolution 0 thru 9 - Picks the front panel resolution from 1 Hz to 1 GHz. Also chooses gate time which is related to resolution; 1 Hz = 1 Sec, 10 Hz = 100 Sec, 100 Hz = 10 msec, 1 kHz to 1 GHz = 1 msec.

FA – FAST ACTIVE - Causes the counter to go into the fast cycle mode of operation. In this mode, the front panel sample rate/hold control is inactive and the fastest sample rate is attained. The counter will not go into the FAST ACTIVE mode of operation until HOLD ACTIVE is disabled.

FP – FAST PASSIVE - Terminates FA.

DA – DISPLAY ACTIVE - Outputs frequency reading to both front panel and GPIB Bus.

DP – DISPLAY PASSIVE - Output frequency reading to GPIB Bus only but not to front panel display.

OA – OFFSET ACTIVE - Add frequency and power offset to readings.

OP – OFFSET PASSIVE - Does not add frequency and power offset to readings.

RA – Stay in data output mode during data output. This OPCODE increases output data rate.

RP – Service other operations of the counter after outputting each BYTE.

TN – Service request disabled.

TS – Service request enabled. Counter will pull service request line after each reading.

EZ – EXPONENT ZERO - Output format.

ES – EXPONENT SCIENTIFIC - Output format.

PA – POWER ACTIVE - Enables power meter option.

PP – POWER PASSIVE - Terminates power meter option.

PO – POWER OFFSET - Enables entry of power offsets. Take a new reading after data entry.

TA – TEST ACTIVE - Enables 200 MHz self test. TA mode will automatically be disabled when other OPCODES are entered.

TP – TEST PASSIVE - Terminates test function.

MEASUREMENT OUTPUT FORMAT

The EIP 545/548 transmit the following string of characters to output a measurement.

Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Format																		
EZ (Exponent Zero)	b	±	D	D	D	D	D	D	D	D	D	D	D	D	E	0	CR	LF
ES (Exponent Sci) *	±	D	D	D	D	D	D	D	D	D	D	D	D	D	E	D	CR	LF
Freq. + Power **	(Format for either EZ or ES)																	
	♭	♭	♭	♭	♭	♭	♭	♭	♭	♭	±	D	D	D	•	D	CR	LF

♭ = Blank

D = Digit

CR = Carriage Return

LF = Line Feed

* in Exponent Scientific one digit represents the position of the decimal point. Exponent digit can be either 0, 3, 6, or 9.

** when both frequency and power information is output, two lines of data are presented. The first line is frequency information in either EZ or ES. The second line is the power information and the decimal point is always fixed for 0.1 dB resolution.

Note: including blanks, 18 characters are always transmitted.

READING A MEASUREMENT

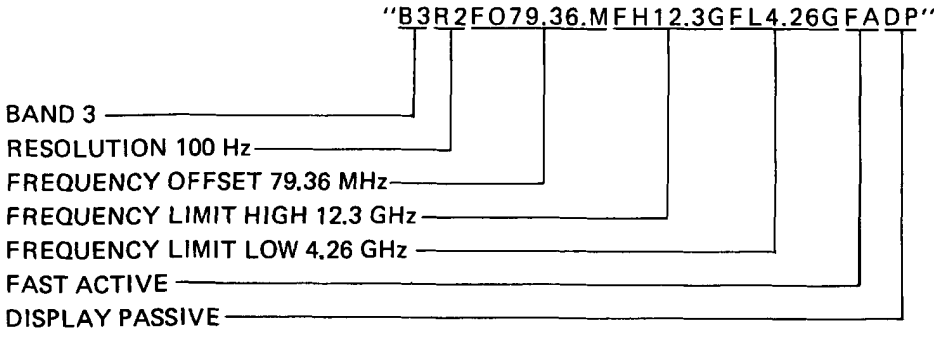
To read a measurement from the counters to a calculate, the counter must first be addressed to talk and the calculator to listen. The examples below indicate how a calculator may read a measurement from the counter.

```
10 red 719, A
20 prt A                    } HP 9825A

10 input @ 19:A
20 print A                  } TEK 4051

10 enter 719, A
20 print A                  } HP 9845A
```

The EIP 545/548 can use two different modes. HA which takes one reading then waits for a reset command or a Device Trigger GPIB Bus Command. In this condition when addressed to talk the counter is sent a reset or Device Trigger and a new reading is output to the BUS. The counter will hold that particular reading on the display until another reset command or Device Trigger command is recieved. The other mode is HP or HOLD PASSIVE. In this mode data is read out in a normal BUS fashion. The display automatically updates corresponding to the sample rate chosen. In this condition successive readings can be output without generating a reset or Device Trigger command each time.

PROGRAM EXAMPLES

By addressing the counter to listen and sending the following program string, it sets up the following measurement conditions.



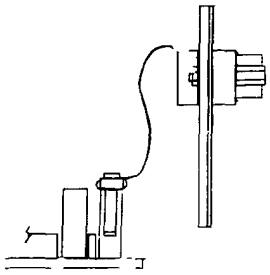
The following programs illustrate how the controllers can control the EIP 545/548 counters. These programs cause the counters to make a series of frequency measurements. The calculators read the measurements into memory and prints the results. The programs assume the counter talk and listen address is decimal "19".

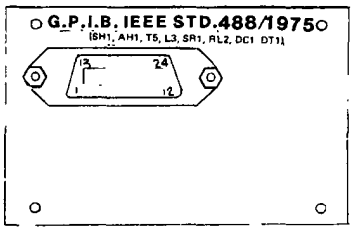
```
HP 9825A    0:  dim A (10)
            1:  rem 7
            2:  wrt 719, "B3R2FO-4.55M"
            3:  wait 300
            4:  for I = 1 to 10
            5:  red 719, A ( I )
            6:  prt A ( I )
            7:  next I
            8:  end
HP9845A     10: output 719, "B3R2FO-4.55M"
            15: wait 300
            20: input 719, A
            30: print "Frequency minus offset equals", A
            40: Go to 20
TEK 4051    10: print @19: "B3R2FO-4.55M"
            20: input @ 19: A
            30: print "Frequency minus offset equals", A
            40: Go to 20
```

The 9825A programs causes the 545/548 to take a series of ten readings, print them on the 9825A paper tape and stop. Notice that an offset of 4.55 MHz is subtracted from each reading.

The programs shown for the 9845A and TEK 4051 cause the counter to make a frequency measurement and print that measurement. To end the program, initiate a "STOP" command. This is accomplished on the 9845A with the key labeled "STOP". On the TEK 4051 use the key labeled "BREAK". To restart the program enter the RUN statement followed by the line number that is printed in the INTERRUPT message.

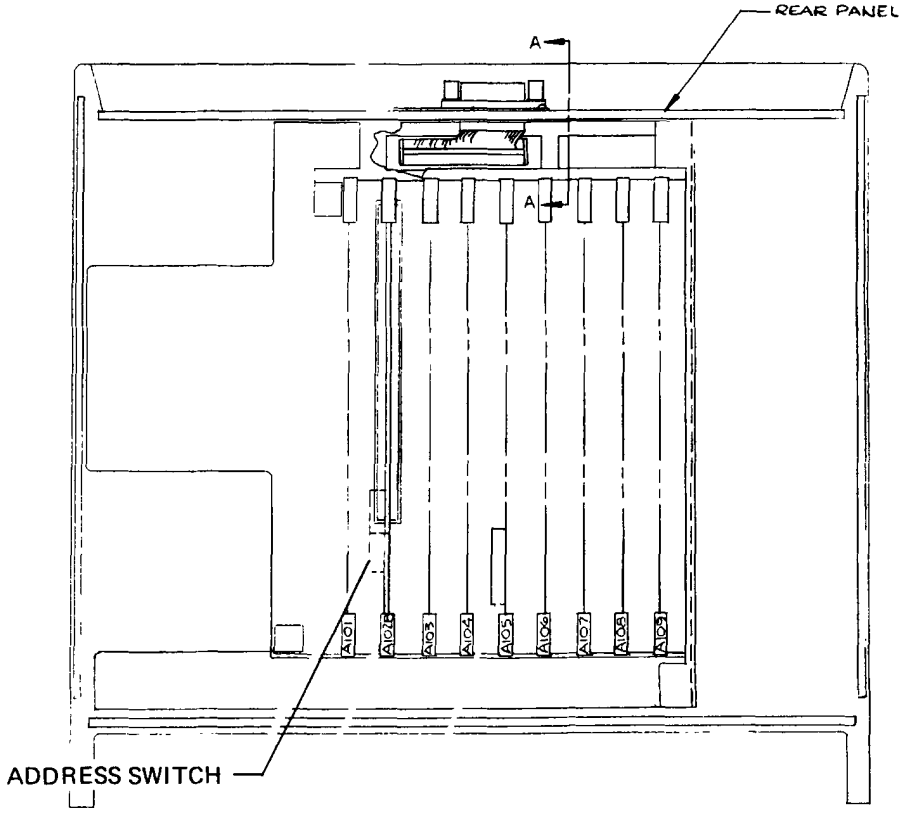
PAGE BLANK INTENTIONALLY





DETAIL A-A

CONTACT	SIGNAL LINE	CONTACT	SIGNAL LINE
1	DIO 1	13	DIO 5
2	DIO 2	14	DIO 6
3	DIO 3	15	DIO 7
4	DIO 4	16	DIO 8
5	EOI	17	REN
6	DAV	18	GND (6)
7	NRFD	19	GND. (7)
8	NDAC	20	GND (8)
9	IFC	21	GND. (9)
10	SRQ	22	GND. (10)
11	ATN	23	GND (11)
12	SHIELD	24	GND. LOGIC



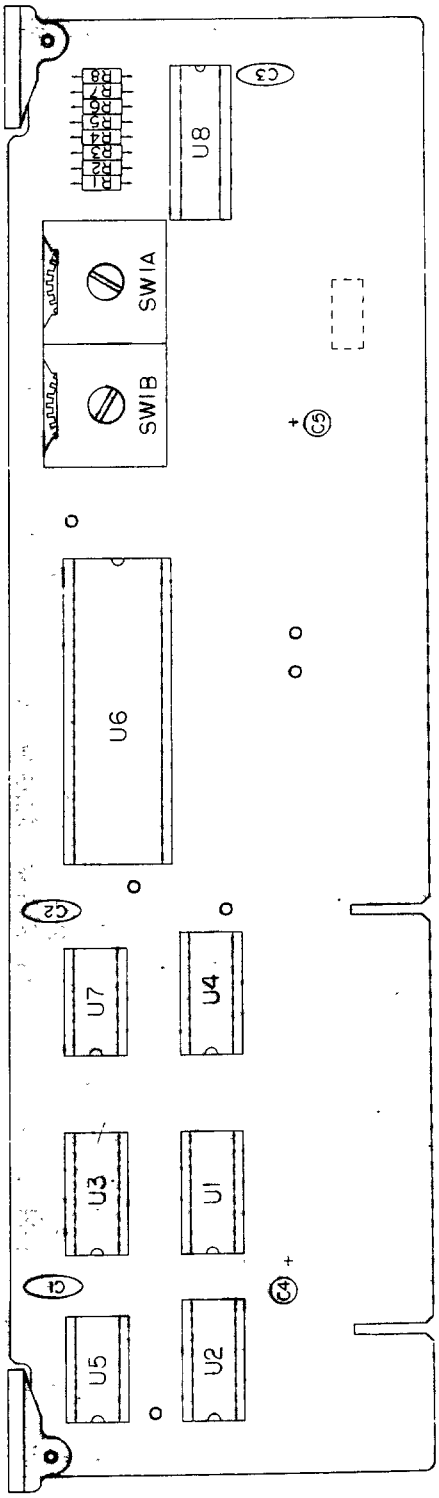
2010140 - A

SEE G.P.I.B MANUAL FOR ADDRESS SETTING INSTRUCTIONS.

Figure 08-2. Location of GPIB in Counter

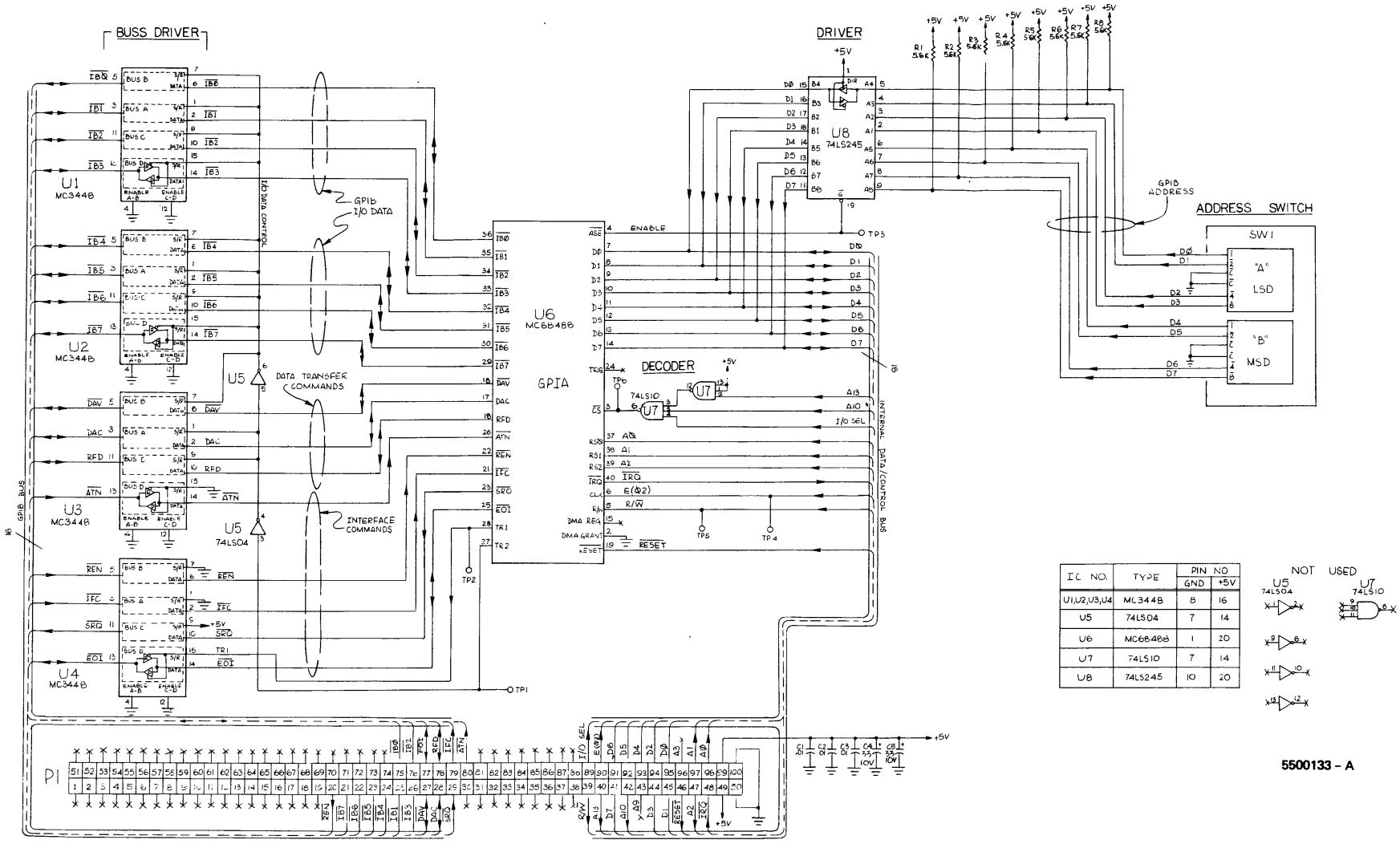
OPTION 08—GENERAL PURPOSE INTERFACE BUS 2010140

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
08	GPIB Option	2010140		EIP	
-1	PCB Assy, GPIB (A102B)	2020133	1	EIP	
C1	Cer, .01μF, %, V	2150003	3	TG - S10	
C2	C1				
C3	C1				
C4	Tant, 33μF, %, 10V	2300015	2	TAG20 - 33/10 - 50	
C5	C4				
R1 thru R8	Comp, 5.6K, 5%, W	4010562	8	RC07GF562J	
SW1A and SW1B	Thumbwheel Switch	4540004	1	2X2270 - 0000	
TP1 thru TP6	P.C. pin .040 diameter	2620032	6	460-2970-02-03	
U1 thru U4	Quad 3-state Bus Transciever	3053448	4	MC3448	
U5	Hex Inverter	3087404	1	74LS04	
U6	General Purpose Interface Adaptor	3058488	1	MC68488	
U7	Tri Input NAND Gate	3087410	1	74LS10	
U8	Oct Bus Transciever	3084245	1	74LS245	



2020133 - A

Figure 08-3. GPIB Component Locator



IC NO.	TYPE	PIN NO	
		GND	+5V
U1,U2,U3,U4	MC3448	8	16
U5	74LS04	7	14
U6	MC68488	1	20
U7	74LS10	7	14
U8	74LS245	10	20

5500133 - A

Figure 08-4. GPIB Schematic

OPTION 09
REAR PANEL INPUT

Option 09 provides rear panel input for 545/548 counters and counters equipped with option 06 in the following manner:

545/548 Counters:

1. Reversing the converter assembly so that the Band 3 input connector protrudes through the hole in the rear panel that is identified as J113.

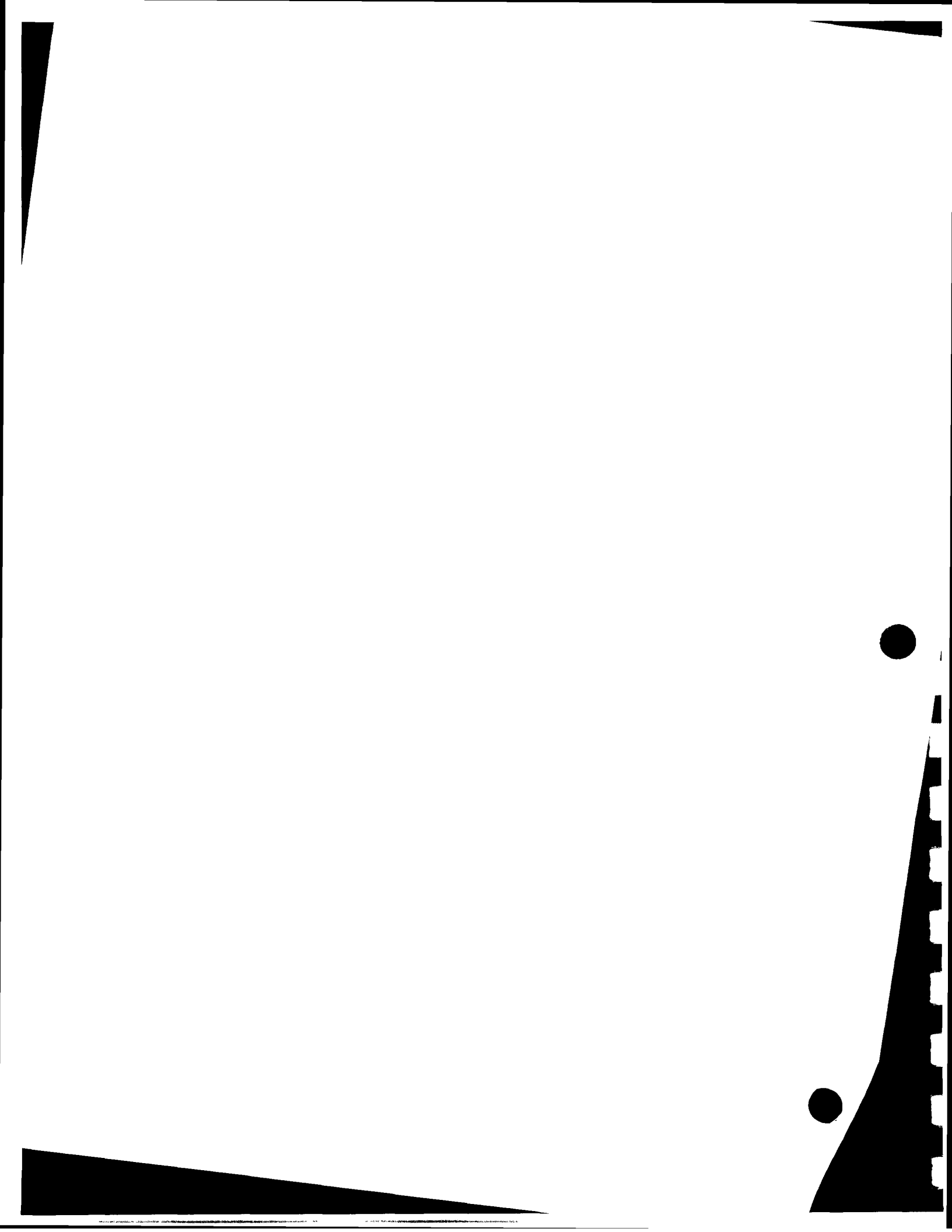
2. Reversing the Band 1 and Band 2 connectors to the holes marked J111 and J112 respectively on the rear panel.

Option 06 Equipped Counters:

1. Reversing the converter assembly so that the Band 3 input connector protrudes through the hole in the rear panel that is identified as J113. Reversing the Remote Sensor and Band 3 jumper connectors to the holes marked J114A (Rmt. Sensor) and J114B (Band 3 connector) respectively.

2. Reversing the Band 1 and Band 2 connectors to the holes marked J111 and J112 respectively on the rear panel.

NOTE: The specifications for the counter do not change when the input is from the rear panel.



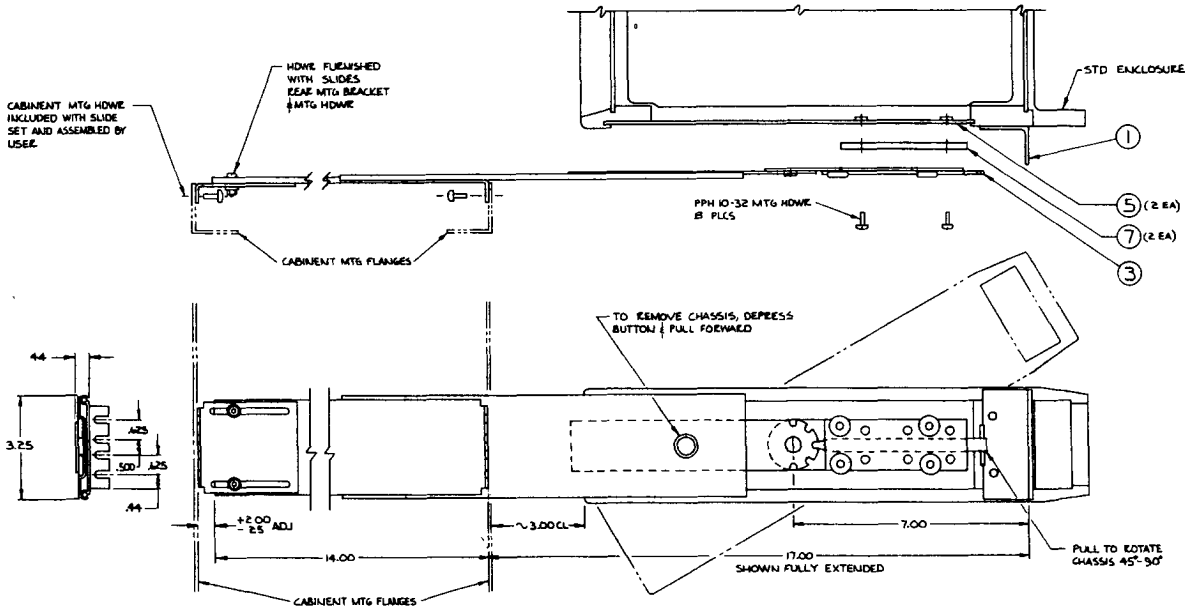
OPTION 10
CHASSIS SLIDE

Option 10 equips your counter with the hardware required to mount the unit in a standard 19" wide console. With the chassis slide installed the counter can be serviced without removing it from the rack.

The option consists of:

OPTION 10 – 2010147

①	Rack Mount Kit	– 2010008-01
③	Slide Set	– 5000189
⑤	Side Panels	– 5210179
⑦	Spacers	– 5210249



1. All MTG HDWR and hole spacing conforms to MIL-STD-189.
2. To install slides in field; Remove top cover and top frame; Mount special side panels (5210179) on Std. enclosure.
3. Item numbers within ◯ symbol are on P/L 2010147. All other items assembled or exploded are shown for clarification or reference only.

Side View of Counter With Option 10 Installed

APPENDIX A
ACCESSORIES

REMOTE SENSORS

The remote sensor that is now available is the model 591 that provides a frequency range of 26.5 - 40 GHz, -20 dBm sensitivity, and maximum input of +7 dBm. The sensors for 40 - 60 GHz, 60 - 90 GHz, and 90 - 110 GHz will be available in the near future. Please contact EIP or your local representative for more information. The following is a copy of the label for the 591 sensor. It contains all the information you will require for operation and ordering.

SPECIFICATIONS – MODEL 591

RANGE	26.5 – 40 GHz
SENSITIVITY	-20 dBm
CONNECTOR	UG599/U Waveguide Flange (WR28 waveguide)
MAX. INPUT LEVEL	+5 dBm
DAMAGE LEVEL	+10 dBm

THIS KIT SHOULD CONTAIN :

LO Coax Cable, Long, part number 2040217
IF Coax Cable, Short, part number 2040218
26.5 - 40 GHz Sensor, part number 2030022

TO INSTALL :

Before connecting the remote sensor to the frequency source, verify that the power level is within the limits specified for the sensor.

Connect the long LO cable from the upper jack to the remote sensor.

Connect the short IF cable from the lower jack, on the front panel, to the Band 3 input.

CAUTION

To avoid static discharge that can damage or destroy the diode in the remote sensor, connect the LO cable to the counter first, then touch the shield to the body of the sensor.

TO OPERATE :

The 591 sensor is designated as Band 41 on the model 548 counter. On counters equipped with Option 06 Extended Frequency and the 591 remote sensor , Band 41 is selected by :

PRESS : BAND [ ] [4] [1]

NOTE

Frequency limits (low/high) and power meter function (Option 02) are operational only to 26.5 GHz.

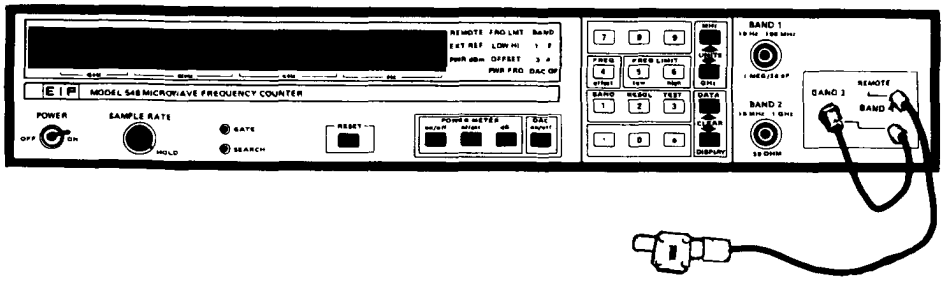
TO REPAIR :

The remote sensor requires no maintenance. If loss of sensitivity is experienced, the diode in the mixer may be damaged. This diode can be replaced. Unscrew the knurled cap and pull out the diode. Replace it with a 1N53B type diode that can be ordered from the manufacturer.

Alpha Industries, Inc.
20 Sylvan Road
Woburn, Mass 01807

Or the diode can be ordered from EIP as part number 2730053.

Return this sensor to EIP for all other repairs.



SERVICE KIT

This service kit for the 545/548 counter contains the following:

2000017 – Service Kit

2020147 – GPIB/BCD extender board

2020184 – Standard extender board

2020185 – Band 2 extender board

2040221 – Cable, BNC to Select

2040222 – Cable, BNC to PC JK

2040225 – Cable, 3 way adapter

2610054 – Test Cable, BNC E/Z HK

5000094 – IC Extractor tool

The kit comes in a handy carrying case.

SPECIAL W-10

MANUAL CHANGE INFORMATION
MODEL 545

THE FOLLOWING CHANGE APPLYS TO THE W-10 MODIFICATION OF A BASIC COUNTER, AND DOES NOT INCLUDE OTHER CHANGES DUE TO THE ADDITION OF OTHER OPTIONS OR MODIFICATIONS.

IN ANY CORRESPONDENCE OR PARTS ORDERING RELATED TO THIS COUNTER BE SURE TO SPECIFY THE COMPLETE MODEL AND SERIAL NUMBER OF THE COUNTER.

DESCRIPTION:
The W-10 special modifications to the 545 counter provide electromagnetic interference (EM1) in accordance with U.S. Navy contract specifications.

MANUAL CHANGE INFORMATION

MODEL 545 / 548

At EIP we continually strive to keep up with the latest electronic developments by adding circuit and component improvements to our instruments as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes into the printed manuals immediately. As a result, your counter may contain some or all of the following changes.

PAGE NUMBER

3-3 Add to the Band 3 Operation the following note.

CAUTION
IN THE RANGE OF 2.0 to 7.6 GHz, THE COUNTER RESET BUTTON SHOULD BE DEPRESSED SO THAT THE YIG (YTTRIUM-IRON-GARNET) FILTER WILL BE CENTERED ON THE INPUT FREQUENCY AND THEREBY DECREASE THE VSWR

3-4 Rear panel fuse should read : "Use a 1 A, S/B, MDL type for 100/120V operation.
"Use a .50 A, S/B, FST type for 220/240V operation.

6-2 Figure 6-1, LINE (col 2) — A15 (U4 pin 8) should be bared.
— A14 (pin 10) should be bared.

6-20 Test 07 is correct as written for counters with PROMs at revision M. Test 07 with PROMs at revision N should read :

07 VCO Test This test cycles the VCO frequency from 400 to 500 MHz, in increments of 50 kHz. The cycle rate can be adjusted by the sample rate pot. 07 tests the VCO and the phase lock circuitry.

9-3 Item 2, fuse 5000079 has been changed to 1 A, S/B, part number 5000085.
fuse 5000168 has been changed to .50 A, S/B, part number 5000169.

9-4. Cables - Band 1 Coax part number 2040165 should be cross referenced as A1J111 - A109J6.

100-3 A100 Counter Interconnect (2020180)
— Change J6 to Str Hdr type, part number 2620186
— Change J7 to Str Hdr type, part number 2620187
— Change XA101 connector to part number 2620183
— Change XA102 connector to part number 2620185
— Change XA103 connector to part number 2620184

106-3 Count Chain Assy (2020136) — Q2, Q3, Q7 are now type SMT1128, part number 4710035
Mark schematic (5500136) on page 106-7.

108-4 A103 Converter Control (2020138)
— Change R9 to 5.1M, part number 4010515
— Add C15, Mica, 150pF, part number 2250005.

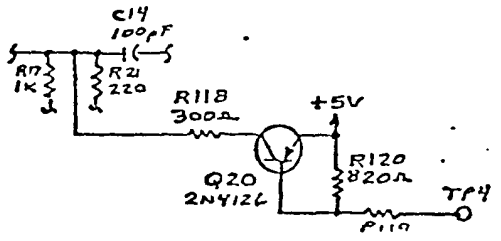
108-5
— Change R34 to 200 ohm, part number 4010201.

108-7 A103 Converter Control (5500138)
— Add C15 between ground and the junction of U8c, pin 10 and R34. Mark schematic with changes to R9, C15, and R34.

109-6 Band 2 Converter (2020139)
— Add Q20, same as Q6, Change quantity of part number 4704126 to 7.
— Q9, Q11 now NPN RF, part number 4710024

109-8 Band 2 Converter (2020139)
— Add R118, Comp, 300 ohm, ¼W, part number 4010301
— Add R119, Comp, 3.9K ohm, ¼W, part number 4010392
— Add R120, Comp, 820 ohm, ¼W, part number 4010821

109-11 Band 2 Converter Schematic (5500139)
— Add circuit to schematic as shown below.



PAGE NUMBER

01-9 A103 DAC Option (2020145) — R2 is now Prec, 20K, 1%, ¼W, part number 4052002
— R3 is now Prec, 2.8K, 1%, ¼W, part number 4052871
— U1 is now LM741CN, part number 3040741
— Change A103 to A104
— Change C3 to 100 pF, part number 2260034

01-11 A103 DAC Schematic (5500145) — Mark schematic with component value changes.

03/04/05-6 Time Base Options (2020144) — Change U1 to type uA78MGUIC
— Change U2 to type uA79MGUIC

08-5 GPIB Option — Add DAC Option code set : DC00 — Turn DAC off
DC01 — Select 1 Hz digit
thru
DC12 — Select 100 GHz, 10 GHz, 1 GHz, digits

08-9 Add to available commands : DC, DC01 thru DC12 — DAC Option digits selection
Picks the MSD of three consecutive digits to be transfered to DAC Assy.

08-14 Detail AA, cable should be attached to the bottom of connector for GPIB on rear panel.

05-6 Figure 05-4 — Add the following :

Harmonic Number N	
18 - high	102,167 — 105,875 MHz
18 - low	104,329 — 115,125 MHz
19 - high	107,903 — 112,875 MHz
19 - low	110,065 — 115,125 MHz

NOTE : All frequency ranges are shown in MHz, not in GHz.

MANUAL CHANGE INFORMATION

MODEL 545 / 548

At EIP we continually strive to keep up with the latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. As a result, your counter may contain some or all of the changes listed below.

IMPORTANT, PLEASE READ

The signatures will change with the revision level of the PROMs that are installed in each counter. Insert this page in your manual as soon as you unpack the instrument. Match your PROMs to the signatures in the following table.

PROM SET, BASIC

	START	STOP	CLOCK
CONNECTION	A105 U7 PIN 20	A105 U11 PIN 20	A105 TP2
BUTTON	IN ▼	OUT ▲	IN ▼

NODE	SIGNATURE											
A105	REV. L	REV. M	REV. N	REV. P	REV. R	REV. S	REV. T	REV. U	REV. W			
S1 pin 9	32F2	7PHF	HF98	9254	0F65	347P	4P5U	973H	00P7			
10	07H9	P79C	U5PH	91F1	PHU2	30U1	CAUC	H37H	7405			
11	C5A0	PFUF	7U0F	A5U8	90H3	2746	669H	728A	17C7			
12	C7F2	3F48	859H	8903	01HA	5FH9	8708	91F5	13PH			
13	50U8	U8U4	7391	PC26	403A	AHF7	0FU4	0CU3	P7C7			
14	4343	HC75	0145	7U1C	0742	U6U3	362H	44P1	3AAH			
15	8H7C	645U	627C	7C5P	PP7P	F47P	5P67	P97U	6PU1			
16	7F7P	1871	8UH9	6A68	01P6	C2H5	71PP	U265	7453			
+ 5 V	CCPC	CCPC	CCPC	CCPC	CCPC	CCPC	CCPC	CCPC	CCPC			

PROM 1, U20

	START	STOP	CLOCK
CONNECTION	A105 U20 PIN 20	A105 U20 PIN 20	A105 TP2
BUTTON	IN ▼	OUT ▲	IN ▼

NODE	SIGNATURE											
A105	REV. L	REV. M	REV. N	REV. P	REV. R	REV. S	REV. T	REV. U	REV. W			
S1 pin 9	3U29	3464	PUA5	11U8	A52A	AAF9	1C5P	8U26	AA4U			
10	FCHA	130U	HC64	1AF7	354H	0HA0	1U36	PU9F	00C9			
11	0H2A	0A88	7217	5P2H	0A62	AFH2	F78U	3946	5HA3			
12	7883	3H3F	U2U9	3806	0UU6	4F63	CP2H	H4F8	PPPF			
13	9U07	2HF0	65U2	4C1H	5U63	P651	CHCF	F9CP	140U			
14	H06U	8F96	15PH	11UA	P998	24CC	7553	72F2	594U			
15	C6H6	F516	PP11	7612	023P	74F8	7FPF	1HPH	FCP1			
16	H692	537U	2890	PF18	UCUU	P64F	4CHC	A81C	A10H			
+ 5 V	826P	826P	826P	826P	826P	826P	826P	826P	826P			

PROM 2 , U8

	START	STOP	CLOCK
CONNECTION	A105 U8 PIN 20	A105 U8 PIN 20	A105 TP2
BUTTON	IN ▼	OUT ▲	IN ▼

NODE	SIGNATURE											
A105	REV. L	REV. M	REV. N	REV. P	REV. R	REV. S	REV. T	REV. U	REV. W			
S1 pin 9	859C	4HA4	A42F	5AC3	5AC3	HA25	8PP0	4F9H	U44C			
10	7H2F	5P1A	UU86	88AP	88AP	9H97	H705	H016	HF5C			
11	CH85	9833	F2AA	21A7	21A7	5605	6535	8780	67P4			
12	9A0F	62C1	FF47	9176	9176	1UF1	C2UC	907F	PC8A			
13	U63H	3977	H0U0	9PFH	P9FH	6609	3805	PFCA	45HP			
14	8482	170A	3974	HC32	HC32	1U93	0C36	8717	5427			
15	F9C3	2H09	U0P6	18P8	18P8	AU5A	0P3P	F1CU	43H2			
16	AP27	HH74	2UH2	A076	A086	69HA	H1UU	8270	H03C			
+ 5 V	826P	826P	826P	826P	826P	826P	826P	826P	826P			